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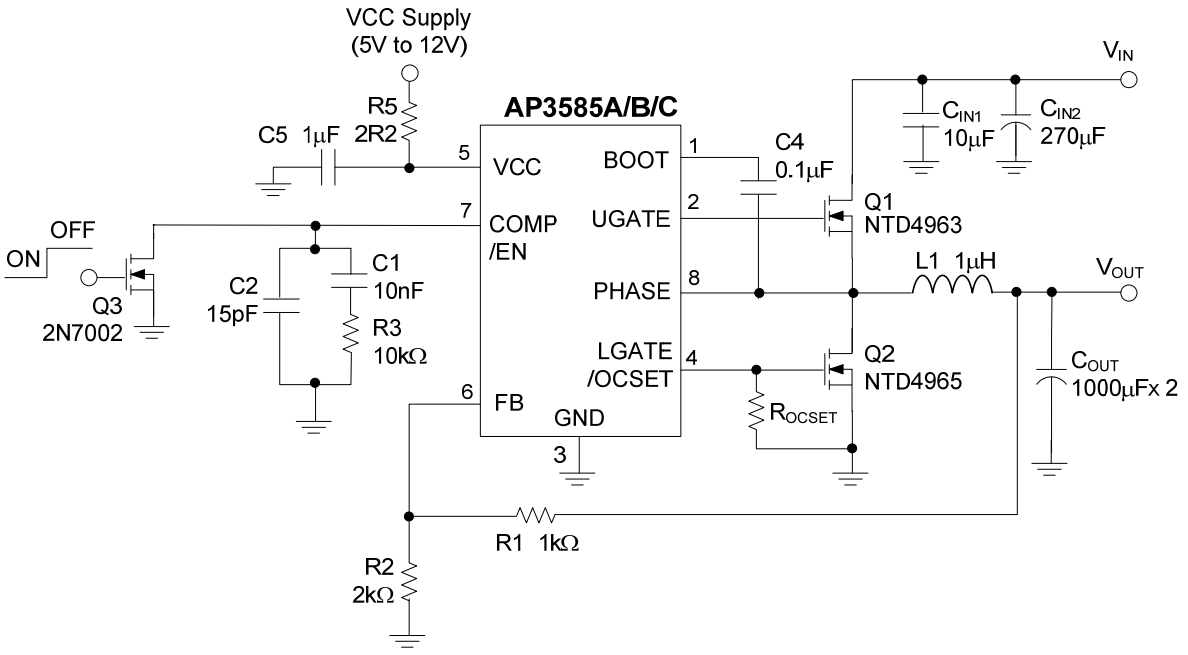
Typical Applications Circuit



Pin Descriptions

Pin Number		Pin Name	Function
SO-8	SO-8EP		
1	1	BOOT	Bootstrap pin. Connect a bootstrap capacitor from this pin to PHASE for creating a BOOT voltage suitable to drive a standard N-Channel MOSFET.
2	2	UGATE	Upper-gate drive pin. Connect this pin to the upper MOSFET gate providing the gate drive. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.
3	3	GND	Ground for the IC. All voltage levels are measured with respect to this pin. Connect this pin directly to the low side MOSFET source and ground plane with the lowest impedance. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
4	4	LGATE/OCSET	Low-side Gate Driver Output and Over-Current Setting Input. This pin is the gate driver for low-side MOSFET. It is also used to set the maximum inductor current. Refer to the section in “Function Description” for detail.
5	5	VCC	Bias supply pin. Provides a 4.5V to 13.2V bias supply for the chip from this pin. The pin should be bypassed with a capacitor to GND.
6	6	FB	Feedback pin. This pin is the inverting input of the internal error amplifier. Use FB pin, in combination with the COMP pin, to compensate the voltage control feedback loop of the converter. A resistor divider from output to GND is used to set the output voltage.
7	7	COMP/EN	Compensation and disable pin. This pin is the output of the Error Amplifier. Pull COMP pin low will shut down the IC.
8	8	PHASE	This pin connects to the source of the upper MOSFET and the drain of the lower MOSFET. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.
–	9	Exposed Pad	Exposed Pad as ground pin.

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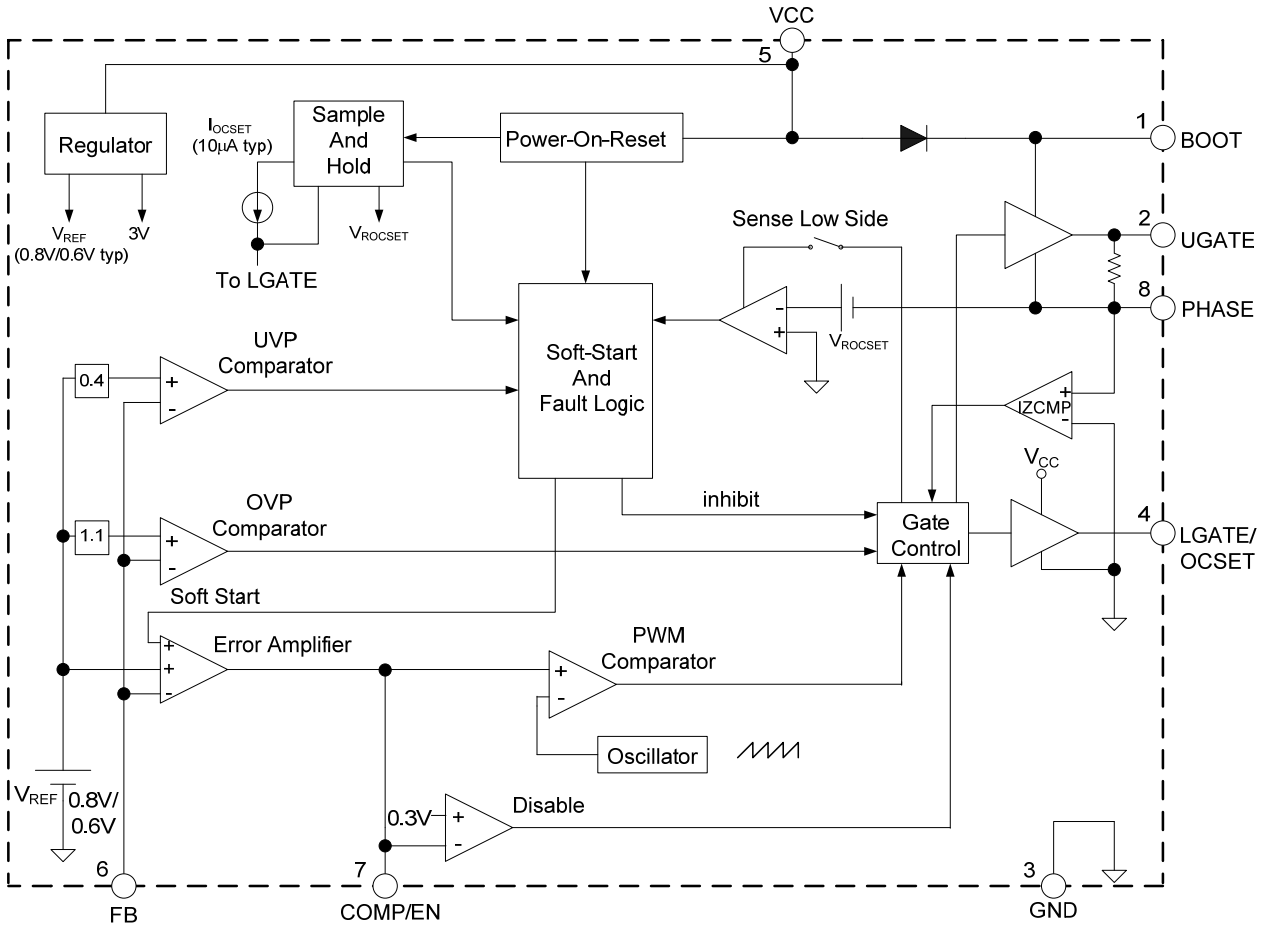
Functional Block Diagram



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Absolute Maximum Ratings (Note 4)

Symbol	Parameter	Rating		Unit
V_{CC}	Supply Input Voltage	-0.3 to 15		V
$V_{BOOT-PHASE}$	BOOT to PHASE Voltage	-0.3 to 15		V
V_{UGATE}	UGATE to PHASE Voltage	DC	-0.3 to $V_{BOOT-PHASE}$+0.3	V
		<200ns	-5 to $V_{BOOT-PHASE}$+5	
V_{PHASE}	PHASE to GND Voltage	DC	-0.3 to 15	V
		<200ns	-5 to 30	
V_{LGATE}	LGATE to GND Voltage	DC	-0.3 to V_{CC}+0.3	V
		<200ns	-5 to V_{CC}+5	
	Other Pin Voltage	-0.3 to 6		V
P_D	Power Dissipation	SO-8	0.87	W
		SO-8EP	1.43	
θ_{JA}	Thermal Resistance (Junction to Ambient)	SO-8	115	°C/W
		SO-8EP	70	
θ_{JC}	Thermal Resistance (Junction to Case)	SO-8	22	°C/W
		SO-8EP	22	
T_J	Junction Temperature	-40 to +150		°C
T_{STG}	Storage Temperature	-65 to +150		°C
T_{LEAD}	Lead Temperature (Soldering, 10 sec)	+260		°C
–	ESD (Human Body Model) (Note 5)	2000		V
–	ESD (Machine Model) (Note 5)	200		V

Notes: 4. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.

5. Devices are ESD sensitive. Handling precaution is recommended.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Input Voltage	4.5	13.2	V
T_A	Operating Ambient Temperature	-40	+85	°C

Electrical Characteristics (V_{CC} = 12V, T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SUPPLY INPUT						
I_{CC}	Supply Current	UGATE and LGATE Pins Open; Switching	–	5	–	mA
I_{CC_Q}	Quiescent Supply Current	V_{FB} = V_{REF}+0.1V, No Switching	–	4	–	mA
V_{IN}	Power Input Voltage	–	3.0	–	13.2	V

NEW PRODUCT

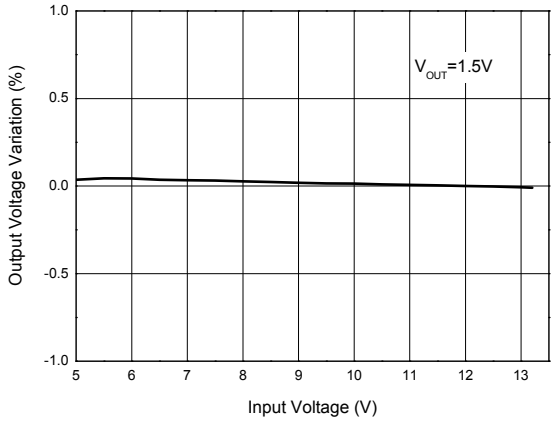
Electrical Characteristics (Cont. V_{CC} = 12V, T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
POWER ON RESET						
V_{POR}	V_{CC} Rising Threshold	V_{CC} Rising	4.0	4.2	4.4	V
V_{POR_HYS}	V_{CC} Threshold Hysteresis	–	–	500	–	mV
ERROR AMPLIFIER						
G_{DC_OL}	Open Loop DC Gain	–	55	70	–	dB
G_{BW}	Gain-bandwidth Product	–	–	10	–	MHz
SR	Slew Rate	–	3	6	–	V/μs
–	Transconductance	–	–	800	1100	μA/V
–	Output Source Current	$V_{FB} < V_{REF}$	80	120	–	μA
–	Output Sink Current	$V_{FB} > V_{REF}$	80	120	–	μA
PWM CONTROLLER GATE DRIVERS						
I_{UG_SRC}	Upper Gate Source Current	V_{BOOT}-V_{PHASE} = 12V, V_{BOOT}-V_{UGATE} = 6V	–	-1.0	–	A
I_{UG_SNK}	Upper Gate Sink Current	V_{BOOT}-V_{PHASE} = 12V, V_{BOOT}-V_{UGATE} = 6V	–	1.5	–	A
R_{UGATE}	Upper Gate Sink Resistance	50mA Source Current	–	2	4	Ω
I_{LG_SRC}	Lower Gate Source Current	V_{CC}-V_{LGATE} = 6V	–	-1	–	A
I_{LG_SNK}	Lower Gate Sink Current	V_{LGATE} = 6V	–	1.5	–	A
R_{LGATE}	Lower Gate Sink Resistance	50mA Source Current	–	1	2	Ω
–	PHASE Falling to LGATE Rising Delay	V_{PHASE} < 1.2V to V_{LGATE} > 1.2V	–	30	–	ns
–	LGATE Falling to UGATE Rising Delay	V_{LGATE} < 1.2V to (V_{UGATE}-V_{PHASE}) > 1.2V	–	30	–	ns
–	Minimum Duty Cycle	–	–	0	–	%
–	Maximum Duty Cycle	–	75	82	89	%
OSCILLATOR						
f_{OSC}	Oscillator Frequency	AP3585A/B	270	300	330	kHz
		AP3585C	180	200	220	
ΔV_{OSC}	Ramp Amplitude	–	–	1.4	–	V_{P-P}
REFERENCE VOLTAGE						
V_{FB}	Feedback Voltage	AP3585A	0.788	0.8	0.812	V
		AP3585B/C	0.591	0.6	0.609	V
I_{FB}	Feedback Bias Current	V_{FB} = 5V	–	10	50	nA
PROTECTION						
V_{FB_UVP}	Under Voltage Protection	–	0.3	0.4	0.5	V
V_{FB_OVP}	Over Voltage Protection	AP3585A	–	1.1	–	V
		AP3585B/C	–	0.8	–	
I_{OCSET}	OC Current Source	–	9	10	11	μA
V_{OCP_MAX}	Built-in Maximum OCP Voltage	–	–	0.375	–	V
t_{SS}	Soft-start Interval	AP3585A	–	2	–	ms
		AP3585B	–	1.5	–	
		AP3585C	–	2.4	–	
$V_{COMP/EN}$	Enable Threshold	–	0.25	0.30	0.35	V
T_{OTSD}	Thermal Shutdown	–	–	+160	–	°C
T_{HYS}	Thermal Shutdown Hysteresis	–	–	+20	–	°C

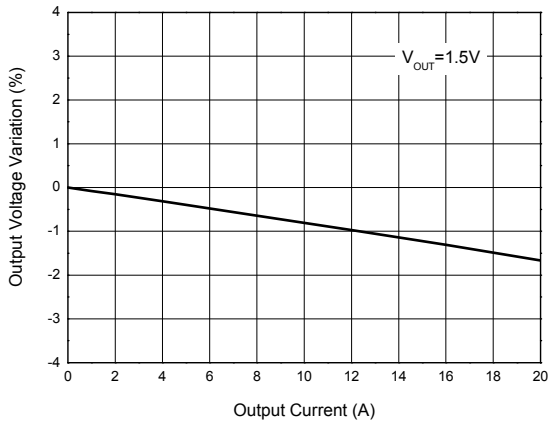
NEW PRODUCT

Performance Characteristics

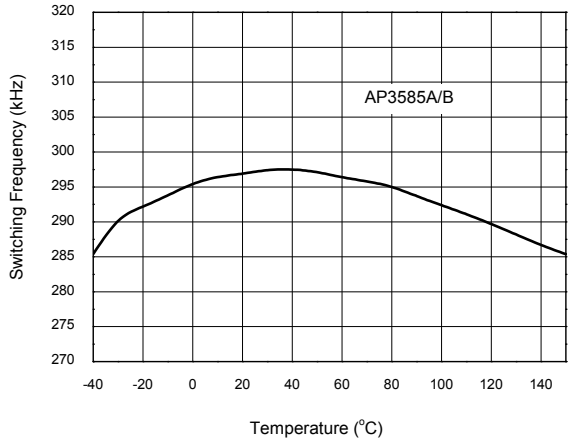
Line Regulation



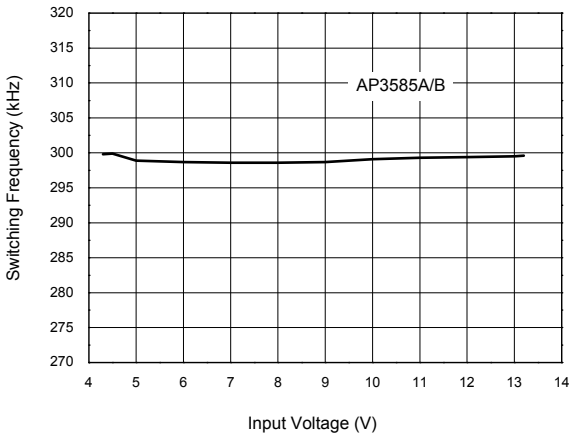
Load Regulation



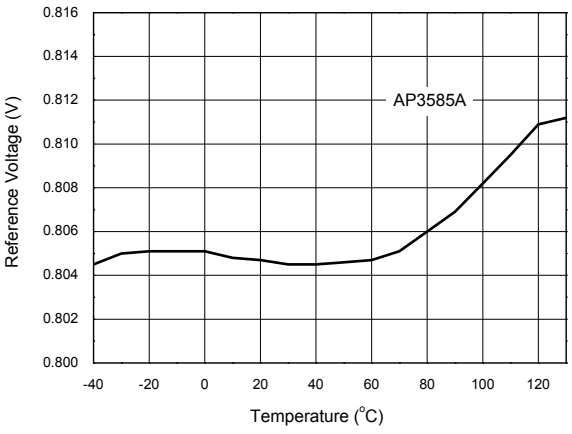
Switching Frequency vs. Temperature



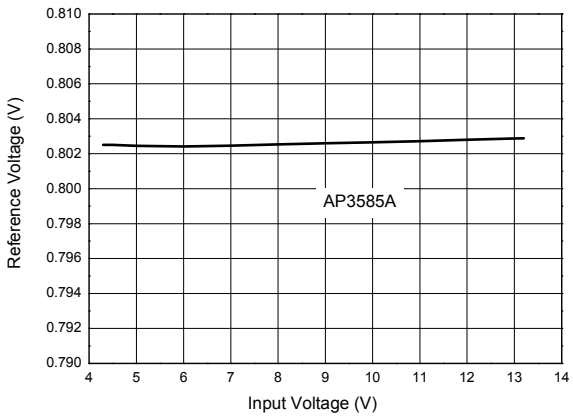
Switching Frequency vs. Input Voltage



Reference Voltage vs. Temperature



Reference Voltage vs. Input Voltage



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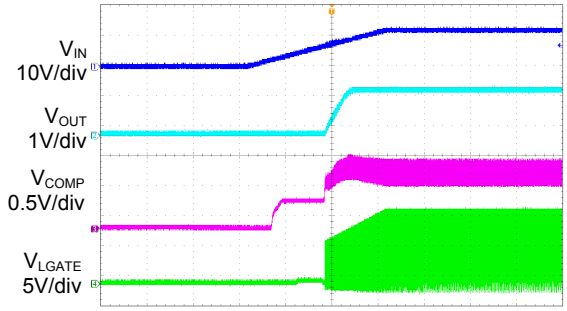
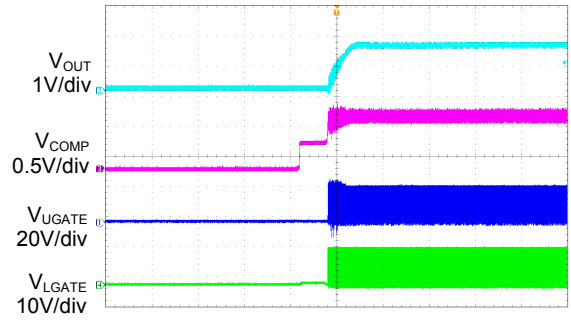
Performance Characteristics (Cont.)

Power-on Waveform (V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 0A)



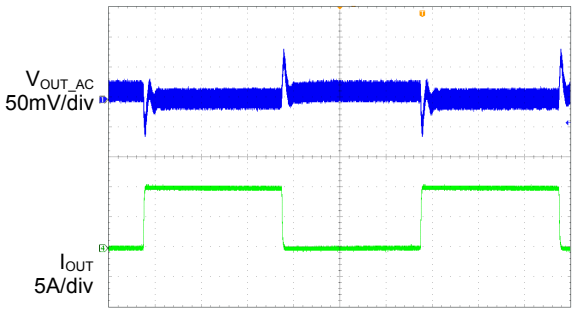
Time 4ms/div

Enable-on Waveform (V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 0A)



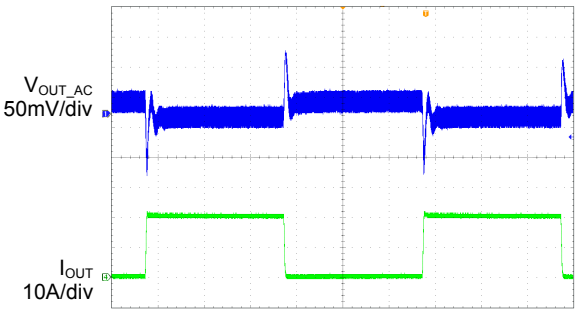
Time 4ms/div

Load Transient Response (V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 0A to 10A)



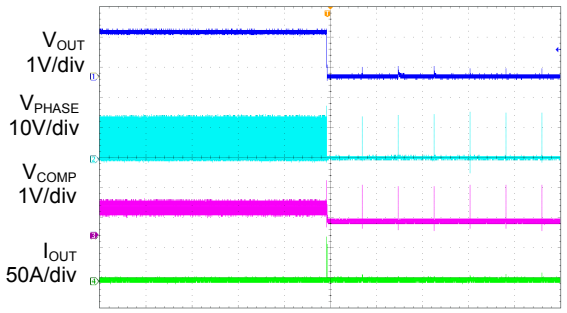
Time 400µs/div

Load Transient Response (V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 0A to 20A)



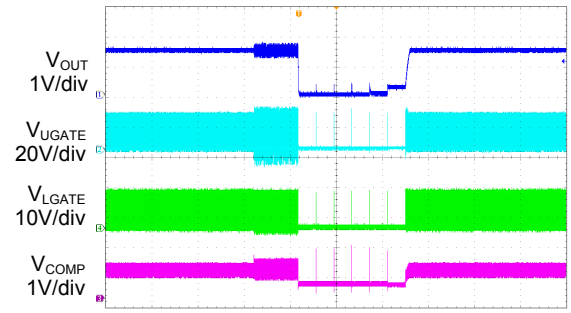
Time 400µs/div

Over Current Protection (V_{IN} = 12V, V_{OUT} = 1.5V)



Time 10ms/div

Under Voltage Protection (V_{IN} = 12V, V_{OUT} = 1.5V)

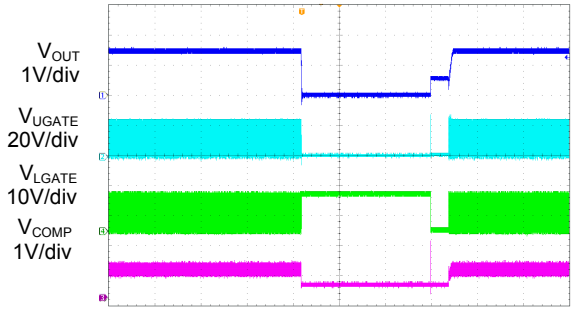


Time 20ms/div

NEW PRODUCT

Performance Characteristics (Cont.)

Over Voltage Protection (V_{IN} = 12V, V_{OUT} = 1.5V)



Time 20ms/div

NEW PRODUCT

Functional Descriptions

The AP3585A/B/C is a voltage-mode single phase synchronous buck controller with embedded MOSFET drivers. This part provides complete protection functions such as over voltage protection, under voltage protection and over current protection. Inductor current information is sensed by $R_{DS(ON)}$ of the low side MOSFET. The over current protection threshold can be simply programmed by a resistor.

Power on Reset and Chip Enable

A power on reset (POR) circuitry continuously monitors the supply voltage at VCC pin. Once the rising POR threshold is exceeded, the AP3585A/B/C sets itself to active state and is ready to accept chip enable command. The rising POR threshold is typically 4.2V at VCC rising.

The COMP/EN is a multifunctional pin: control loop compensation and chip enable as shown in Figure 1. An Enable Comparator monitors the COMP/EN pin voltage for chip enable. A signal level transistor is adequate to pull this pin down to ground and shut down AP3585A/B/C. A 120µA current source charges the external compensation network with 0.45V ceiling when this pin is released. If the voltage at COMP/EN pin exceeds 0.3V, the AP3585A/B/C initiates its soft start cycle.

The 120µA current source keeps charging the COMP pin to its ceiling until the feedback loop boosts the COMP pin higher than 0.45V according to the feedback signal. The current source is cut off when V_{COMP} is higher than 0.45V during normal operation.

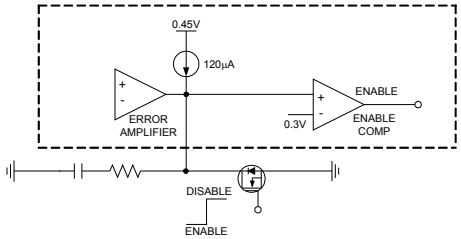


Figure 1. Chip Enable Function

Soft Start

A built-in Soft Start is used to prevent surge current from power supply input V_{IN} during turn-on (Referring to the Functional Block Diagram). The error amplifier is a three-input device. Reference voltage V_{REF} or the internal soft start voltage SS whichever is smaller dominates the behavior of the non-inverting inputs of the error amplifier. SS internally ramps up to 0.8V in 2ms for AP3585A (to 0.6V in 1.5ms for AP3585B and 0.6V in 2.4ms for AP3585C) after the soft start cycle is initiated. The ramp is created digitally, so there will be 100 small discrete steps. Accordingly, the output voltage will follow the SS signal and ramp up smoothly to its target level.

The SS signal keeps ramping up after it exceeds the internal 0.8V for AP3585A (0.6V for AP3585B/C) reference voltage. However, the internal 0.8V for AP3585A (0.6V for AP3585B/C) reference voltage takes over the behavior of error amplifier after SS > V_{REF}. When the SS signal climbs to its ceiling voltage (4.2V), AP3585A/B/C claims the end of soft start cycle and enables the under voltage protection of the output voltage.

Figure 2 shows a typical start up interval for AP3585A/B/C where the COMP/EN pin has been released from a grounded (system shutdown) state. The internal 120µA current source starts charge the compensation network after the COMP/EN pin is released from ground at T1. The COMP/EN exceeds 0.3V and enables the AP3585A/B/C at T2. The COMP/EN continues ramping up the stays at 0.45V before the SS starts ramping at T3. The output voltage follows the internal SS and ramps up to its final level during T3 and T4. At T4, the reference voltage V_{REF} takes over the behavior of the error amplifier as the internal SS crosses V_{REF}. The internal SS keeps ramping up and stays at 4.2V at T5, where AP3585A/B/C asserts the end of soft start cycle.

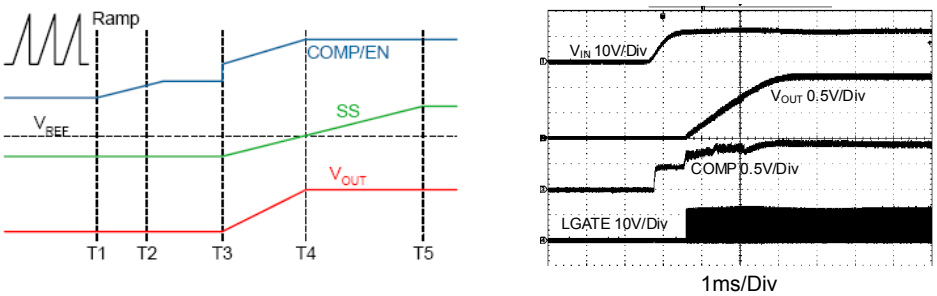


Figure 2. Soft Start Behavior of AP3585A/B/C

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Functional Descriptions (Cont.)

Power Input Detection

The AP3585A/B/C detects PHASE voltage for the present of power input V_{IN} when UGATE turns on the first time. If the PHASE voltage does not exceed 2.0V when UGATE turns on, AP3585A/B/C asserts that V_{IN} is not ready and stops the soft start cycle. However, the internal SS continues ramping up to V_{DD}. Another soft start is initiated after SS ramps up to V_{DD}. The hiccup period is about 1ms. Figure 3 shows the start-up waveform where V_{IN} does not present initially.

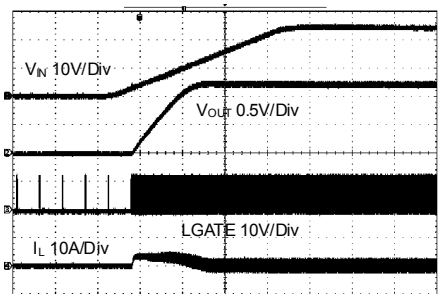


Figure 3. Soft Start Where V_{IN} Does Not Present Initially

Over Current Protection (OCP)

A resistor R_{OCSET} connected from LGATE pin sets the threshold. An internal current source I_{OCSET} (10μA typically), flowing through R_{OCSET} determines the OCP trigger point, which can be calculated using the following equation:

$$I_{LIMIT} = \frac{I_{OCSET} \times R_{OCSET}}{R_{DS(ON)} \text{ of the low side MOSFET}}$$

If R_{OCSET} is absent or larger than 40kΩ, AP3585A/B/C will work in build-in Maximum OCP Mode. Then the current limit will be:

$$I_{LIMIT} = 375mV / R_{DS(ON)}$$

Because the $R_{DS(ON)}$ of MOSFET increases with temperature, it is necessary to take this thermal effect into consideration in calculating OCP point.

When OCP is triggered, both UGATE and LGATE will go low to stop the energy transfer to the load. Controller will try to restart in a hiccupped way. Figure 4 shows the hiccupped over current protection.

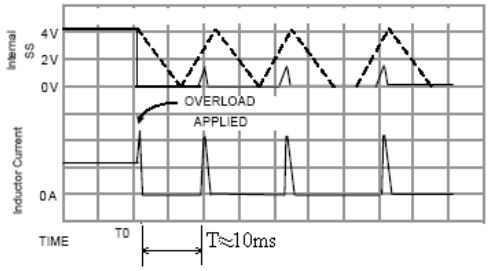


Figure 4. Hiccupped Over Current Protection

Over Voltage Protection (OVP)

The feedback voltage is continuously monitored for over voltage protection. When OVP is triggered, LGATE will go high and UGATE will go low to discharge the output capacitor.

The AP3585A/B/C provides full-time over voltage protection whenever soft start completes or not. The typical OVP threshold is 137.5% of the internal reference voltage V_{REF}. AP3585A/B/C provides non-latched OVP. The controller will return to normal operation if over voltage condition is removed.

Under Voltage Protection (UVP)

The feedback voltage is also monitored for under voltage protection. The under voltage protection has 15μs triggered delay. When UVP is triggered, both UGATE and LGATE will go low. Unlike OCP, UVP is not a latched protection; controller will always try to restart in a hiccupped way.

NEW PRODUCT

Functional Descriptions (Cont.)

Thermal Shutdown

If the junction temperature of the device reaches the thermal shutdown limit of +160°C, the PWM and the oscillator are turned off and UGATE and LGATE are driven low, turning off both MOSFETs. When the junction cools to the required level (+140°C nominal), the PWM initiates soft start as during a normal power-up cycle.

Output Voltage Selection

The output voltage can be programmed to any level between the 0.8V (for AP3585A) internal reference (0.6V for AP3585B/C) to the 80% of V_{IN} supply. The lower limitation of output voltage is caused by the internal reference. The upper limitation of the output voltage is caused by the maximum available duty cycle (80%). This is to leave enough time for over-current detection. Output voltage out of this range is not allowed.

A voltage divider sets the output voltage (Refer to the typical application circuit). In real applications, choose R1 in 100Ω to 10kΩ range and choose appropriate R2 according to the desired output voltage.

$$V_{OUT} = 0.8V \times \frac{R1 + R2}{R2} \qquad \text{AP3585A}$$

$$V_{OUT} = 0.6V \times \frac{R1 + R2}{R2} \qquad \text{AP3585B/C}$$

PCB Layout Considerations

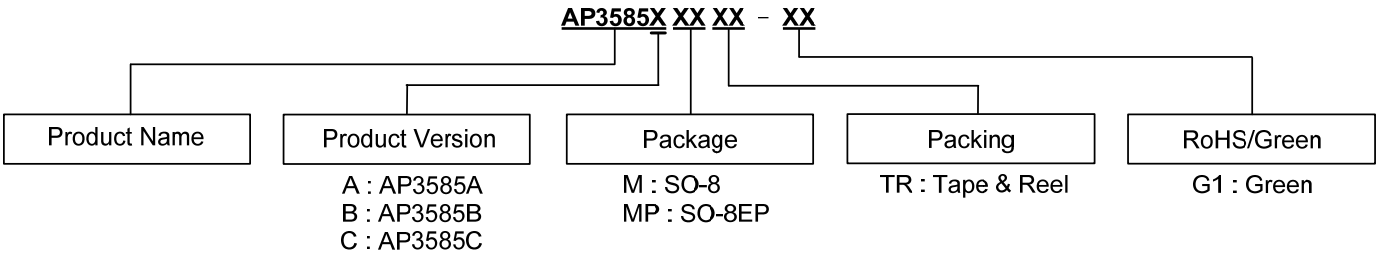
High speed switching and relatively large peak currents in a synchronous-rectified buck converter make the PCB layout a very important part of design. Switching current from one power device to another can generate voltage spikes across the impedances of the interconnecting bond wires and circuit traces. The voltage spikes can degrade efficiency and radiate noise, which results in over-voltage stress on devices. Careful component placement layout a printed circuit design can minimize the voltage spikes induced in the converter.

Follow the below layout guidelines for optimal performance of AP3585A/B/C.

1. The turn-off transition of the upper MOSFET prior to turn-off, the upper MOSFET was carrying the full load current. During turn-off, current stops flowing in the upper MOSFET and is picked up by the low side MOSFET. Any inductance in the switched path generates a large voltage spike during the switching interval. Careful component selections, layout of the critical components, and use shorter and wider PCB traces help in minimizing the magnitude of voltage spikes.
2. The power components and the PWM controller should be placed firstly. Place the input capacitors, especially the high-frequency ceramic decoupling capacitors, close to the power switches. Place the output inductor and output capacitors between the MOSFETs and the load. Also locate the PWM controller near MOSFETs.
3. Use a dedicated grounding plane and use vias to ground all critical components to this layer. Use an immediate via to connect the component to ground plane including GND of AP3585A/B/C.
4. Apply another solid layer as a power plane and cut this plane into smaller islands of common voltage levels. The power plane should support the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers for the PHASE node.
5. The PHASE node is subject to very high dV/dt voltages. Stray capacitance between this island and the surrounding circuitry tend to induce current spike and capacitive noise coupling. Keep the sensitive circuit away from the PHASE node and keep the PCB area small to limit the capacitive coupling. However, the PCB area should be kept moderate since it also acts as main heat convection path of the lower MOSFET.
6. The PCB traces between the PWM controller and the gate of MOSFET and also the traces connecting source of MOSFETs should be sized to carry 2A peak currents.

NEW PRODUCT

Ordering Information



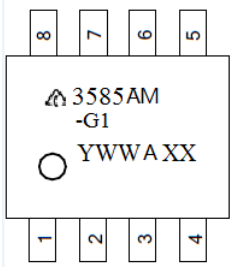
Diodes IC's Pb-free products with "G1" suffix in the part number, are RoHS compliant and green.

Package	Temperature Range	Part Number	Marking ID	Packing
SO-8	-40°C to +85°C	AP3585AMTR-G1	3585AM-G1	4000/Tape & Reel
		AP3585BMTR-G1	3585BM-G1	4000/Tape & Reel
		AP3585CMTR-G1	3585CM-G1	4000/Tape & Reel
SO-8EP		AP3585AMPTR-G1	3585AMP-G1	4000/Tape & Reel
		AP3585BMPTR-G1	3585BMP-G1	4000/Tape & Reel
		AP3585CMPTR-G1	3585CMP-G1	4000/Tape & Reel

Marking Information

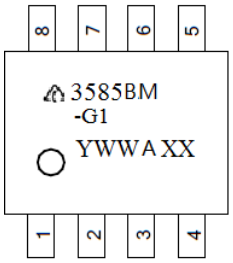
(1) SO-8

(Top View)



First and Second Lines: Logo and Marking ID
Third Line: Date Code
Y: Year
WW: Work Week of Molding
A: Assembly House Code
XX: 7th and 8th Digits of Batch Number

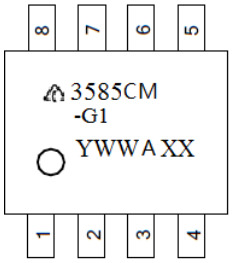
(Top View)



First and Second Lines: Logo and Marking ID
Third Line: Date Code
Y: Year
WW: Work Week of Molding
A: Assembly House Code
XX: 7th and 8th Digits of Batch Number

NEW PRODUCT

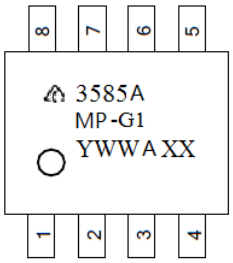
Marking Information (Cont.)



First and Second Lines: Logo and Marking ID
Third Line: Date Code
Y: Year
WW: Work Week of Molding
A: Assembly House Code
XX: 7th and 8th Digits of Batch Number

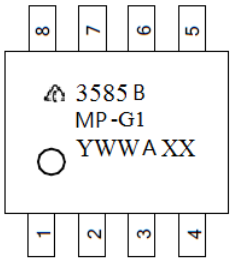
(2) SO-8EP

(Top View)



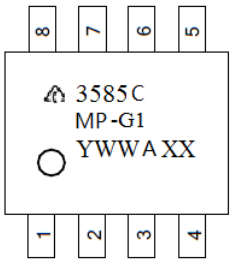
First and Second Lines: Logo and Marking ID
Third Line: Date Code
Y: Year
WW: Work Week of Molding
A: Assembly House Code
XX: 7th and 8th Digits of Batch Number

(Top View)



First and Second Lines: Logo and Marking ID
Third Line: Date Code
Y: Year
WW: Work Week of Molding
A: Assembly House Code
XX: 7th and 8th Digits of Batch Number

(Top View)

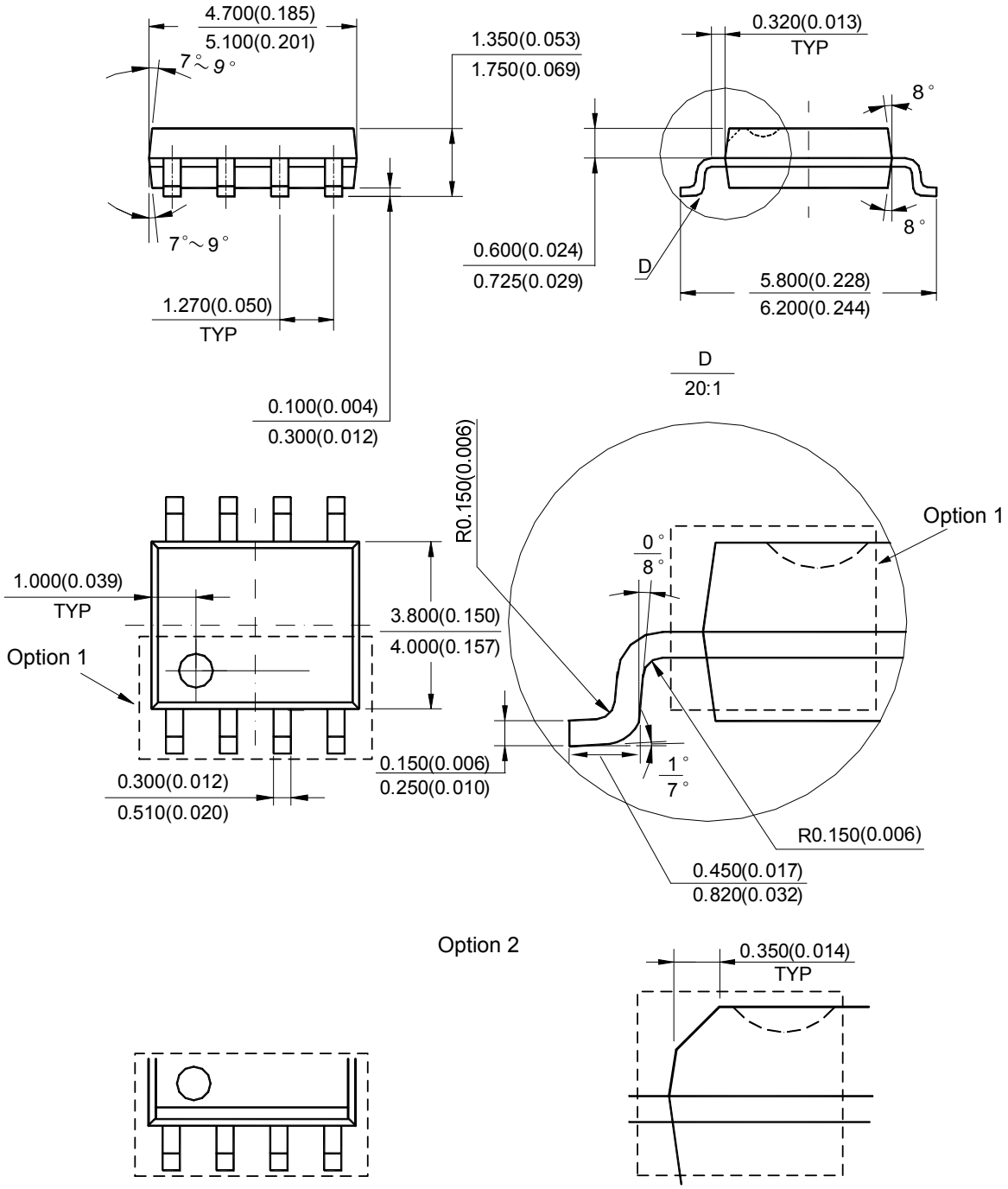


First and Second Lines: Logo and Marking ID
Third Line: Date Code
Y: Year
WW: Work Week of Molding
A: Assembly House Code
XX: 7th and 8th Digits of Batch Number

NEW PRODUCT

Package Outline Dimensions (All dimensions in mm(inch).)

(1) Package Type: SO-8

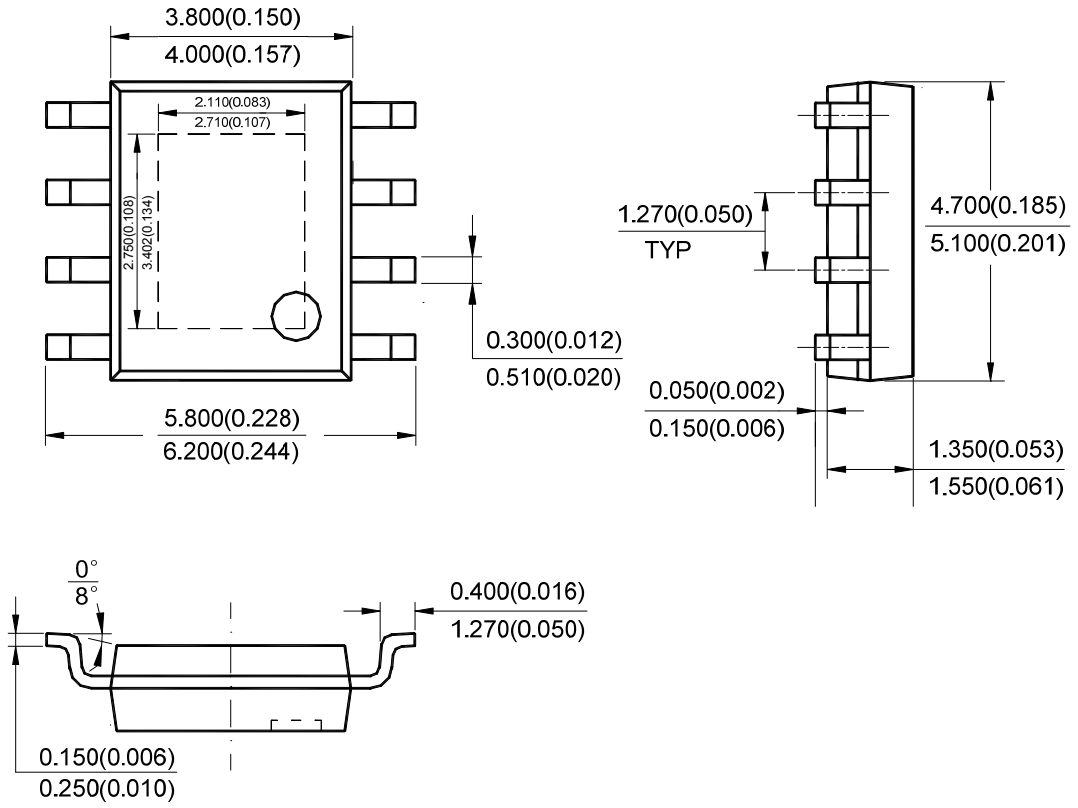


Note: Eject hole, oriented hole and mold mark is optional.

NEW PRODUCT

Package Outline Dimensions (Cont. All dimensions in mm(inch).)

(2) Package Type: SO-8EP

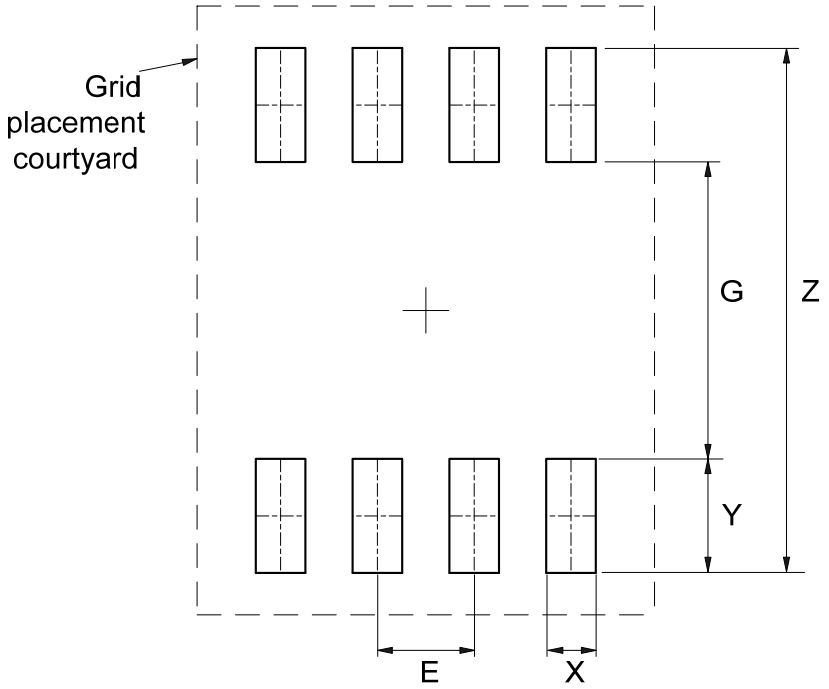


Note: Eject hole, oriented hole and mold mark is optional.

NEW PRODUCT

Suggested Pad Layout

(1) Package Type: SO-8

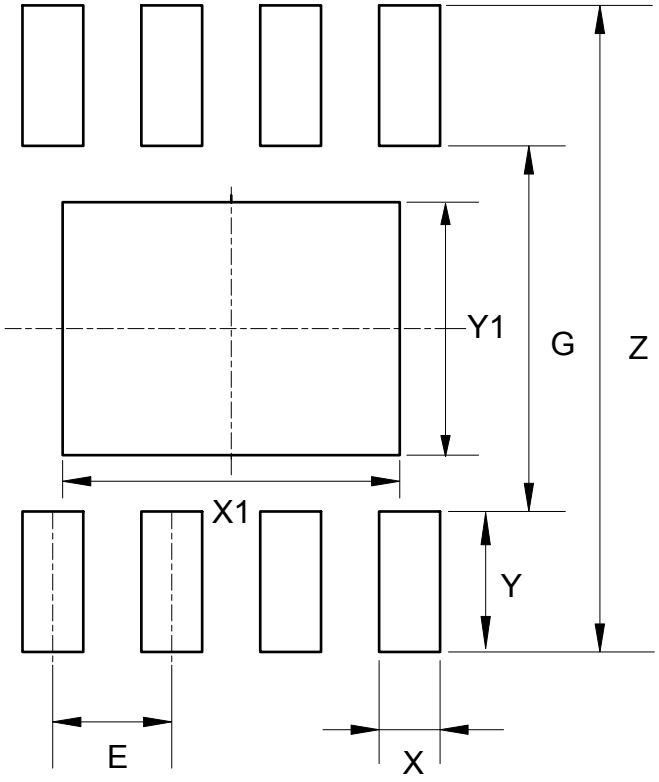


Dimensions	Z (mm)/(inch)	G (mm)/(inch)	X (mm)/(inch)	Y (mm)/(inch)	E (mm)/(inch)
Value	6.900/0.272	3.900/0.154	0.650/0.026	1.500/0.059	1.270/0.050

NEW PRODUCT

Suggested Pad Layout (Cont.)

(2) Package Type: SO-8EP



Dimensions	Z (mm)/(inch)	G (mm)/(inch)	X (mm)/(inch)	Y (mm)/(inch)	X1 (mm)/(inch)	Y1 (mm)/(inch)	E (mm)/(inch)
Value	6.900/0.272	3.900/0.154	0.650/0.026	1.500/0.059	3.600/0.142	2.700/0.106	1.270/0.050

NEW PRODUCT

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