# Low-Voltage, Dual-Supply, SPST, CMOS Analog Switches

## ABSOLUTE MAXIMUM RATINGS

(Voltages Referenced to V-)
V+ .....-0.3V, +13V
Voltage into Any Terminal (Note 1) .....-0.3V to (V+ + 0.3V) or ±10mA (whichever occurs first)
Continuous Current into Any Terminal.....±10mA
Peak Current, NO_ or COM_
(pulsed at 1ms,10% duty cycle).....±20mA
Continuous Power Dissipation ($T_A$ = +70°C)
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) ...727mW
8-Pin SO (derate 5.88mW/°C above +70°C).....471mW
5-Pin SOT23-5 (derate 7.1mW/°C above +70°C) .....571mW
8-Pin CERDIP (derate 8.00mW/°C above +70°C).....640mW
Operating Temperature Ranges
MAX4503C_ _/MAX4504C_ _ .....0°C to +70°C
MAX4503E_ _/MAX4504E_ _ .....-40°C to +85°C
MAX4503MJA/MAX4504MJA .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

**Note 1:** Voltages on any signal terminal exceeding V+ or V- are clamped by internal diodes. Limit forward-diode current to maximum current rating.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS—±5V Supply

(V+ = +4.5V to +5.5V, V- = -4.5V to -5.5V, $V_{INH}$ =3.5V, $V_{INL}$ = 1.5V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.)

| PARAMETER | SYMBOL | CONDITIONS | | | MIN | TYP (Note 2) | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | | |
| Analog Signal Range | $V_{COM}$, $V_{NO}$, $V_{NC}$ | | | | V- | | V+ | V |
| COM to NO or NC On-Resistance | $R_{ON}$ | $V_{COM\_}$ = 3.5V, $I_{COM}$ = 1mA | $T_A$ = +25°C | | | 60 | 250 | Ω |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | | 350 | |
| NO or NC Off Leakage Current (Note 3) | $I_{NO(OFF)}$, $I_{NC(OFF)}$ | V+ = 5.5V, V- = -5.5V, $V_{COM\_}$ = ±4.5V, $V_{NO}$ or $V_{NC}$ = ∓4.5V | $T_A$ = +25°C | | -1 | 0.01 | 1 | nA |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | C, E | -10 | | 10 | |
| | | | | M | -100 | | 100 | |
| COM Off Leakage Current (Note 3) | $I_{COM(OFF)}$ | V+ = 5.5V, V- = -5.5V, $V_{COM\_}$ = ±4.5V, $V_{NO}$ or $V_{NC}$ = ∓4.5V | $T_A$ = +25°C | | -1 | 0.01 | 1 | nA |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | C, E | -10 | | 10 | |
| | | | | M | -100 | | 100 | |
| COM On Leakage Current (Note 3) | $I_{COM(ON)}$ | V+ = 5.5V, V- = -5.5V, $V_{COM}$ = ±4.5V, $V_{NO}$ or $V_{NC}$ = ±4.5V | $T_A$ = +25°C | | -2 | 0.01 | 2 | nA |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | C, E | -20 | | 20 | |
| | | | | M | -200 | | 200 | |
| **DIGITAL I/O** | | | | | | | | |
| IN Input Logic High | $V_{IH}$ | | | | (V+) - 1.5 | | V+ | V |
| IN Input Logic Low | $V_{IL}$ | | | | V- | | (V+) - 3.5 | V |
| IN Input Current Logic High or Low | $I_{IH}$, $I_{IL}$ | $V_{IN}$ = V+, 0V | | | -1 | 0.03 | 1 | µA |

## ELECTRICAL CHARACTERISTICS—±5V Supply (continued)

(V+ = +4.5V to +5.5V, V- = -4.5V to -5.5V, $V_{INH}$ = 3.5V, $V_{INL}$ = 1.5V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP (Note 2) | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **SWITCH DYNAMIC CHARACTERISTICS** | | | | | | | |
| Turn-On Time | $t_{ON}$ | $V_{IN}$ = 3V, $R_L$ = 1kΩ<br>$V_{NO}$ or $V_{NC}$ = 3V, Figure 1 | $T_A$ = +25°C | | 30 | 150 | ns |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | 240 | |
| Turn-Off Time | $t_{OFF}$ | $V_{IN}$ = 3V, $R_L$ = 1kΩ<br>$V_{NO}$ or $V_{NC}$ = 3V, Figure 1 | $T_A$ = +25°C | | 20 | 100 | ns |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | 150 | |
| Charge Injection (Note 4) | Q | $C_L$ = 1nF, $V_{NO\_}$ = 0V, $R_S$ = 0Ω,<br>$T_A$ = +25°C, Figure 2 | | | 1 | 10 | pC |
| Off Isolation | $V_{ISO}$ | $R_L$ = 50Ω, $C_L$ = 15pF, $V_{NO}$ = $1V_{RMS}$,<br>f = 100kHz, $T_A$ = +25°C, Figure 3 | | | <-90 | | dB |
| NO or NC Off Capacitance | $C_{NO(OFF)}$ | f = 1MHz, $T_A$ = +25°C, Figure 4 | | | 3 | | pF |
| COM Off Capacitance | $C_{OFF(COM)}$ | f = 1MHz, $T_A$ = +25°C, Figure 4 | | | 3 | | pF |
| COM On Capacitance | $C_{ON(COM)}$ | f = 1MHz, $T_A$ = +25°C, Figure 4 | | | 9 | | pF |
| **POWER SUPPLY** | | | | | | | |
| V+, V- Supply Current | I+, I- | $V_{IN}$ = 0V or V+ | $T_A$ = +25°C | -125 | 40 | 125 | µA |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | -200 | | 200 | |

# Low-Voltage, Dual-Supply, SPST, CMOS Analog Switches

## ELECTRICAL CHARACTERISTICS—±3V Supply

(V+ = +2.7V to +3.3V, V- = -2.7V to -3.3V, $V_{INH}$ = 2.4V, $V_{INL}$ = 0.8V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.)

| PARAMETER | SYMBOL | CONDITIONS | | | MIN | TYP (Note 2) | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | | |
| Analog Signal Range | $V_{COM}$, $V_{NO}$, $V_{NC}$ | | | | 0 | | V+ | V |
| COM to NO or NC On-Resistance | $R_{ON}$ | $V_{COM\_}$ = 1.5V, $I_{COM}$ = 0.1mA | $T_A$ = +25°C | | | 100 | 400 | Ω |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | | 500 | |
| NO or NC Off Leakage Current (Notes 3, 4) | $I_{NO(OFF)}$, $I_{NC(OFF)}$ | $V_{COM\_}$ = ±1.5V, $V_{NO}$ or $V_{NC}$ = ∓1.5V, V+ = 3.3V, V- = -3.3V | $T_A$ = +25°C | | -1 | | 1 | nA |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | C, E | -10 | | 10 | |
| | | | | M | -100 | | 100 | |
| COM Off Leakage Current (Notes 3, 4) | $I_{COM(OFF)}$ | $V_{COM\_}$ = ±1.5V, $V_{NO}$ or $V_{NC}$ = ∓1.5V, V+ = 3.3V, V- = -3.3V | $T_A$ = +25°C | | -1 | | 1 | nA |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | C, E | -10 | | 10 | |
| | | | | M | -100 | | 100 | |
| COM On Leakage Current (Notes 3, 4) | $I_{COM(ON)}$ | $V_{NO}$ or $V_{NC}$ = ±1.5V, $V_{COM\_}$ = ±1.5V, V+ = 3.3V, V- = -3.3V | $T_A$ = +25°C | | -2 | | 2 | nA |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | C, E | -20 | | 20 | |
| | | | | M | -200 | | 200 | |
| **DIGITAL I/O** | | | | | | | | |
| IN Input Logic High | $V_{INH}$ | | | | 2.4 | | V+ | V |
| IN Input Logic Low | $V_{INL}$ | | | | V- | | 0.4 | V |
| IN Input Current Logic High or Low | $I_{IH}$, $I_{IL}$ | | | | -1 | 0.03 | 1 | µA |
| **POWER SUPPLY** | | | | | | | | |
| V+, V- Supply Current | I+, I- | IN = 0V or V+ | $T_A$ = +25°C | | -100 | 25 | 100 | µA |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | -175 | | 175 | |

**Note 2:** The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

**Note 4:** Guaranteed, not production tested.

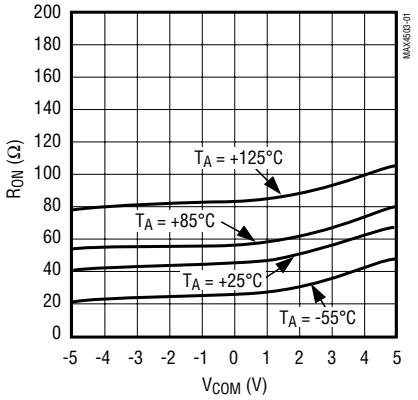
**Note 3:** Leakage parameters are 100% tested at maximum rated hot operating temperature, and guaranteed by correlation at +25°C.

**Note 5:** SOT packaged parts are 100% tested at +25°C. Limits at maximum and minimum rated temperature are guaranteed by design and correlation limits at +25°C.

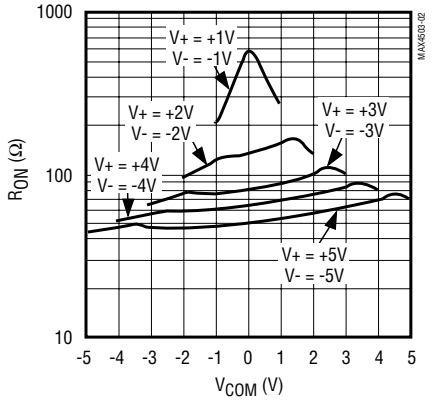
## Typical Operating Characteristics

(V+ = +5V, V- = -5V, $T_A$ = +25°C, unless otherwise noted.)

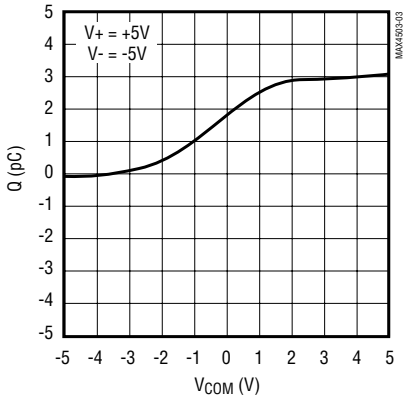
**ON-RESISTANCE vs. $V_{COM}$ AND TEMPERATURE**



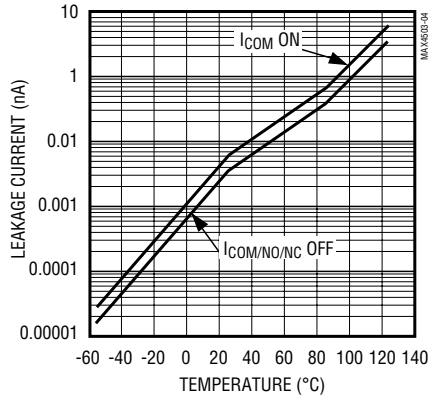

**ON-RESISTANCE vs. $V_{COM}$**



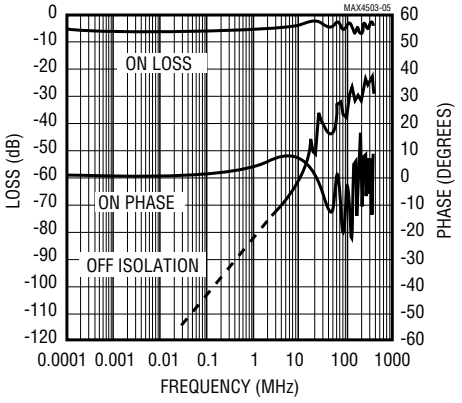

**CHARGE INJECTION vs. $V_{COM}$**



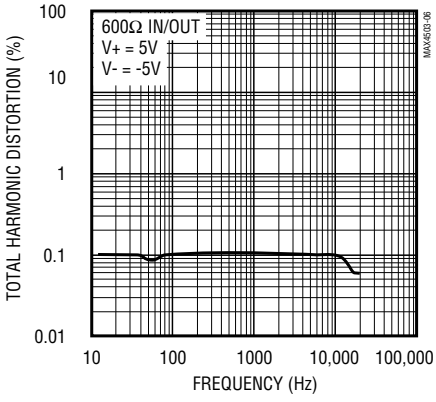

**LEAKAGE CURRENT vs. TEMPERATURE**



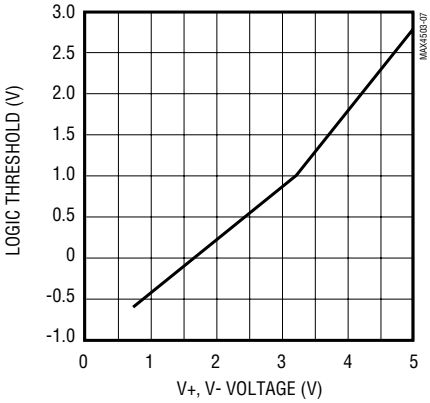

**FREQUENCY RESPONSE (50Ω IN AND OUT)**




**TOTAL HARMONIC DISTORTION vs. FREQUENCY**




**LOGIC THRESHOLD vs. V+ AND V-**



# Low-Voltage, Dual-Supply, SPST, CMOS Analog Switches

## Pin Description

| PIN | | | | NAME | FUNCTION |
|---|---|---|---|---|---|
| MAX4503 | | MAX4504 | | | |
| DIP/SO | SOT23-5 | DIP/SO | SOT23-5 | | |
| 1 | 1 | 1 | 1 | COM | Analog Switch Common Terminal |
| 2, 3, 5 | — | 2, 3, 5 | — | N.C. | No Connect (not internally connected) |
| 4 | 5 | 4 | 5 | V+ | Positive (analog and digital) Supply Voltage Input |
| 6 | 4 | 6 | 4 | IN | Digital Control Input |
| 7 | 3 | 7 | 3 | V- | Negative (analog) Supply Voltage Input |
| 8 | 2 | — | — | NO | Analog Switch Normally Open Terminal |
| — | — | 8 | 2 | NC | Analog Switch Normally Closed Terminal |

**Note:** NO, NC, and COM pins are identical and interchangeable. Either may be considered as an input or output; signals pass equally well in both directions.

## Applications Information

### Power-Supply Considerations

The MAX4503/MAX4504's construction is typical of most CMOS analog switches, except they have only two supply pins: V+ and V-. These voltages set the analog voltage limits of the switch. Reverse ESD-protection diodes are internally connected between IN and each analog signal pin and both V+ and V-. If any analog signal exceeds V+ or V-, one of these diodes will conduct. During normal operation, these (and other) reverse-biased ESD diodes leak, forming the only current drawn from V-. Additional current flows through V+ from the logic-level translator.

Virtually all the analog leakage current is provided through the ESD diodes. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or V- and the analog signal. This means their leakages will vary as the signal varies. The *difference* in the two diode leakages to the V+ and V- pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of either the same or opposite polarity.

There is no connection between the analog signal paths and V+ or V-.

V+ and V- also power the internal logic and logic-level translators. Since there is no ground pin, the logic input has a low-current pull-up to V+ and the logic limit is set by an internal comparator referenced to V+. The logic-level translators convert the logic levels to switched V+ and V- signals, to drive the gates of the analog signals. This drive signal is the only connection between the logic supplies (and signals) and the analog supplies. COM, NO, and NC pins have ESD-protection diodes to V+ and V-.

The logic is CMOS compatible when V+ is +5V. CMOS compatibility is maintained with all V+ values, assuming that the CMOS logic is operated from the same V+ supply. Since the MAX4503/MAX4504 have no ground pins, the logic levels are internally referenced to V+.

**Do not connect the MAX4503/MAX4504 V+ to +3V and connect the logic-level pins to TTL-logic-level signals. TTL levels can exceed +3V and violate the absolute maximum ratings, damaging the part and/or external circuits.**

### High-Frequency Performance

In 50Ω systems, signal response is reasonably flat up to 50MHz. (see *Typical Operating Characteristics*). Above 20MHz the on-response has several minor peaks which are highly layout dependent. The problem is not in turning the switch on, but in turning it off. The off-state switch acts like a capacitor, and passes higher frequencies with less attenuation. At 10MHz, off isolation is about -65dB in 50Ω systems, becoming worse (approximately 20dB per decade) as frequency increases. Higher circuit impedances also make off isolation worse.

## Test Circuits/Timing Diagrams

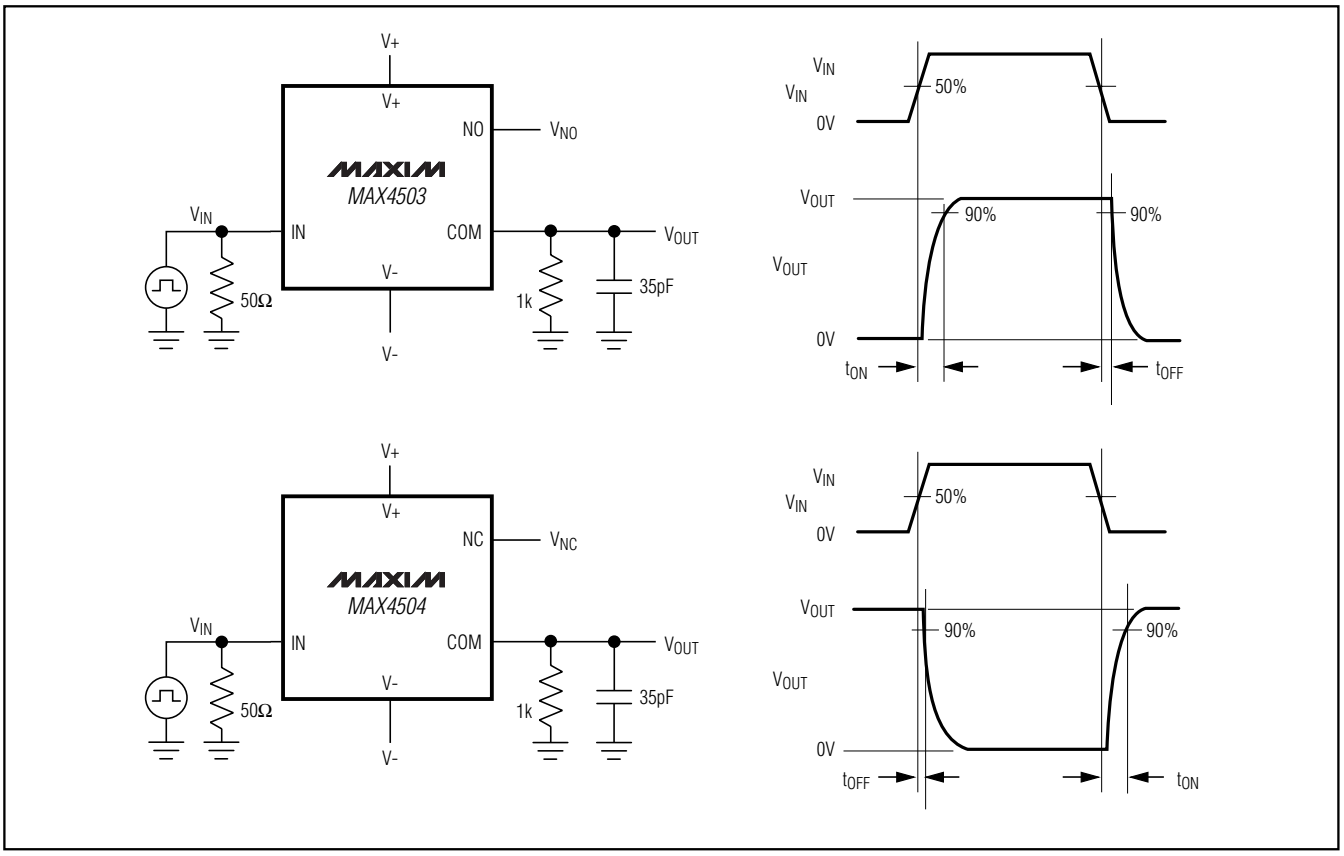



*Figure 1. Switching Times*

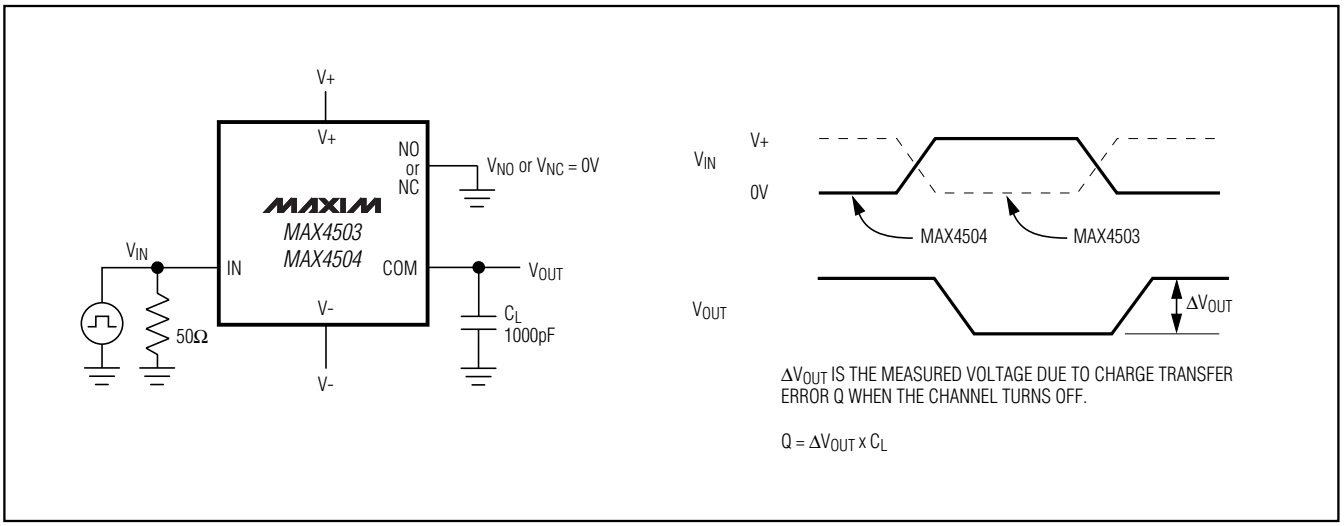



*Figure 2. Charge Injection*

# Low-Voltage, Dual-Supply, SPST, CMOS Analog Switches

## Test Circuits/Timing Diagrams (continued)

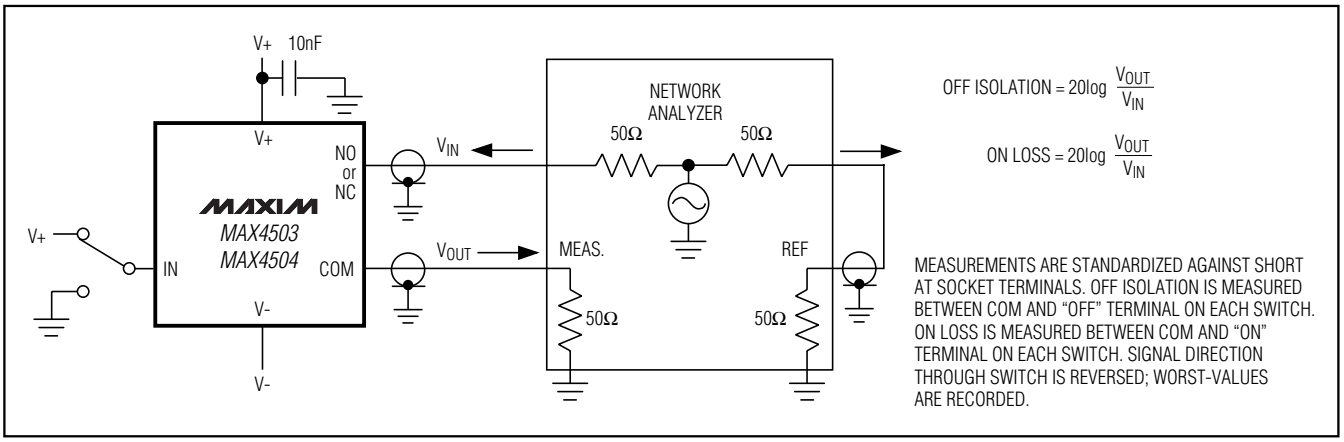



*Figure 3. Off Isolation and On Loss*

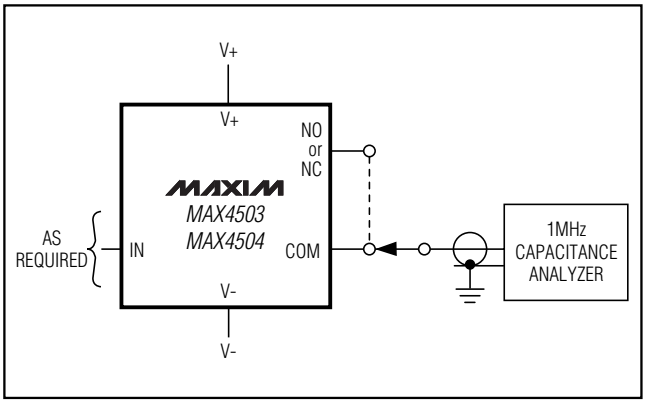


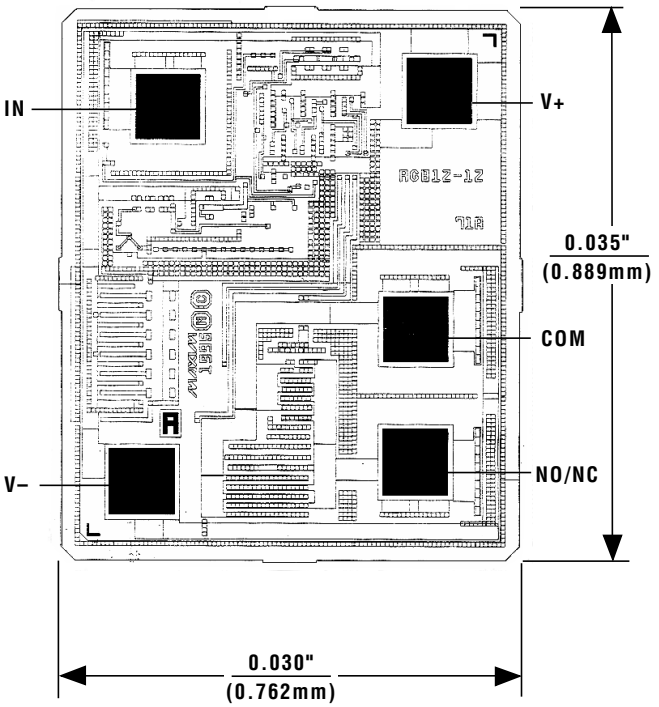

*Figure 4. NO, NC, and COM Capacitance*

## Ordering Information (continued)

| PART | TEMP. RANGE | PIN-PACKAGE |
|---|---|---|
| **MAX4504**CPA | 0°C to +70°C | 8 Plastic DIP |
| MAX4504CSA | 0°C to +70°C | 8 SO |
| MAX4504CUK | 0°C to +70°C | 5 SOT23-5 |
| MAX4504C/D | 0°C to +70°C | Dice* |
| MAX4504EPA | -40°C to +85°C | 8 Plastic DIP |
| MAX4504ESA | -40°C to +85°C | 8 SO |
| MAX4504EUK | -40°C to +85°C | 5 SOT23-5 |
| MAX4504MJA | -55°C to +125°C | 8 CERDIP** |

**Contact factory for dice specifications.*
***Contact factory for availability.*

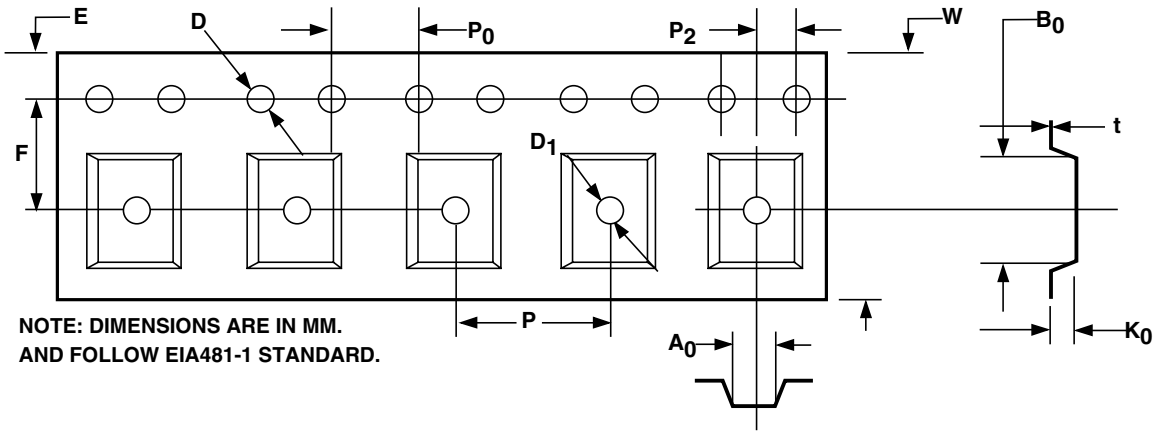
## Chip Topography




TRANSISTOR COUNT: 36

SUBSTRATE IS INTERNALLY CONNECTED TO V+

## Tape-and-Reel Information




NOTE: DIMENSIONS ARE IN MM.
AND FOLLOW EIA481-1 STANDARD.

| | | |
|---|---|---|
| $A_0$ | 3.200 | ±0.102 |
| $B_0$ | 3.099 | ±0.102 |
| D | 1.499 | +0.102 +0.000 |
| $D_1$ | 0.991 | +0.254 +0.000 |

| | | |
|---|---|---|
| E | 1.753 | ±0.102 |
| F | 3.505 | ±0.051 |
| $K_0$ | 1.397 | ±0.102 |
| P | 3.988 | ±0.102 |

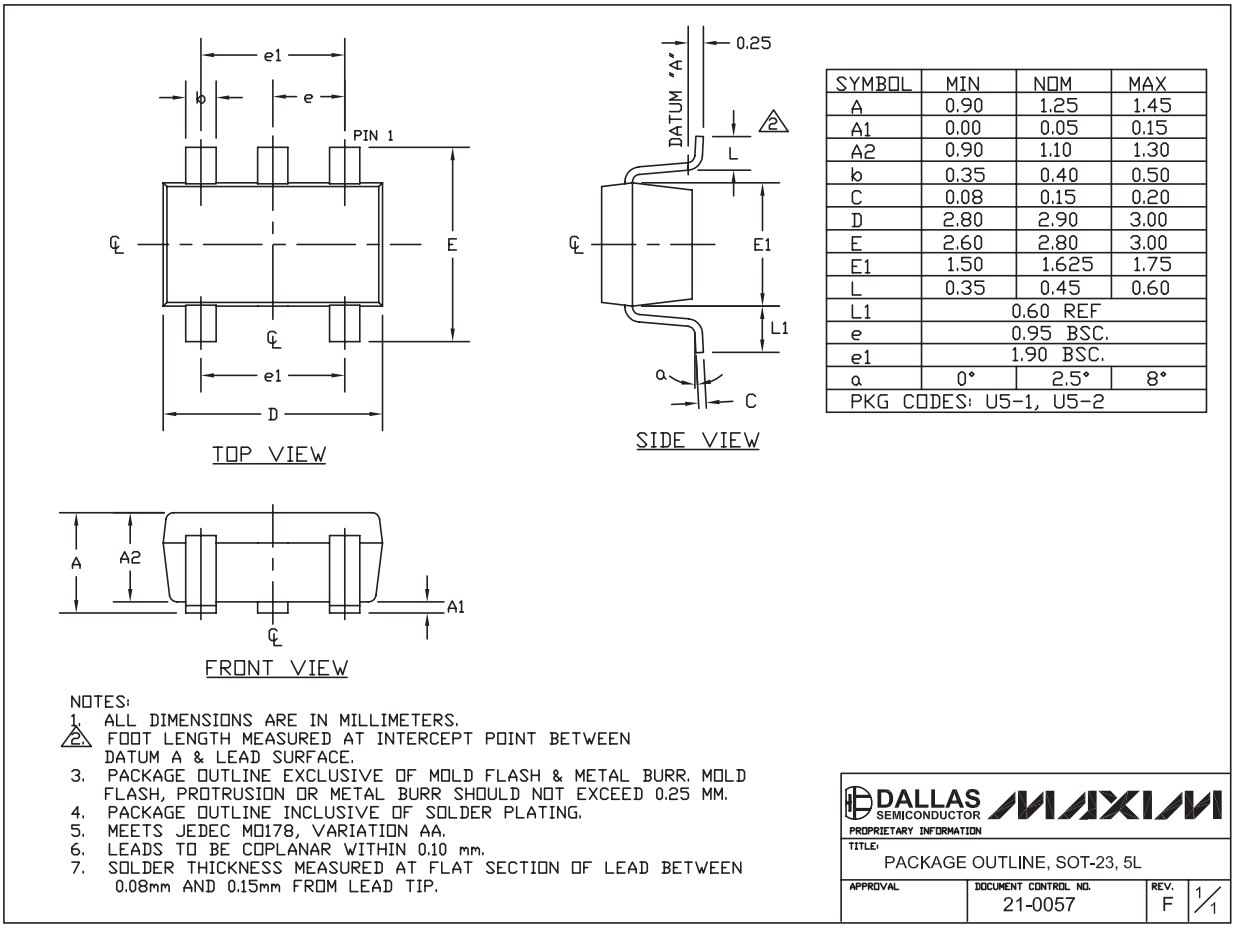
| | | |
|---|---|---|
| $P_0$ | 3.988 | ±0.102 |
| $P_0$10 | 40.005 | ±0.203 |
| $P_2$ | 2.007 | ±0.051 |
| t | 0.254 | ±0.127 |
| W | 8.001 | +0.305 -0.102 |

5 SOT23-5

# Low-Voltage, Dual-Supply, SPST, CMOS Analog Switches

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



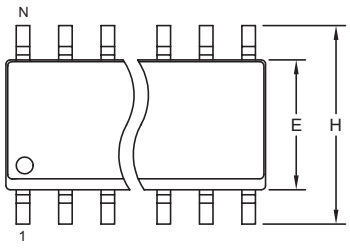

| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 0.90 | 1.25 | 1.45 |
| A1 | 0.00 | 0.05 | 0.15 |
| A2 | 0.90 | 1.10 | 1.30 |
| b | 0.35 | 0.40 | 0.50 |
| C | 0.08 | 0.15 | 0.20 |
| D | 2.80 | 2.90 | 3.00 |
| E | 2.60 | 2.80 | 3.00 |
| E1 | 1.50 | 1.625 | 1.75 |
| L | 0.35 | 0.45 | 0.60 |
| L1 | 0.60 REF | | |
| e | 0.95 BSC. | | |
| e1 | 1.90 BSC. | | |
| α | 0° | 2.5° | 8° |
| PKG CODES: U5-1, U5-2 | | | |

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

SOICN .EPS

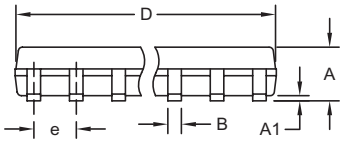
| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.053 | 0.069 | 1.35 | 1.75 |
| A1 | 0.004 | 0.010 | 0.10 | 0.25 |
| B | 0.014 | 0.019 | 0.35 | 0.49 |
| C | 0.007 | 0.010 | 0.19 | 0.25 |
| e | 0.050 BSC | | 1.27 BSC | |
| E | 0.150 | 0.157 | 3.80 | 4.00 |
| H | 0.228 | 0.244 | 5.80 | 6.20 |
| L | 0.016 | 0.050 | 0.40 | 1.27 |



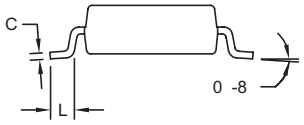

TOP VIEW

VARIATIONS:

| | INCHES | | MILLIMETERS | | | |
|---|---|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX | N | MS012 |
| D | 0.189 | 0.197 | 4.80 | 5.00 | 8 | AA |
| D | 0.337 | 0.344 | 8.55 | 8.75 | 14 | AB |
| D | 0.386 | 0.394 | 9.80 | 10.00 | 16 | AC |




FRONT VIEW




SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, .150" SOIC

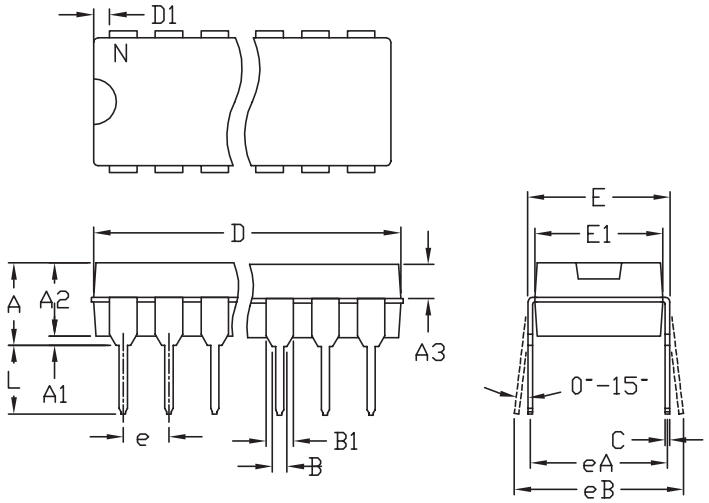
| APPROVAL | DOCUMENT CONTROL NO. | REV. | |
|---|---|---|---|
| | 21-0041 | B | 1/1 |

# Low-Voltage, Dual-Supply, SPST, CMOS Analog Switches

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

PDIPN.EPS




| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | --- | 0.180 | --- | 4.572 |
| A1 | 0.015 | --- | 0.38 | --- |
| A2 | 0.125 | 0.175 | 3.18 | 4.45 |
| A3 | 0.055 | 0.080 | 1.40 | 2.03 |
| B | 0.015 | 0.022 | 0.381 | 0.56 |
| B1 | 0.045 | 0.065 | 1.14 | 1.65 |
| C | 0.008 | 0.014 | 0.2 | 0.355 |
| D1 | 0.005 | 0.080 | 0.13 | 2.03 |
| E | 0.300 | 0.325 | 7.62 | 8.26 |
| E1 | 0.240 | 0.310 | 6.10 | 7.87 |
| e | 0.100 BSC. | | 2.54 BSC. | |
| eA | 0.300 BSC. | | 7.62 BSC. | |
| eB | 0.400 BSC. | | 10.16 BSC. | |
| L | 0.115 | 0.150 | 2.921 | 3.81 |

| | INCHES | | MILLIMETERS | | | |
|---|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | N | MS001 |
| D | 0.348 | 0.390 | 8.84 | 9.91 | 8 | AB |
| D | 0.735 | 0.765 | 18.67 | 19.43 | 14 | AC |
| D | 0.745 | 0.765 | 18.92 | 19.43 | 16 | AA |
| D | 0.885 | 0.915 | 22.48 | 23.24 | 18 | AD |
| D | 1.015 | 1.045 | 25.78 | 26.54 | 20 | AE |
| D | 1.14 | 1.265 | 28.96 | 32.13 | 24 | AF |
| D | 1.360 | 1.380 | 34.54 | 35.05 | 28 | *5 |

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
5. SIMILIAR TO JEDEC MO-058AB
6. N = NUMBER OF PINS

MAXIM — 120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194 PROPRIETARY INFORMATION

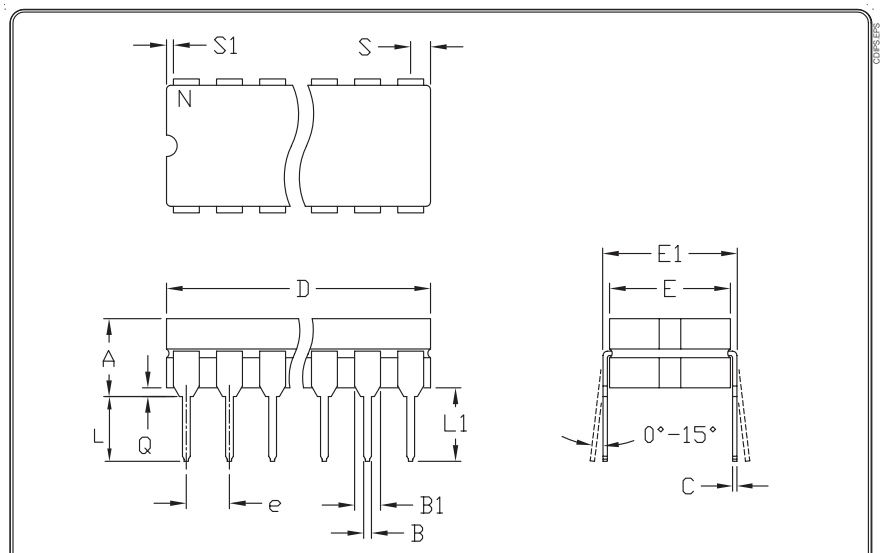
TITLE: PACKAGE FAMILY OUTLINE: PDIP .300"

1/1

21-0043 D — DOCUMENT CONTROL NUMBER — REV

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)




| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | --- | 0.200 | --- | 5.08 |
| B | 0.014 | 0.023 | 0.36 | 0.58 |
| B1 | 0.038 | 0.065 | 0.97 | 1.65 |
| C | 0.008 | 0.015 | 0.20 | 0.38 |
| E | 0.220 | 0.310 | 5.59 | 7.87 |
| E1 | 0.290 | 0.320 | 7.37 | 8.13 |
| e | 0.100 | | 2.54 | |
| L | 0.125 | 0.200 | 3.18 | 5.08 |
| L1 | 0.150 | --- | 0.00 | --- |
| Q | 0.015 | 0.070 | 0.38 | 1.78 |
| S | --- | 0.098 | --- | 2.49 |
| S1 | 0.005 | --- | 0.13 | --- |

| | INCHES | | MILLIMETERS | | | |
|---|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | N | CASE |
| D | --- | 0.405 | --- | 10.29 | 8 | P:D4 |
| D | --- | 0.785 | --- | 19.94 | 14 | C:D1 |
| D | --- | 0.840 | --- | 21.34 | 16 | E:D2 |
| D | --- | 0.960 | --- | 24.38 | 18 | V:D6 |
| D | --- | 1.060 | --- | 26.92 | 20 | R:D8 |
| D | --- | 1.280 | --- | 32.51 | 24 | L:D9 |

NOTES:
1. CONTROLLING DIMENSION: INCH
2. MEETS 1835 CASE OUTLINE CONFIGURATION #1 AS SHOWN IN ABOVE TABLE
3. N = NUMBER OF PINS

MAXIM 120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194
PROPRIETARY INFORMATION

PACKAGE FAMILY OUTLINE: CDIP .300"
TITLE

1/1

21-0045 A
DOCUMENT CONTROL NUMBER REV

## Revision History

Changes made at Rev 1: 1, 4, 10, 11, 12

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Maxim Integrated:

MAX4503CUK+T MAX4503EUK+T MAX4504CSA+ MAX4504CSA+T MAX4504CUK+T MAX4504EUK+T