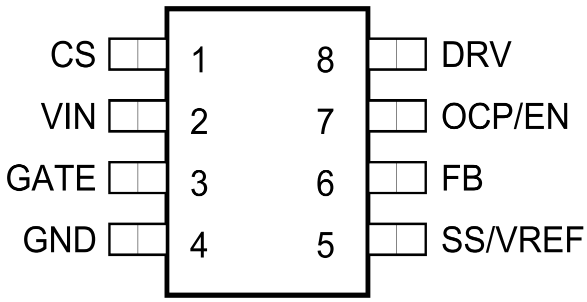
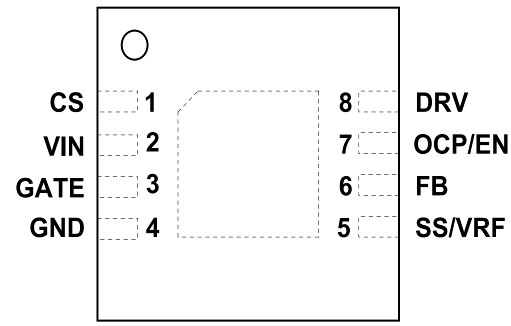
Pin Configuration, MSOP-8

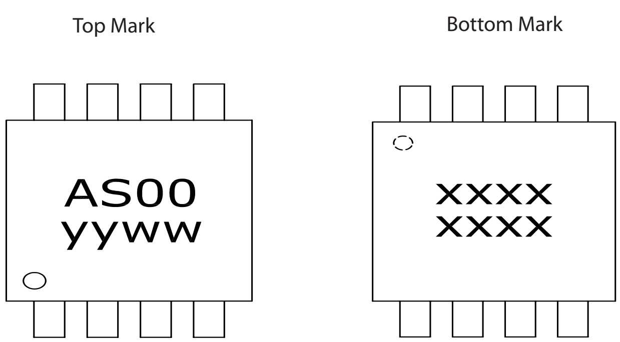


Pin Configuration, MLPD-UT8



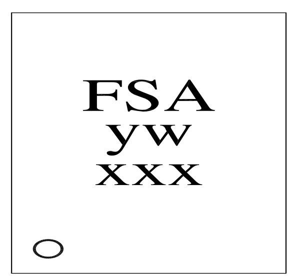
2mm x 3mm x 0.6mm MLPD-UT8

Marking Information, MSOP-8



nnnn=Part Number Code (Example AS00)- Reference Part No. Code for MSOP
yyww=Date Code (Example: 0752)
xxxx = Semtech Lot No. (Example: E901)
xxxx = Semtech Lot No. (Example: 01-1)

Marking Information, MLPD-UT8



nnn=Part Number (Example FSA) - Reference Part No. Code for small MLP
yw =Datecode (Reference Package Marking Design Guide lines, Appendix A)
xxx = Semtech Lot No. (Example: 901)

Ordering Information

Device	Package
SC2604MSTRT(1)(2)	MSOP-8
SC2604ULTRT(1)(2)	2mm x 3mm x 0.6mm MLPD-UT8
SC2604EVB-1	Evaluation Board, MSOP-8
SC2604EVB-2	Evaluation Board, MLPD-8

Notes:
(1) Available in tape and reel only. A reel contains 2,500 devices.
(2) Available in lead-free package only. Device is Pb Free, Halogen Free, and WEEE/RoHS compliant.

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Absolute Maximum Ratings

V_{IN} Supply Voltage .... -0.3 to 20V

CS Pin Voltage...-0.3 to 20V

GATE Pin Voltage.......................................-0.3 to 20V

DRV Pin Voltage ....-0.3 to 25V

OCP/EN Pin Voltage ....-0.3 to 7V

SS/VREF Pin Voltage ....-0.3 to 7V

FB Pin Voltage ....-0.3 to 7V

Peak IR Reflow Temperature .... 260°C

ESD Protection Level[(2)] 2000V

Thermal Information

Thermal Resistance, Junction to Ambient[(1)]

MSOP-8 .... 160 °C/W

MLPD-UT8............................... 50 °C/W

Maximum Junction Temperature .... 15 0°C

Storage Temperature Range ....-45 to +150 °C

Lead Temperature (Soldering) 10 sec .... 300 °C

Recommended Operating Conditions

Input Voltage Range .... 4.5V to 16V

Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

NOTES-

(1) Calculated from package in still air, mounted to 3" x 4.5", 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

(2) Tested according to JEDEC standard JESD22-A114-B.

Electrical Characteristics

Unless otherwise noted, V_{IN} = 12V, V_O = 25V, -40°C < T_A = T_J < 125°C.

Parameter	Conditions	Min	Typ	Max	Units
Input Supply					
V_{IN} Supply Voltage		4.5		16	V
V_{IN} Start Voltage	V_{IN} Rising		4.2	4.5	V
V_{IN} Start Hysteresis			400		mV
V_{IN} Supply Current	Switching, GATE pin floating		6.0	9.0	mA
V_{IN} Shutdown Current	OCP/EN = Low			200	µA
Error Amplifier					
Feedback Voltage	I_O = 100mA	1.225	1.250	1.275	V
Feedback Bias Current	V_{IN} = 12V, V_{FB} = $V_{SS/VREF}$		0.5	1.0	µA
Error Amplifier Gain [(1)]			90		V/V
Oscillator					
Oscillator Frequency		320	400	480	kHz
Maximum Duty Cycle		86	90		%
Internal Ramp Peak [(2)]			1.4		V
Internal Ramp Valley [(2)]			0.4		V
Regulation					
Load Regulation	I_O = 0.1A to 1A			0.5	%
Line Regulation	V_{IN} = 5V to 16V, I_O = 0.1A			0.125	%/V
	V_{IN} = 5V to 16V, I_O = 0.1A, T_J = 25°C		0.065		

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Electrical Characteristics (Cont.)

Unless otherwise noted, V_{IN} = 12V, V_O = 25V, -40°C < T_A = T_J < 125°C.

Parameter	Conditions	Min	Typ	Max	Units
PWM Switch Gate Drive					
Gate Source Current	V_{IN} = 12V, C_{GATE} = 10nF	0.5	0.8		A
Gate Sink Current	V_{IN} = 12V, C_{GATE} = 10nF	0.5	0.8		A
PWM Switch Soft Start					
Soft Start Charge Current			55		µA
SS/VREF Threshold to Shutdown Switch	Pull down below this level to disable PWM Switch gate			100	mV
SS/VREF Threshold to Turn-on Switch	Pull above this level to enable PWM Switch gate	310			mV
Disconnect Switch Gate Drive					
DRV Source Current	V_{IN} = 12V, V_{DRV} = 15.5V		45		µA
DRV Sink Current	V_{IN} = 12V, V_{DRV} = 8V		45		µA
Charge Pump Voltage	V_{IN} = 5V	2.15			V
	V_{IN} = 12V	4.3		5.8	V
Over Current Protection					
Current Limit Threshold	V_{IN} - CS	61	72	83	mV
OCP/EN Threshold	Pull down below this level to disable Disconnect FET gate	520	590	660	mV
OCP/EN Charge Current			37		µA
OCP/EN Discharge Current			1.0		µA
CS Input Current			0.2		µA

Note: (1). Guaranteed by Characterization
(2). Guaranteed by design

Pin Descriptions

Pin	Pin Name	Pin Function
1	CS	Current sense input (negative)
2	VIN	Device supply voltage (also positive current sense input)
3	GATE	PWM gate driver output for boost converter. This pin swings from 0V to V_{IN}.
4	GND	Device ground
5	SS/VREF	Soft start and reference voltage pin
6	FB	Error amplifier inverted input
7	OCP/EN	When a capacitor is tied to this pin, the maximum inrush current is controlled during start-up. The capacitor value also determines the off-time after the device has entered hiccup mode. Pulling this pin low can disable the linear and the switcher to turn off the circuit.
8	DRV	Gate drive of input disconnect FET limiting system input current
	Thermal Pad	Pad for heatsinking purposes. Connect to ground plane using multiple vias. Not connected internally.

Block Diagram

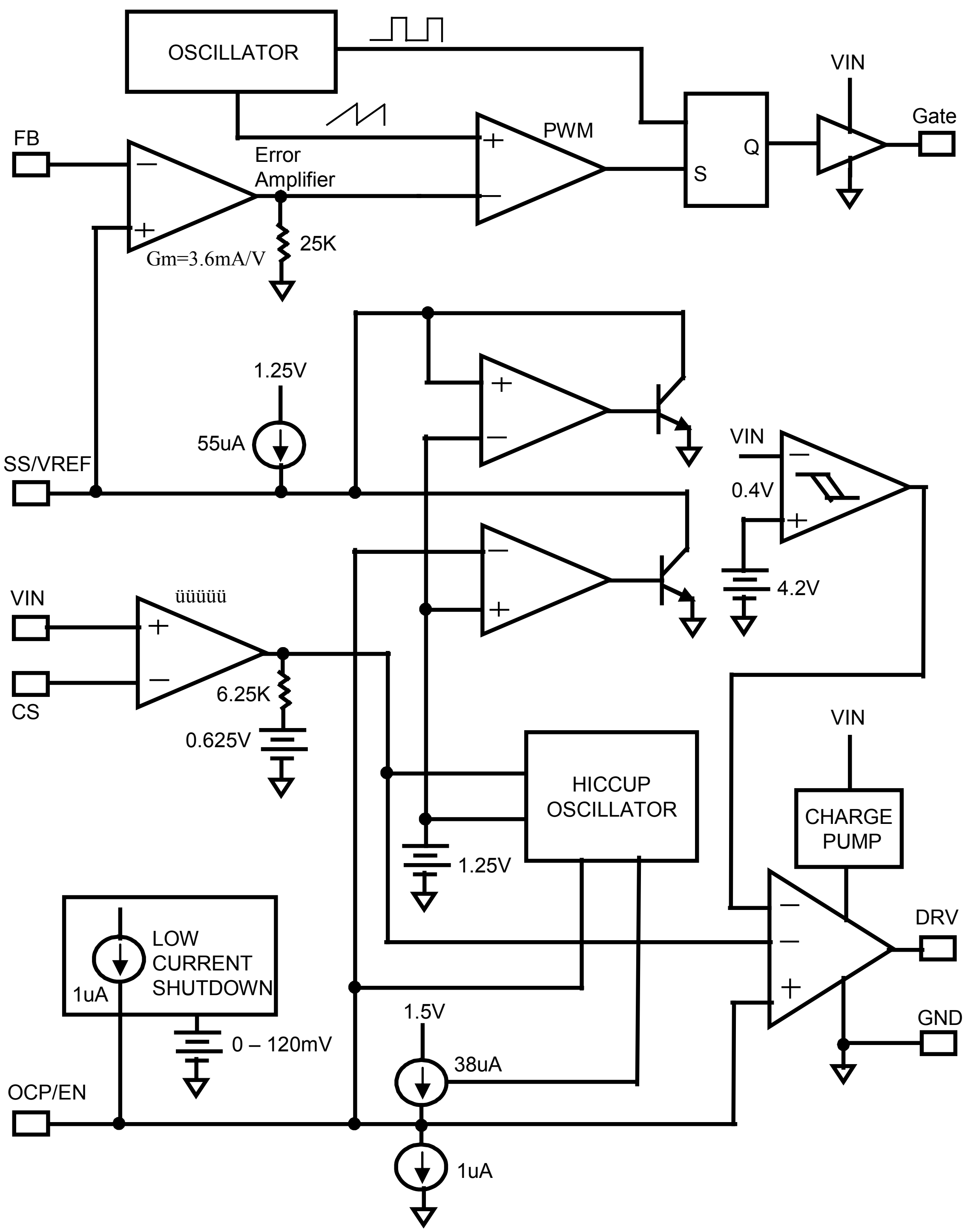
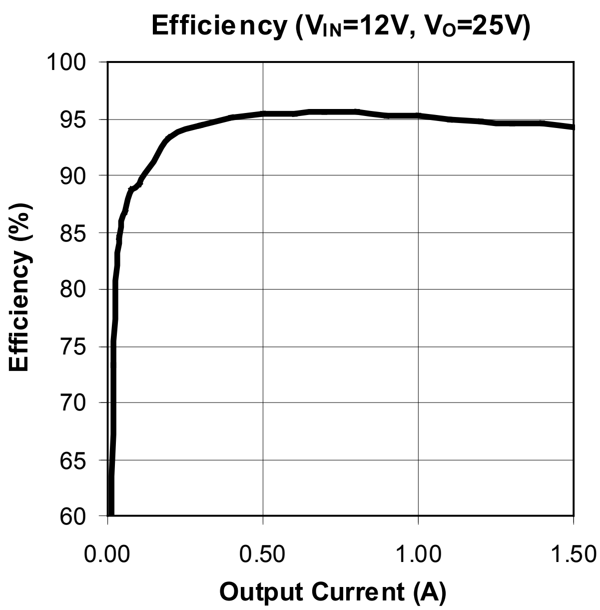
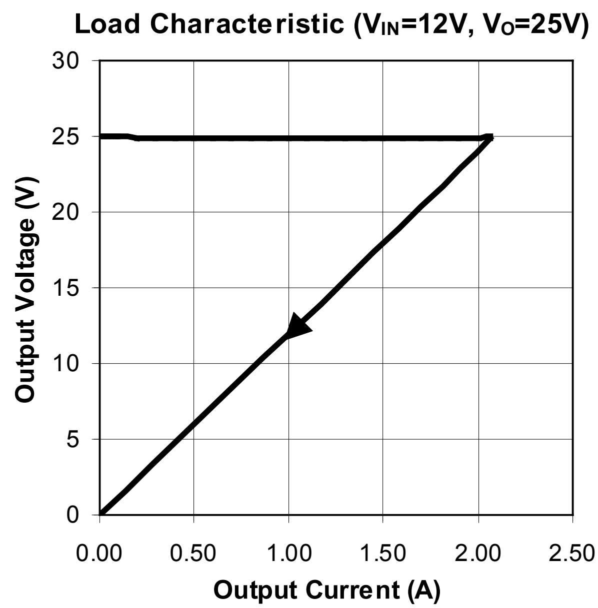
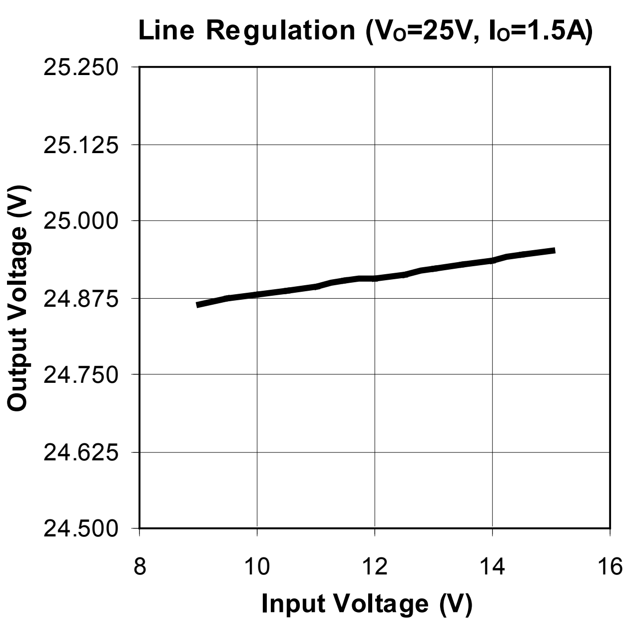


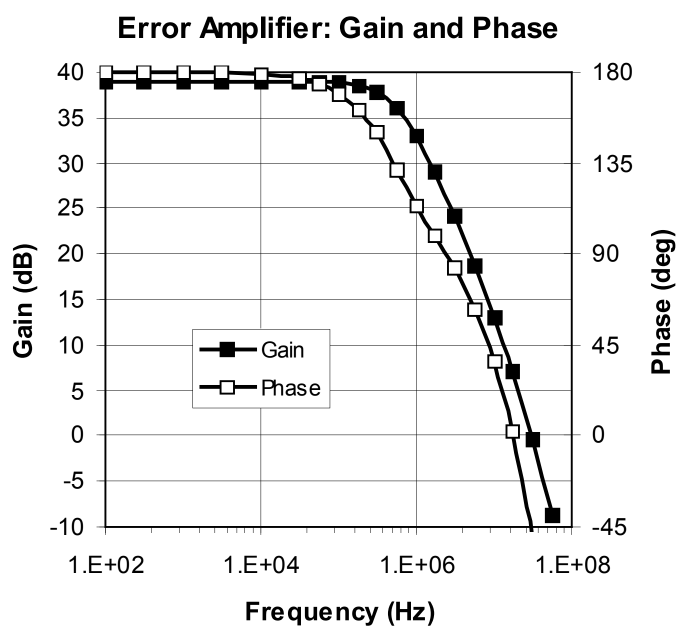
Figure 2. SC2604 Function Diagram

Typical Characteristics



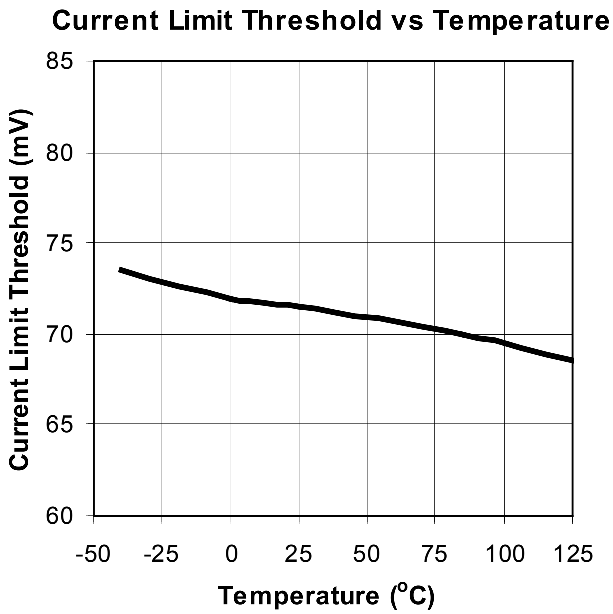


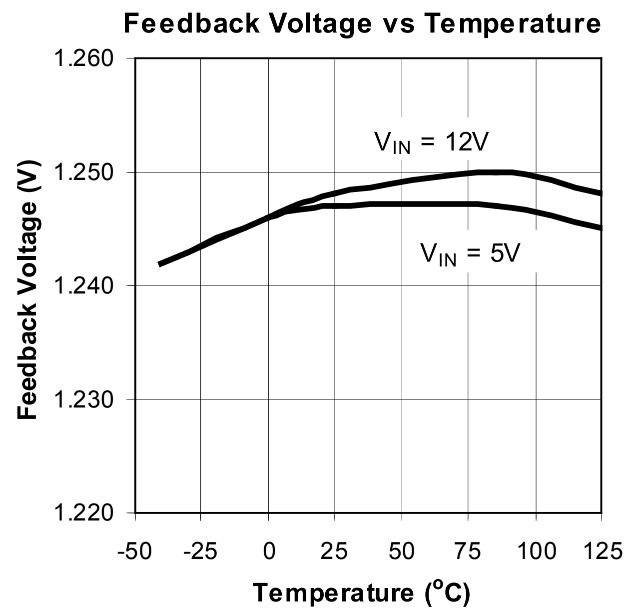


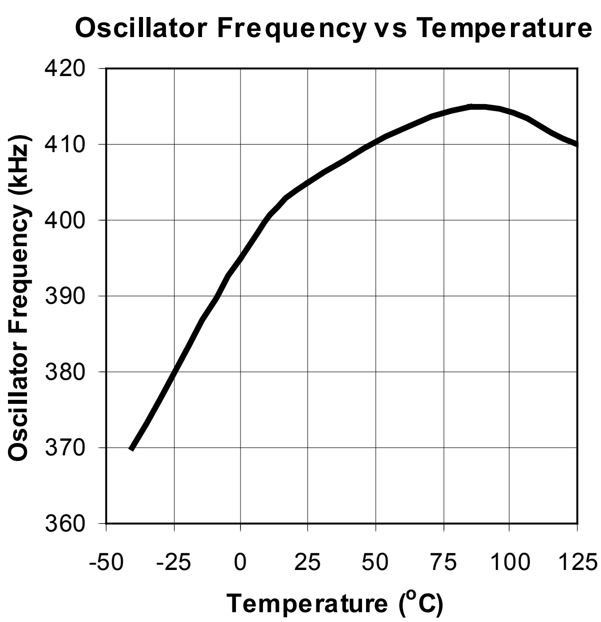


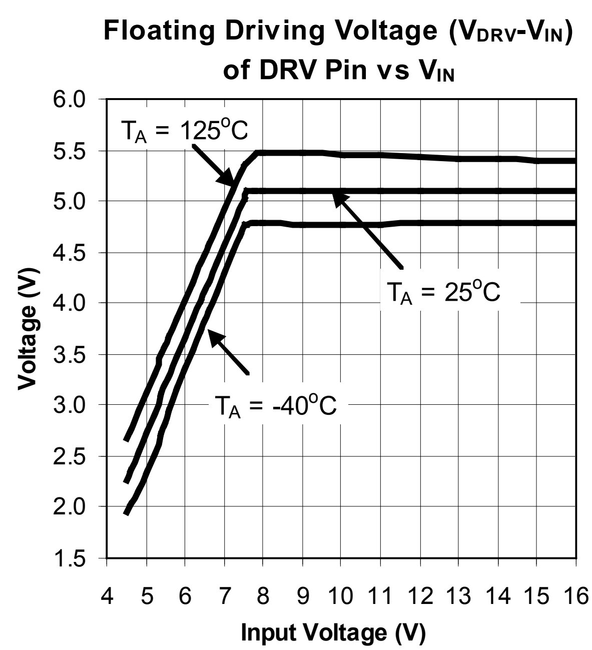
Simulation

Typical Characteristics (Cont.)









Applications Information

PWM Control Loop

The SC2604 is a voltage-mode PWM controller with a fixed switching frequency of 400kHz for use in high efficiency, boosted voltage, DC/DC power supplies.

As shown in Figure 2, the PWM control loop of the SC2604 consists of a 400kHz oscillator, a PWM comparator, a voltage error amplifier, and a FET driver. The boost converter output voltage is fed back to FB (error amplifier negative) and is regulated to the reference voltage at SS/VREF pin. The error amplifier output is compared with the 400kHz ramp to generate a PWM wave, which is amplified and used to drive the boost FET (Q_2 in Figure 1) for the converter. The PWM controller works with soft start and fault monitoring circuitry to meet application requirements.

UVLO, Start-up, and Shutdown

To initiate the SC2604, a supply voltage is applied to V_{IN}. The DRV and GATE are held low. When V_{IN} voltage exceeds UVLO (Under Voltage Lockout) threshold, typically 4.2V, an internal current source (37µA) begins to charge the OCP/EN pin capacitor. The OCP/EN voltage ramps from near ground to over 1.25V but the voltage between 0.625V and 1.25V provides the linear soft-start range for the disconnect FET (Q_1). When the OCP/EN voltage is over 1.25V, the OCP hiccup is enabled, and SS/VREF pin is released. At this moment, another internal current source (55µA) begins to charge the SS/VREF pin capacitor. When the SS/VREF pin voltage reaches 0.5V, the error amplifier output will rise to 0.4V, then the PWM comparator begins to switch. The switching regulator output is slowly ramping up for a soft turn-on. The details of SC2604 start-up timing is shown in Figure 3.

If the supply voltage at V_{IN} pin falls below UVLO threshold (3.8V typically) during a normal operation, the DRV pin is pulled low to cut off the supply power of the boost converter, while the OCP/EN pin capacitor is discharged with a 1µA internal current source. When the OCP/EN pin falls below 1.25V, the SS/VREF pin is forced to ground. This completely shuts down the boost conveter.

Directly pulling the OCP/EN pin below 0.52V can also allow a complete shutdown of the output. Pulling the SS/VREF pin below 0.1V only shuts the boost FET (Q_2 in Figure 1) off and the output voltage will be (V_{IN}-V_d).

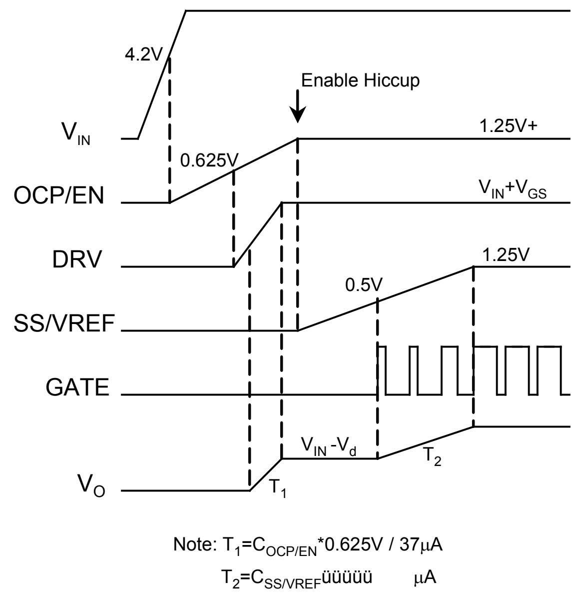


Figure 3. Start-up Timing Diagram

Hiccup Mode Short Circuit Protection

Hiccup mode over-current protection is utilized in the SC2604. When an increasing load causes a voltage of 72mv to occur from V_{IN} to CS then a current limit hiccup sequence is started. The sequence starts by pulling DRV low and discharging the OCP/EN pin with a 1µA current source. When the OCP/EN pin falls below 1.25V, the SS/VREF pin is forced to ground (similar to the UVLO shutdown described in the last setion).

When the voltage on the OCP/EN pin falls to near zero volt, the 1µA discharge current becomes a 37µA charging current and the OCP/EN pin starts to charge and DRV is enabled. When the OCP/EN voltage rises from 0.625V to 1.25V, the current in the disconnect FET is allowed to increase from zero to a maximum of 72mV/(Current Sense Resistor Value). If the over-current condition still exists when OCP/EN crosses 1.25V then the hiccup sequence will re-start. If there is no over-current as OCP/EN crosses 1.25V then the SS/VREF pin is released to rise and allow a

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Applications Information (Cont.)

soft-start of the switching boost regulator.

The DRV pin of the SC2604 is meant to drive an N-Channel FET that can disconnect the input supply in the event of an over-current condition. The OCP/EN capacitor becomes part of a hiccup oscillator that is charged with 37µA and discharged with 1µA to provide a low duty cycle for the FET Q_1.

It should be understood that sufficiently fast ramp rates on the OCP/EN pin and the SS/VREF pin can trigger a hiccup event because of the charging current demanded by the boost regulator output capacitor.

Setting the Output Voltage

In Figure 1, an external resistive divider R_3 and R_5 with its center tap tied to the FB pin sets the output voltage.

$$R_3 = R_5\left(\frac{V_{OUT}}{1.25V} - 1\right)$$

In some applications, a RC branch (R_6, C_{12} in the Typical Schematic on page 12) will be needed for loop stability.

Maximum Duty Cycle

The maximum duty cycle, D_{max} defines the upper limit of power conversion ratio

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1 - D_{MAX}}$$

Calculating Current Sense Resistor

Current sense resistor is placed at the input to sense inductor peak current of the boost regulator. The value of the resistor can be calculated by

$$R_{CS} = \frac{72mV}{I_{PEAK}}$$

where I_{PEAK} is the allowed boost inductor peak current.

In many applications, a noise filter circuit (R_1=200, C_{10}=10nF in the Typical Schematic on page 12) may be needed for the input current sensing.

Capacitor at OCP/EN Pin - $C_{OCP/EN}$

As the current at start-up may hit its current limit threshold, the ramp rate of the current must be slow enough to allow the output capacitor to be fully charged to a voltage one diode drop V_d less than input voltage V_{IN}. To guarantee a successful start-up at no load, the value of the capacitor at the OCP/EN pin has to satisfy the following formula:

$$C_{OCP/EN} > \frac{C_{OUT}(V_{IN} - V_d)}{0.625}\frac{R_{CS}}{750}$$

Disconnect FET Selection

The floating driving voltage of DRV pin drops slightly as the supply voltage V_{IN} is below 7.5V (Typical Characteristics on page 8), where a FET with low gate threshold voltage ($V_{GS(TH)}$) has to be used for the disconnect FET. In a 5V input application, a FET with $V_{GS(TH)}$=2V, such as FDD6672A from Fairchild, is needed.

Layout Guidelines

Careful attentions to layout requirements are necessary for successful implementation of the SC2604 PWM controller. High currents switching at 400kHz are present in the application and their effect on ground plane voltage differentials must be understood and minimized.

1) The high power parts of the circuit should be laid out first. A ground plane should be used, the number and position of ground plane interruptions should be such as to not unnecessarily compromise ground plane integrity. Isolated or semi-isolated areas of the ground plane may be deliberately introduced to constrain ground currents to particular areas, for example the input capacitor and bottom Schottky ground.

2) The loop formed by the output Capacitor(s) (C_{OUT}), the FET (Q_1), the current sensing resistor, and the Schottky (D_1) must be kept as small as possible, as shown on the layout diagram in Figure 4. This loop contains all the high current, fast transition switching. Connections should be as wide and as short as possible to minimize loop inductance. Minimizing this loop area will reduce EMI,

Applications Information (Cont.)

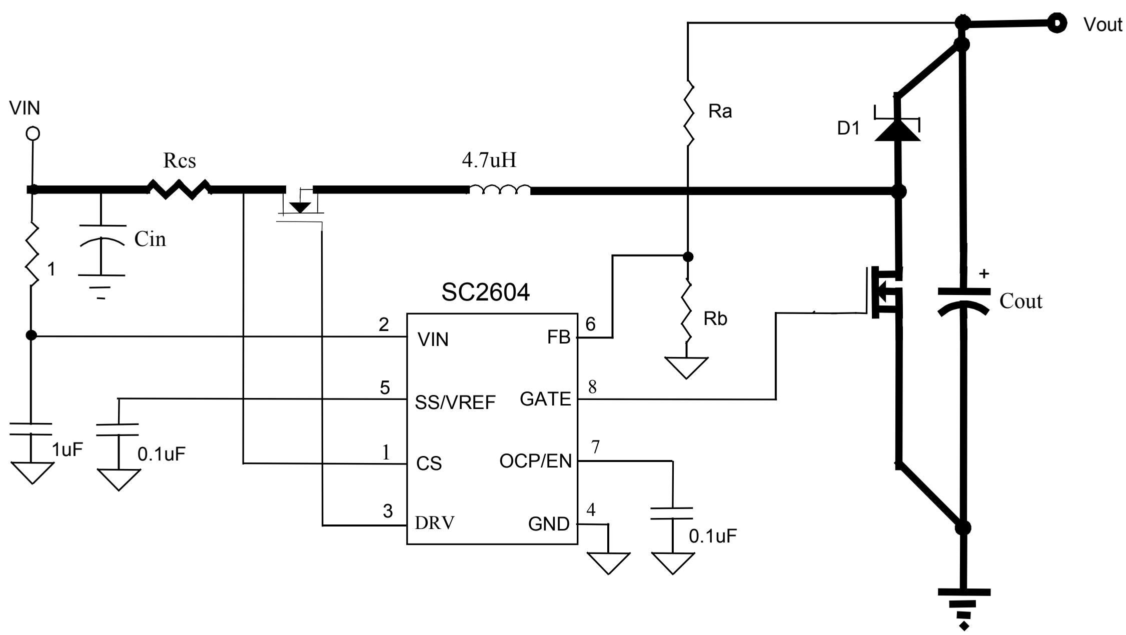
lower ground injection currents, resulting in electrically "cleaner" grounds for the rest of the system and minimize source ringing, resulting in more reliable gate switching signals.

3) The connection between the junction of Q_1, D_1 and the output capacitor should be a wide trace or copper region. It should be as short as practical. Since this connection has fast voltage transitions, keeping this connection short will minimize EMI.

4) The Output Capacitor(s) (C_{OUT}) should be located as close to the load as possible, fast transient load currents are supplied by C_{OUT} only, and connections between C_{OUT} and the load must be short, wide copper areas to minimize inductance and resistance.

5) The SC2604 is best placed over an isolated ground plane area. The soft-start capacitor and the Vin decoupling capacitor should also connected to this ground pad area. This isolated ground area should be connected to the main ground by a trace that runs from the GND pin to the ground side of the output capacitor. If this is not possible, the GND pin may be connected to the ground path between the Output Capacitor and the C_{IN}, Q_1, D_1 loop. Under no circumstances should GND be returned to a ground inside the C_{IN}, Q_1, D_1 loop.

6) Input voltage of the SC2604 should be supplied from the power rail through a 1Ω resistor, the Vin pin should be decoupled directly to GND by a 0.1µF~1µF ceramic capacitor, trace lengths should be as short as possible.

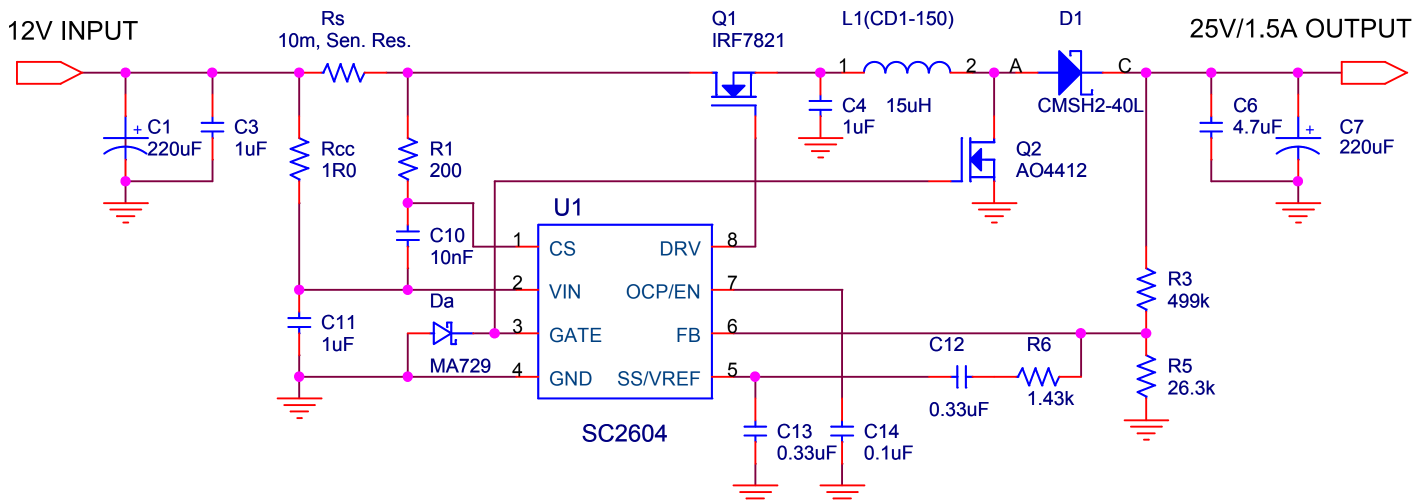


Note: Heavy lines indicate the critical loop carrying high pulsating current.
The inductance of the loop needs to be minimized.

Figure 4. SC2604 Layout Diagram

Applications Information (Cont.)

Typical application schematic with 12V input and 25V/1.5A output



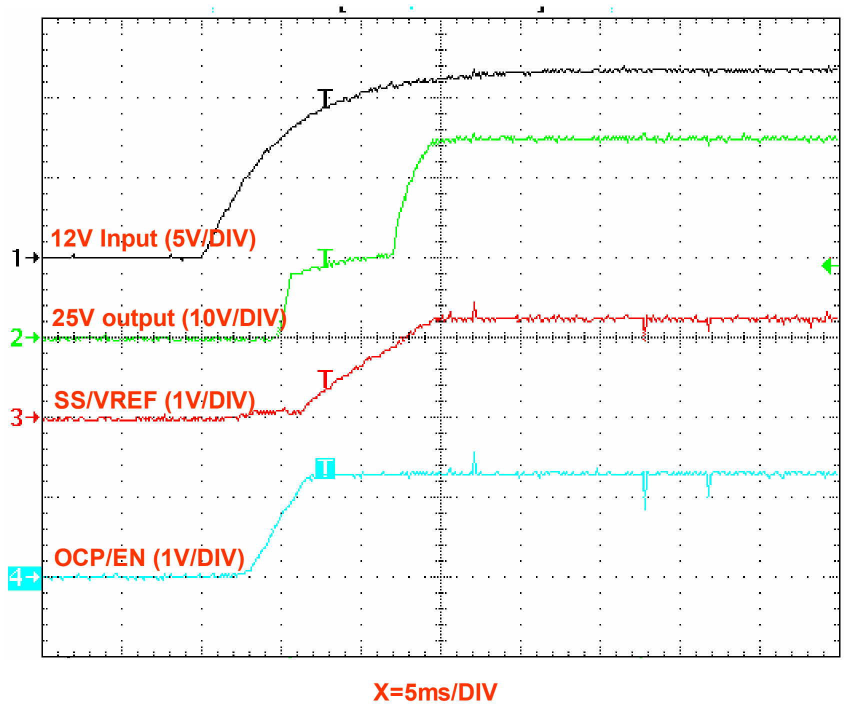
Note: A small Schottky diode (Da) may be required in some applications to clamp negative spike at the GATE pin.

Bill of materials

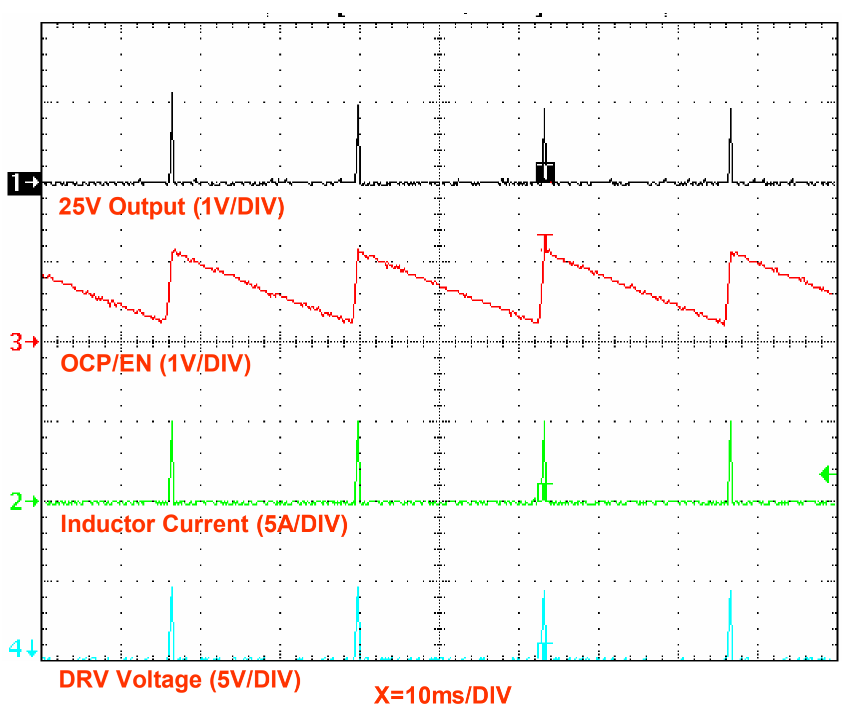
Item	Quantity	Reference	Part (P/N of Vender)	Vendor
1	1	C1	220uF/10V	Rubycon, ZL
2	3	C3,C4,C11	1uF/16V	Vishay
3	1	C6	4.7uF/50V	Murata
4	1	C7	220uF/35V/160m	Rubycon, YXF
5	1	C10	10nF	Vishay
6	1	C12	0.33uF	Vishay
7	1	C13	0.33uF	Vishay
8	1	C14	0.1uF	Vishay
9	1	D1	CMSH2-40L (Schottky diode)	Central Semi
10	1	Da	MA729 (Schottky diode)	Panasonic
11	1	L1	15uH/3.5A (CD1-150)	Coiltronics
12	1	Q1	IRF7821	IR
13	1	Q2	AO4412	Alpha & Omega Semi.
14	1	Rs	15m(Sensing Res.)	Vishay
15	1	R1	200	Vishay
16	1	Rcc	1R0	Vishay
17	1	R3	499k	Vishay
18	1	R5	26.1k	Vishay
19	1	R6	1.43k	Vishay
20	1	U1	SC2604	Semtech

Applications Information (Cont.)

Start up



Inductor current and DRV pin voltage at OCP



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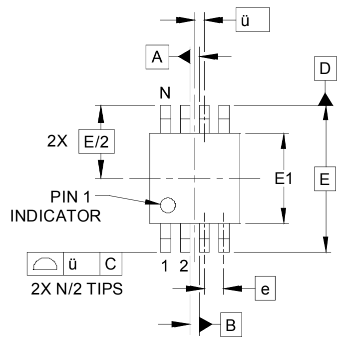
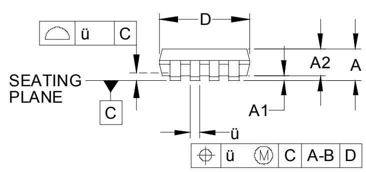
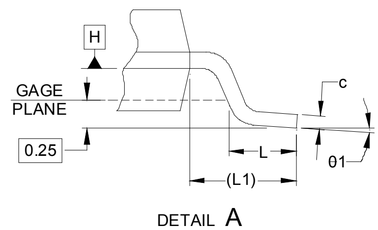
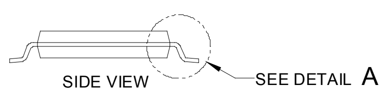
Outline Drawing - MSOP-8



DIM	DIMENSIONS INCHES MIN	NOM	MAX	üüüüü MIN	NOM	MAX
A	-	-	.043	-	-	1.10
A1	.000	-	.006	0.00	-	0.15
A2	.030	-	.037	0.75	-	0.95
b	.009	-	.015	0.22	-	0.38
c	.003	-	.009	0.08	-	0.23
D	.114	.118	.122	2.90	3.00	3.10
E1	.114	.118	.122	2.90	3.00	3.10
E	.193 BSC			4.90 BSC		
e	.026 BSC			0.65 BSC		
L	.016	.024	.032	0.40	0.60	0.80
L1	(.037)			(.95)		
N	8			8		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.005			0.13		
ccc	.010			0.25		



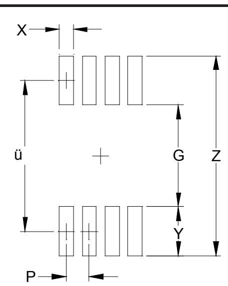




NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE ü
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MO-187, VARIATION AA.

Land Pattern - MSOP-8

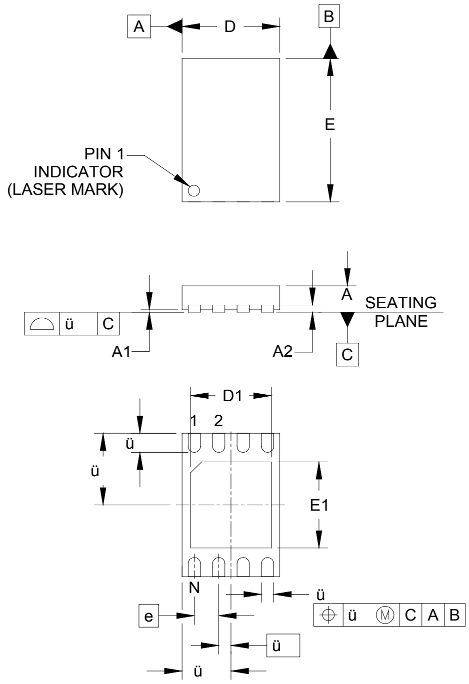


DIM	DIMENSIONS INCHES	üüüüü
C	(.161)	(4.10)
G	.098	2.50
P	.026	0.65
X	.016	0.40
Y	.063	1.60
Z	.224	5.70

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

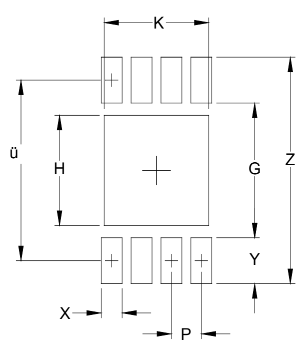
Outline Drawing - 2x3 MLPD-UT8



DIM	INCHES			üüüüü		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.020	-	.024	0.50	-	0.60
A1	.000	-	.002	0.00	-	0.05
A2	(.006)			(0.1524)		
b	.007	.010	.012	0.18	0.25	0.30
D	.075	.079	.083	1.90	2.00	2.10
D1	.059	.065	.069	1.50	1.65	1.75
E	.114	.118	.122	2.90	3.00	3.10
E1	.065	.071	.075	1.65	1.80	1.90
e	.020 BSC			0.50 BSC		
L	.012	.016	.020	0.30	0.40	0.50
N	8			8		
aaa	.003			0.08		
bbb	.003			0.08		

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Land Pattern - 2x3 MLPD-UT8



DIM	INCHES	üüüüü
C	(.116)	(2.95)
G	.087	2.20
H	.071	1.80
K	.069	1.75
P	.020	0.50
X	.012	0.30
Y	.030	0.75
Z	.146	3.70

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

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