

Absolute Maximum Ratings

| | | | |
|--------------------------------------|-----------------------------------|---|-----------------|
| V _{CC} to GND | -0.3V to +6.0V | Continuous Power Dissipation (T _A = +70°C) | |
| RESET to GND | | 4-Pin SC70 (derate 3.1mW/°C above +70°C)..... | 245mW |
| Open-Drain | -0.3V to +6.0V | 4-Pin SOT143 (derate 4mW/°C above +70vC)..... | 320mW |
| Push-Pull | -0.3V to (V _{CC} + 0.3V) | Operating Temperature Range..... | -40°C to +125°C |
| MR to GND..... | -0.3V to (V _{CC} + 0.3V) | Storage Temperature Range..... | -65°C to +150°C |
| Input/Output Current (all pins)..... | 20mA | Junction Temperature..... | +150°C |
| | | Lead Temperature (soldering, 10s) | +300°C |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{CC} = +1.2V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|------------------|--|-----------------------|-----------------|-------|-------|
| Operating Voltage Range | V _{CC} | T _A = 0°C to +125°C | 1.0 | | 5.5 | V |
| | | T _A = -40°C to 0°C | 1.2 | | 5.5 | |
| Supply Current | I _{CC} | V _{CC} = +5.5V, no load | | 7 | 13 | µA |
| | | V _{CC} = +3.6V, no load | | 6 | 11 | |
| | | V _{CC} = +2.5V, no load | | 4 | 8 | |
| | | V _{CC} = +1.8V, no load | | 3 | 7.5 | |
| V _{CC} Reset Threshold (See the Reset Threshold Table) | V _{TH} | T _A = +25°C | -1.5% | V _{TH} | +1.5% | V |
| | | T _A = -40°C to +85°C | -2.5% | | +2.5% | |
| | | T _A = +85°C to +125°C | -3% | | +3% | |
| V _{CC} Reset Delay | t _{RD} | V _{CC} falling at 10mV/µs from V _{TH} + 100mV to V _{TH} - 100mV | | 35 | | µs |
| V _{CC} Reset Timeout Period | t _{RP} | D3 option | 150 | 225 | 300 | ms |
| | | D7 option | 1200 | 1800 | 2400 | |
| MR Timeout Period | t _{MRP} | D3 and D7 options | 150 | 225 | 300 | ms |
| MR Rising Debounce Period (Note 2) | t _{DEB} | D3 and D7 options | 150 | 225 | 300 | ms |
| MR Input Voltage | V _{IL} | V _{TH} < +4V | 0.3 x V _{CC} | | | V |
| | V _{IH} | | 0.7 x V _{CC} | | | |
| | V _{IL} | V _{TH} ≥ +4V | 0.8 | | | |
| | V _{IH} | | 2.4 | | | |
| MR Minimum Input Pulse | | | 1 | | | µs |
| MR Glitch Rejection | | | | 100 | | ns |
| MR to RESET Delay | | | | 200 | | ns |
| MR Pullup Resistance | | MR to V _{CC} | 500 | 1560 | 3000 | Ω |
| RESET Output High (MAX6468 Only) | V _{OH} | V _{CC} ≥ +2.5V, I _{SOURCE} = 500µA, RESET not asserted | 0.8 x V _{CC} | | | V |
| | | V _{CC} ≥ +4.5V, I _{SOURCE} = 800µA, RESET not asserted | 0.8 x V _{CC} | | | |

Electrical Characteristics

($V_{CC} = +1.2V$ to $+5.5V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$, unless otherwise noted. Typical values are at $T_A = +25^{\circ}C$.) (Note 1)

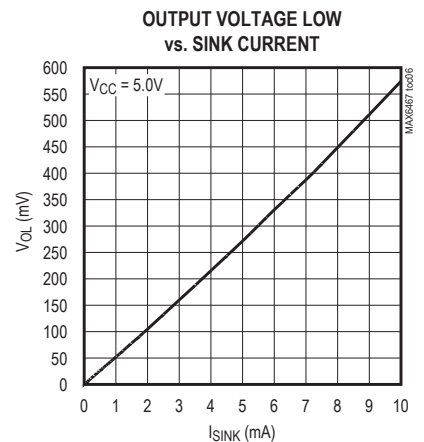
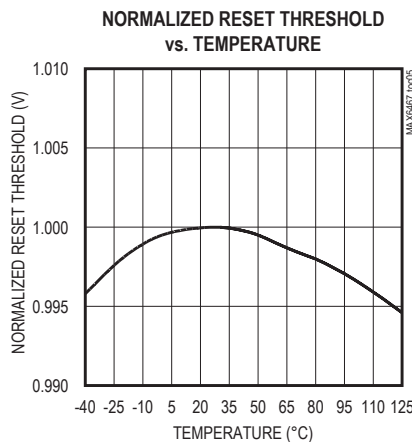
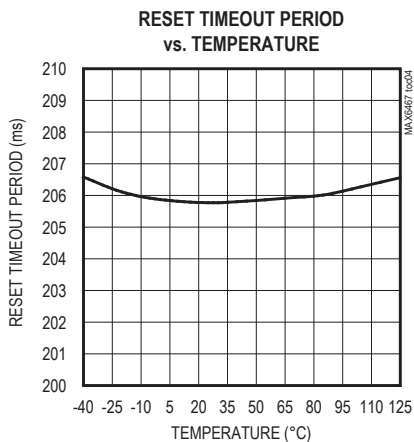
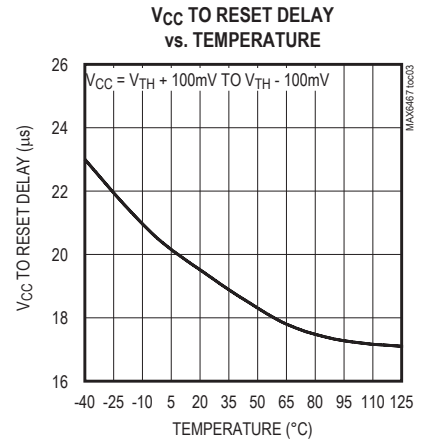
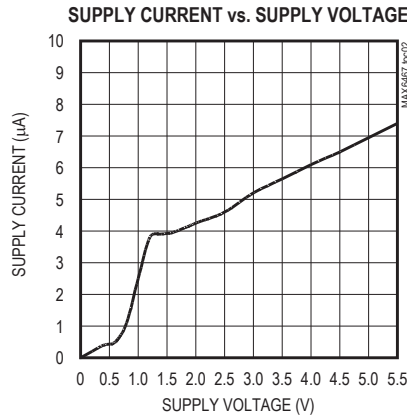
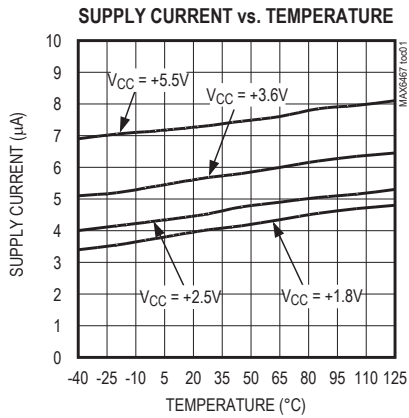
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|-----------|--|-----|-----|-----|---------|
| \overline{RESET} Output Low | V_{OL} | $V_{CC} \geq +1V$, $I_{SINK} = 80\mu A$, \overline{RESET} asserted | | | 0.3 | V |
| | | $V_{CC} \geq +2.5V$, $I_{SINK} = 1.2mA$, \overline{RESET} asserted | | | 0.3 | |
| | | $V_{CC} \geq +4.5V$, $I_{SINK} = 3.2mA$, \overline{RESET} asserted | | | 0.3 | |
| RESET Output Leakage Current (MAX6467 Only) | I_{LKG} | \overline{RESET} not asserted | | | 1 | μA |

Note 1: Specifications over temperature are guaranteed by design. Production testing at $T_A = +25^{\circ}C$ only.

Note 2: The \overline{MR} input ignores falling edges that occur within the \overline{MR} rising debounce period (t_{DEB}) after \overline{MR} first rises from low to high (after a valid \overline{MR} reset assertion). This prevents invalid reset assertion due to switch bounce.

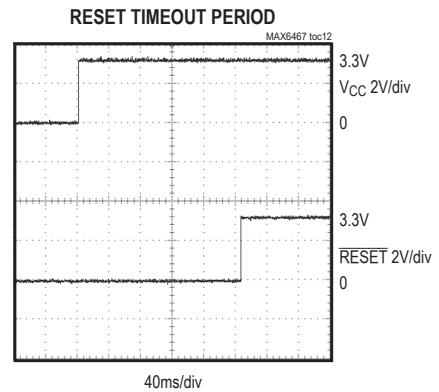
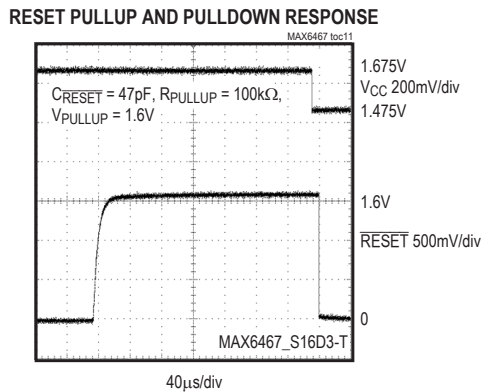
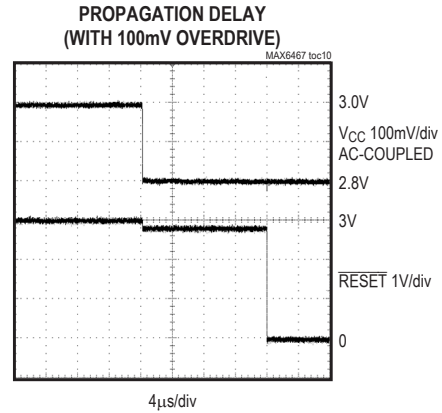
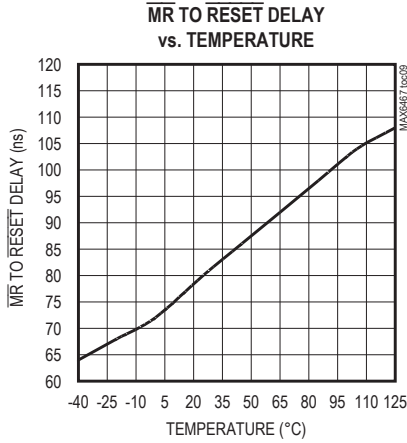
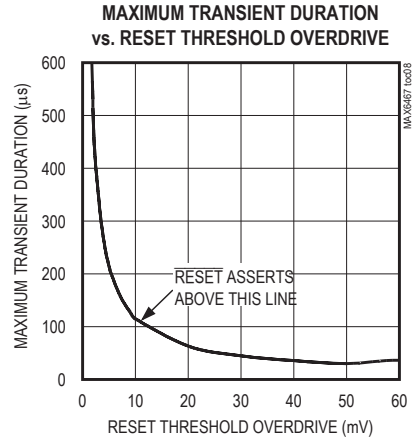
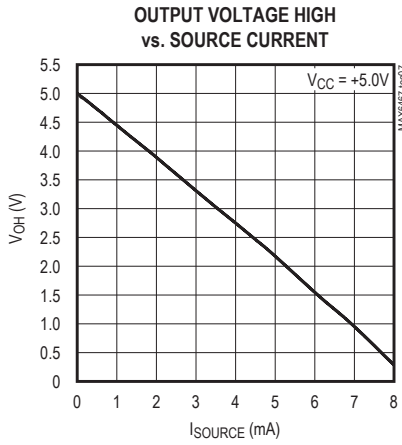
Typical Operating Characteristics

($V_{CC} = +5V$, MAX6468US29D3 device, $T_A = +25^{\circ}C$, unless otherwise noted.)

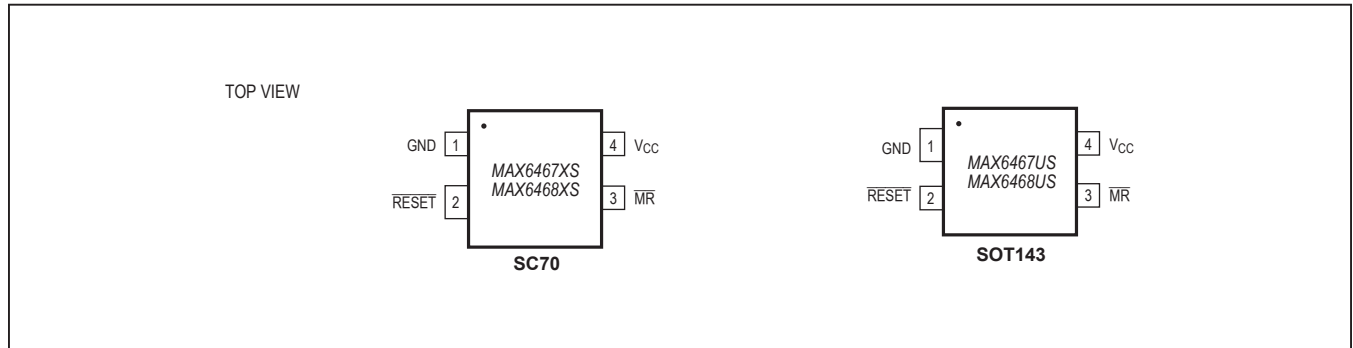


Typical Operating Characteristics

($V_{CC} = +5V$, MAX6468US29D3 device, $T_A = +25^\circ C$, unless otherwise noted.)



Pin Configurations



Pin Description

| PIN | NAME | FUNCTION |
|-----|---------------------------|---|
| 1 | GND | Ground |
| 2 | $\overline{\text{RESET}}$ | Reset Output. $\overline{\text{RESET}}$ is an active-low open-drain (MAX6467) or push-pull (MAX6468) output. $\overline{\text{RESET}}$ asserts low when V_{CC} drops below the selected threshold and remains low for the V_{CC} reset timeout period after V_{CC} rises above the threshold. The $\overline{\text{RESET}}$ one-shot asserts low for a fixed $\overline{\text{MR}}$ reset timeout period on the falling edge of the manual reset input. The open-drain output requires an external pullup resistor. |
| 3 | $\overline{\text{MR}}$ | Manual Reset Input. Drive $\overline{\text{MR}}$ low to initiate a reset output. $\overline{\text{MR}}$ controls an edge-triggered one-shot that asserts $\overline{\text{RESET}}$ low for a fixed $\overline{\text{MR}}$ timeout period when $\overline{\text{MR}}$ is driven low. Internal timing circuitry ignores switch close and open bounce to ensure proper one-shot reset timing. |
| 4 | V_{CC} | Power-Supply Input. V_{CC} provides power to the device and is also a monitored voltage. When V_{CC} drops below the selected threshold, $\overline{\text{RESET}}$ asserts low and remains low for the reset timeout period after V_{CC} rises above the threshold. For better noise immunity, bypass V_{CC} to GND with a 0.1 μ F capacitor. |

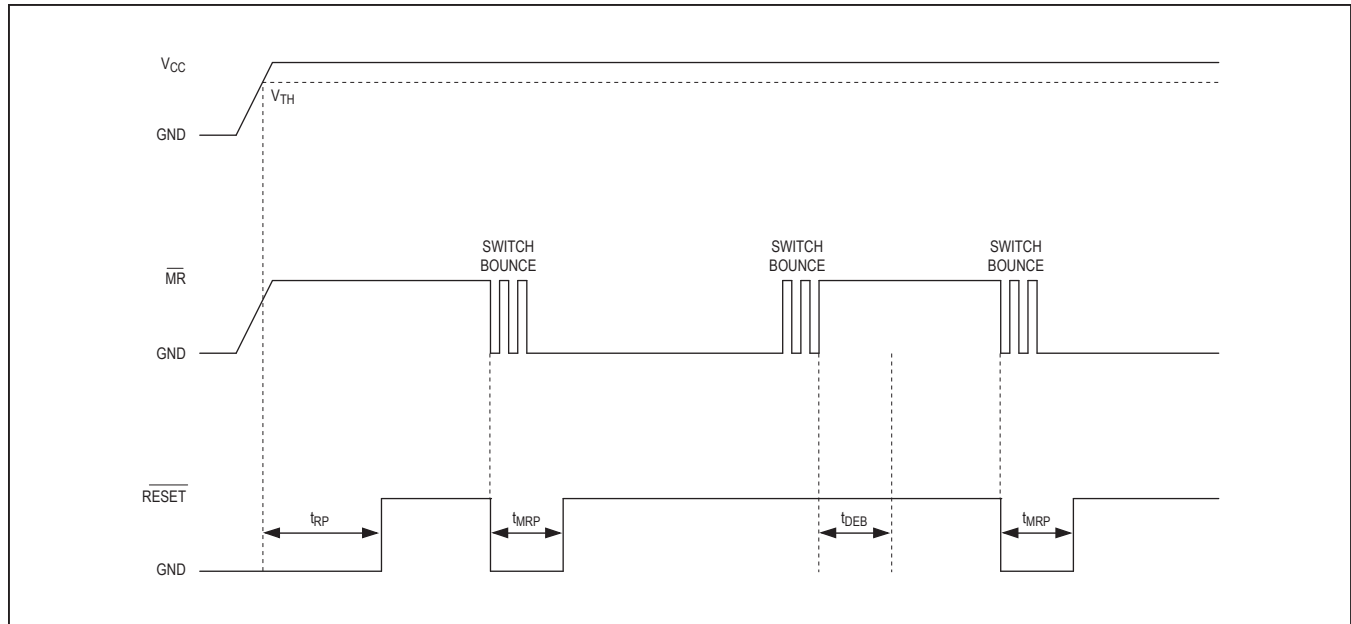


Figure 1. Timing Diagram

Detailed Description

Reset Output

The MAX6467 provides an active-low open-drain $\overline{\text{RESET}}$ output. The MAX6468 provides an active-low push-pull $\overline{\text{RESET}}$ output. $\overline{\text{RESET}}$ asserts low if V_{CC} drops below the selected threshold or if a falling edge occurs on $\overline{\text{MR}}$. $\overline{\text{RESET}}$ remains low for the V_{CC} reset timeout period after V_{CC} increases above the threshold voltage or is one-shot pulsed low for the $\overline{\text{MR}}$ timeout period after a falling edge on $\overline{\text{MR}}$.

Manual Reset Input

Many μP -based products require manual reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. A falling edge on $\overline{\text{MR}}$ asserts

$\overline{\text{RESET}}$ low. $\overline{\text{RESET}}$ is one-shot pulsed low for the $\overline{\text{MR}}$ timeout period after a falling edge on $\overline{\text{MR}}$. An internal 1.5k Ω pullup resistor to V_{CC} allows MR to be left unconnected if not used. $\overline{\text{MR}}$ can be driven with TTL or CMOS-logic levels, or with open-drain/collector outputs. Connect a normally open momentary pushbutton switch from $\overline{\text{MR}}$ to GND to realize a manual reset function. External debounce circuitry is not required, as the MAX6467/MAX6468 respond to the first falling edge on $\overline{\text{MR}}$ and ignore subsequent falling edges within the reset timeout period and during the $\overline{\text{MR}}$ debounce period (see Figure 1). After $\overline{\text{MR}}$ goes high for 150ms (t_{DEB}), the manual reset one-shot is ready to trigger a reset on the next $\overline{\text{MR}}$ falling edge. Connect a 0.1 μF capacitor from $\overline{\text{MR}}$ to GND when using long cables to provide additional noise immunity.

Reset Timeout Delay*

| RESET TIMEOUT SUFFIX | V _{CC} RESET TIMEOUT PERIOD (min/max) (ms) | MR TIMEOUT PERIOD (min/max) (ms) | MR RISING DEBOUNCE PERIOD (min/max) (ms) |
|----------------------|---|----------------------------------|--|
| D3 | 150/300 | 150/300 | 150/300 |
| D7 | 1200/2400 | 150/300 | 150/300 |

*Additional reset timeout options may be available. Contact factory for availability.

Applications Information

Falling V_{CC} Transients

In addition to issuing a reset to the μP during power-up, power-down, and brownout conditions, the MAX6467/MAX6468 are relatively immune to short-duration falling V_{CC} transients (glitches). The Typical Operating Characteristics section shows the Maximum Transient Duration vs. V_{CC} Overdrive for which the MAX6467/MAX6468 do not generate a reset pulse. This graph was generated using a falling pulse applied to V_{CC} starting above the actual reset threshold and ending below the threshold by the magnitude indicated (V_{CC} Overdrive). The graph indicates the typical maximum pulse width a falling V_{CC} transient can have without initiating a reset pulse. As the magnitude of the transient increases (goes

farther below the reset threshold), the maximum allowable pulse width decreases. A 0.1μF bypass capacitor from V_{CC} to GND provides additional transient immunity.

Ensuring a Valid RESET Output Down to V_{CC} = 0V

The MAX6467/MAX6468 guarantee proper operation down to V_{CC} = +1V. In applications that require valid reset levels down to V_{CC} = 0V, a pulldown resistor to active-low outputs (MAX6468 only, Figure 3) ensures that RESET remains valid while the RESET output can no longer sink current. This scheme does not work with the open-drain outputs of the MAX6467. Ensure that the resistor value used does not overload the RESET output when V_{CC} is above the reset threshold. For most applications, use 100kΩ to 1MΩ.

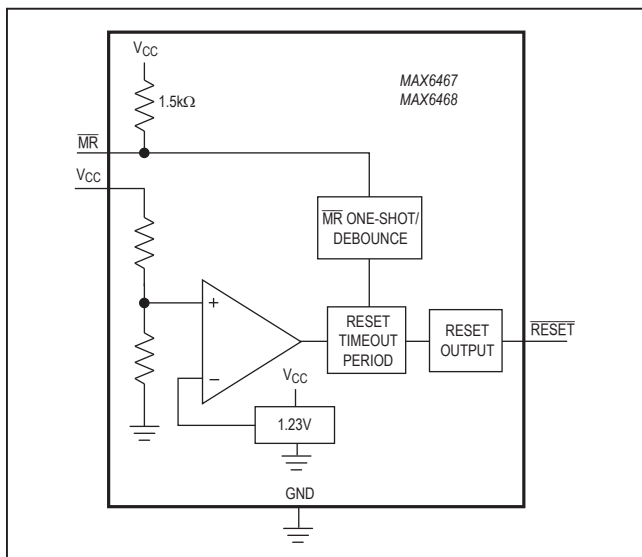


Figure 2. Functional Diagram

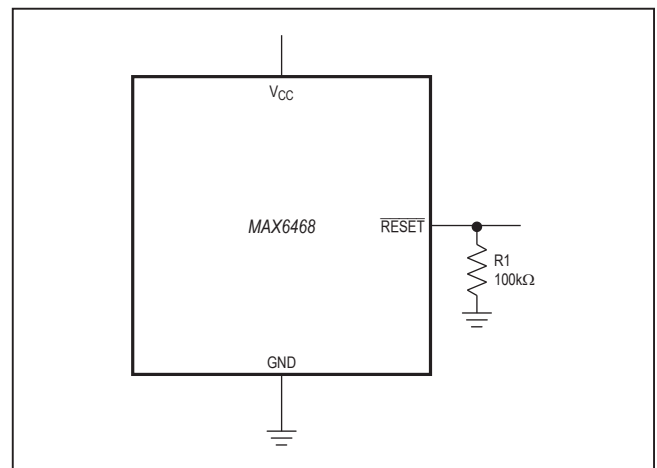


Figure 3. RESET Valid to V_{CC} = 0V

Chip Information

TRANSISTOR COUNT: 748

PROCESS: BICMOS

Standard Versions

| PART | TOP MARK |
|-----------------------|----------|
| MAX6467 XS16D3 | AGL |
| MAX6467XS22D3 | AGM |
| MAX6467XS26D3 | AGN |
| MAX6467XS29D3 | AGO |
| MAX6467XS46D3 | AGP |
| MAX6467US16D3 | KAFN |
| MAX6467US22D3 | KAFO |
| MAX6467US26D3 | KAFP |
| MAX6467US29D3 | KAFQ |
| MAX6467US46D3 | KAFR |
| MAX6468 XS16D3 | AGQ |
| MAX6468XS22D3 | AGR |
| MAX6468XS26D3 | AGS |
| MAX6468XS29D3 | AGC |
| MAX6468XS46D3 | AGB |
| MAX6468US16D3 | KAFS |
| MAX6468US22D3 | KAFT |
| MAX6468US26D3 | KAFU |
| MAX6468US29D3 | KAEW |
| MAX6468US46D3 | KAFV |

Reset Threshold (-40°C to +85°C)

| SUFFIX | V _{TH} (min) | V _{TH} (typ) | V _{TH} (max) |
|--------|-----------------------|-----------------------|-----------------------|
| 46 | 4.509 | 4.625 | 4.741 |
| 45 | 4.388 | 4.500 | 4.613 |
| 44 | 4.266 | 4.375 | 4.484 |
| 43 | 4.193 | 4.300 | 4.408 |
| 42 | 4.095 | 4.200 | 4.305 |
| 41 | 3.998 | 4.100 | 4.203 |
| 40 | 3.900 | 4.000 | 4.100 |
| 39 | 3.803 | 3.900 | 3.998 |
| 38 | 3.705 | 3.800 | 3.895 |
| 37 | 3.608 | 3.700 | 3.793 |
| 36 | 3.510 | 3.600 | 3.690 |
| 35 | 3.413 | 3.500 | 3.588 |
| 34 | 3.315 | 3.400 | 3.485 |
| 33 | 3.218 | 3.300 | 3.383 |
| 32 | 3.120 | 3.200 | 3.280 |
| 31 | 2.998 | 3.075 | 3.152 |
| 30 | 2.925 | 3.000 | 3.075 |
| 29 | 2.852 | 2.925 | 2.998 |
| 28 | 2.730 | 2.800 | 2.870 |
| 27 | 2.633 | 2.700 | 2.768 |
| 26 | 2.559 | 2.625 | 2.691 |
| 25 | 2.438 | 2.500 | 2.563 |
| 24 | 2.340 | 2.400 | 2.460 |
| 23 | 2.255 | 2.313 | 2.370 |
| 22 | 2.133 | 2.188 | 2.242 |
| 21 | 2.048 | 2.100 | 2.153 |
| 20 | 1.950 | 2.000 | 2.050 |
| 19 | 1.853 | 1.900 | 1.948 |
| 18 | 1.755 | 1.800 | 1.845 |
| 17 | 1.623 | 1.665 | 1.707 |
| 16 | 1.536 | 1.575 | 1.614 |

Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|-------------------------|-----------------|-------------|
| MAX6467 XS__D_-T | -40°C to +125°C | 4 SC70-4 |
| MAX6467XS__D_/V+T* | -40°C to +125°C | 4 SC70-4 |
| MAX6467XS29D3/V+T | -40°C to +125°C | 4 SC70-4 |
| MAX6467XS32D3/V+T | -40°C to +125°C | 4 SC70-4 |
| MAX6467XS16D3/V+T | -40°C to +125°C | 4 SC70-4 |
| MAX6467US__D_-T | -40°C to +125°C | 4 SOT143-4 |
| MAX6468 XS__D_-T | -40°C to +125°C | 4 SC70-4 |
| MAX6468US__D_-T | -40°C to +125°C | 4 SOT143-4 |

Note: Insert reset threshold suffix (see Reset Threshold table) after XS or US. Insert reset timeout delay (see Reset Timeout Delay table) after D to complete the part number. Sample stock is generally held on standard versions only (see Standard Versions table). Standard versions have an order increment requirement of 2500 pieces. Nonstandard versions have an order increment requirement of 10,000 pieces. Contact factory for availability. Devices are available in both leaded and lead-free packaging. Specify lead-free by replacing “T” with “+T” when ordering.

T = Tape and reel.

/V denotes an automotive qualified part.

+Denotes a lead(Pb)-free/RoHS-compliant package.

*Future product—contact factory for availability.

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|--------------|--------------|-------------------------|-------------------------|
| 4 SC70 | X4+1 | 21-0098 | 90-0187 |
| 4 SOT143 | U4+1 | 21-0052 | 90-0183 |

Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|-----------------|---------------|--|---------------|
| 2 | 3/14 | Added /V OPNs | 1 |
| 3 | 4/14 | Removed automotive reference from <i>Applications</i> section | 1 |
| | 6/14 | Reversed 4/14 change and added automotive reference back to <i>Applications</i> section | 1 |
| 4 | 10/14 | Fixed typo in <i>Package Information</i> section | 9 |
| 5 | 10/15 | Fixed MR Pullup Resistance specification in <i>Electrical Characteristics</i> table | 2 |
| 6 | 3/18 | Updated <i>Benefits and Features</i> and <i>Ordering Information</i> table | 1, 9 |
| 6.1 | | Reformatted <i>Standard Versions</i> table | 8 |
| 7 | 3/20 | Updated <i>Features</i> , <i>Absolute Maximum Ratings</i> , <i>Detailed Description</i> , <i>Applications Information</i> , and <i>Package Information</i> table | 1, 2, 6, 7, 9 |
| 8 | 7/21 | Updated <i>Ordering information</i> table | 9 |



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