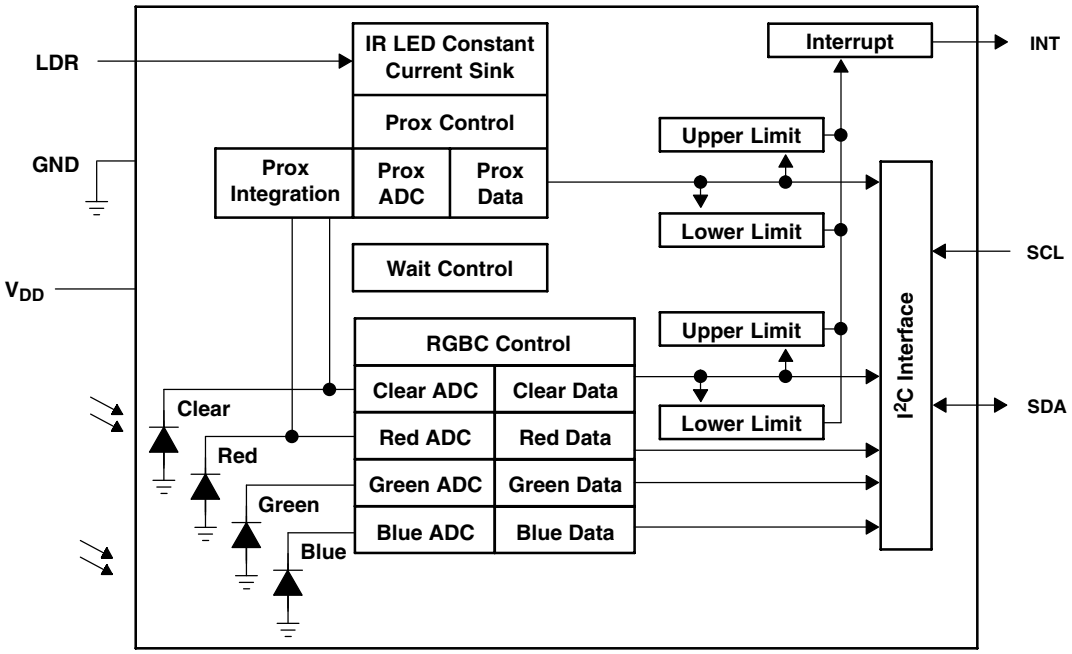
The proximity function is targeted specifically towards battery-powered mobile devices, LCD monitor, laptop, and flat-panel television applications. In cell phones, the proximity detection can detect when the user positions the phone close to their ear. The device is fast enough to provide proximity information at a high repetition rate needed when answering a phone call. It can also detect both close and far distances so the application can implement more complex algorithms to provide a more robust interface. In laptop or monitor applications, the product is sensitive enough to determine whether a user is in front of the laptop using the keyboard or away from the desk. This provides both improved *green* power saving capability and the added security to lock the computer when the user is not present.

Functional Block Diagram



Detailed Description

The TCS3771 light-to-digital device contains a 4 × 4 photodiode array, integrating amplifiers, ADCs, accumulators, clocks, buffers, comparators, a state machine, and an I^2C interface. The 4 × 4 photodiode array is composed of red-filtered, green-filtered, blue-filtered, and clear photodiodes — four of each type. Four integrating ADCs simultaneously convert the amplified photodiode currents to a digital value providing up to 16 bits of resolution. Upon completion of the conversion cycle, the conversion result is transferred to the data registers. The transfers are double-buffered to ensure that the integrity of the data is maintained. Communication to the device is accomplished through a fast (up to 400 kHz), two-wire I^2C serial bus for easy connection to a microcontroller or embedded controller.

The TCS3771 provides a separate pin for level-style interrupts. When interrupts are enabled and a pre-set value is exceeded, the interrupt pin is asserted and remains asserted until cleared by the controlling firmware. The interrupt feature simplifies and improves system efficiency by eliminating the need to poll a sensor for a light intensity or proximity value. An interrupt is generated when the value of an RGBC or proximity conversion exceeds either an upper or lower threshold. In addition, a programmable interrupt persistence feature allows the user to determine how many consecutive exceeded thresholds are necessary to trigger an interrupt. Interrupt thresholds and persistence settings are configured independently for both RGBC and proximity.

Proximity detection requires only a single external IR LED. An internal LED driver can be configured to provide a constant current sink of 12.5 mA, 25 mA, 50 mA or 100 mA of current. No external current limiting resistor is required. The number of proximity LED pulses can be programmed from 1 to 255 pulses. Each pulse has a 14-µs period. This LED current coupled with the programmable number of pulses provides a 2000:1 contiguous dynamic range.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	TYPE	DESCRIPTION
GND	3		Power supply ground. All voltages are referenced to GND.
INT	5	O	Interrupt — open drain (active low).
LDR	4	O	LED driver for proximity emitter — up to 100 mA, open drain.
SCL	2	I	I^2C serial clock input terminal — clock signal for I^2C serial data.
SDA	6	I/O	I^2C serial data I/O terminal — serial data I/O for I^2C .
V_{DD}	1		Supply voltage.

Available Options

DEVICE	ADDRESS	PACKAGE – LEADS	INTERFACE DESCRIPTION	ORDERING NUMBER
TCS37711†	0x39	FN–6	I^2C Vbus = V_{DD} Interface	TCS37711FN
TCS37713†	0x39	FN–6	I^2C Vbus = 1.8 V Interface	TCS37713FN
TCS37715†	0x29	FN–6	I^2C Vbus = V_{DD} Interface	TCS37715FN
TCS37717	0x29	FN–6	I^2C Vbus = 1.8 V Interface	TCS37717FN

† Contact TAOS for availability.

Absolute Maximum Ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . 3.8 V
Digital output voltage range, V_O . . . . . –0.5 V to 3.8 V
Digital output current, I_O . . . . . –1 mA to 20 mA
Storage temperature range, T_{stg} . . . . . –40°C to 85°C
ESD tolerance, human body model . . . . . 2000 V

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to GND.

Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	2.7	3	3.3	V
Operating free-air temperature, T_A	–30		70	°C

Operating Characteristics, V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Supply current	Active — LDR pulses off		235	330	µA
		Wait mode		65		
		Sleep mode — no I^2C activity		2.5	10	
V_{OL}	INT, SDA output low voltage	3 mA sink current	0		0.4	V
		6 mA sink current	0		0.6	
I_{LEAK}	Leakage current, SDA, SCL, INT pins		–5		5	µA
I_{LEAK}	Leakage current, LDR pin		–10		+10	µA
V_{IH}	SCL, SDA input high voltage	TCS37711 & TCS37715	0.7 V_{DD}			V
		TCS37713 & TCS37717	1.25			
V_{IL}	SCL, SDA input low voltage	TCS37711 & TCS37715			0.3 V_{DD}	V
		TCS37713 & TCS37717			0.54	

Optical Characteristics, V_{DD} = 3 V, T_A = 25°C, GAIN = 16, ATIME = 0xF6 (unless otherwise noted) (see Note 1)

PARAMETER		TEST CONDITIONS	Red Channel			Green Channel			Blue Channel			Clear Channel			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
R_e	Irradiance responsivity	λ_D = 465 nm See Note 2	0%		15%	10%		42%	65%		88%	19.2	24	28.8	(counts/ µW/ cm^2)
		λ_D = 525 nm See Note 3	8%		25%	60%		85%	9%		35%	22.4	28	33.6	
		λ_D = 625 nm See Note 4	85%		110%	0%		15%	5%		25%	27.2	34	40.8	

NOTES: 1. The percentage shown represents the ratio of the respective red, green, or blue channel value to the clear channel value.
2. The 465 nm input irradiance is supplied by an InGaN light-emitting diode with the following characteristics: dominant wavelength λ_D = 465 nm, spectral halfwidth $\Delta\lambda$½ = 22 nm, and luminous efficacy = 75 lm/W.
3. The 525 nm input irradiance is supplied by an InGaN light-emitting diode with the following characteristics: dominant wavelength λ_D = 525 nm, spectral halfwidth $\Delta\lambda$½ = 35 nm, and luminous efficacy = 520 lm/W.
4. The 625 nm input irradiance is supplied by a AlInGaP light-emitting diode with the following characteristics: dominant wavelength λ_D = 625 nm, spectral halfwidth $\Delta\lambda$½ = 9 nm, and luminous efficacy = 155 lm/W.

RGBC Characteristics, V_{DD} = 3 V, T_A = 25°C, AGAIN = 16, AEN = 1 (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dark ADC count value	E_e = 0, AGAIN = 60×, ATIME = 0xD6 (100 ms)	0	1	5	counts
ADC integration time step size	ATIME = 0xFF	2.27	2.4	2.56	ms
ADC number of integration steps		1		256	steps
ADC counts per step		0		1024	counts
ADC count value	ATIME = 0xC0 (153.6 ms)	0		65535	counts
Gain scaling, relative to 1× gain setting	4×	3.8	4	4.2	%
	16×	15	16	16.8	
	60×	58	60	63	

Proximity Characteristics, V_{DD} = 3 V, T_A = 25°C, Gain = 16, PEN = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	CONDITION	MIN	TYP	MAX	UNIT
I_{DD}	Supply current	LDR pulse on			3		mA
	ADC conversion time step size	PTIME = 0xFF		2.27	2.4	2.56	ms
	ADC number of integration steps			1		256	steps
	ADC counts per step			0		1023	counts
	IR LED pulse count			0		255	pulses
	LED pulse period	Two or more pulses			14		µs
	LED pulse width — LED on time				6.3		µs
	LED drive current	I_{SINK} sink current @ 600 mV, LDR pin	PDRIVE = 0	80	106	132	mA
			PDRIVE = 1		50		
			PDRIVE = 2		25		
			PDRIVE = 3		12.5		
	Dark count value	E_e = 0, PTIME = 0xFB, PPULSE = 2				900	counts
	Red channel	λ_P = 850 nm, E_e = 45.3 µW/cm^2, PTIME = 0xFB, PPULSE = 2 (See note 1)		1000		3000	counts
	Clear channel	λ_P = 850 nm, E_e = 45.3 µW/cm^2, PTIME = 0xFB, PPULSE = 2 (See note 1)		1000		3000	counts
	Operating distance (See note 2)				30		inches

NOTES: 1. The specified light intensity is 100% modulated by the pulse output of the device so that during the pulse output low time, the light intensity is at the specified level, and 0 otherwise.

2. Proximity Operating Distance is dependent upon emitter properties and the reflective properties of the proximity surface. The nominal value shown uses an IR emitter with a peak wavelength of 850nm and a 20° half angle. The proximity surface used is a 90% reflective (white surface) 16 × 20-inch Kodak Gray Card. 60 mw/SR, 100 mA, 64 pulses, open view (no glass). **Note:** Greater distances are achievable with appropriate system considerations.

Wait Characteristics, V_{DD} = 3 V, T_A = 25°C, Gain = 16, WEN = 1 (unless otherwise noted)

PARAMETER	TEST CONDITIONS	CHANNEL	MIN	TYP	MAX	UNIT
Wait step size	WTIME = 0xFF		2.27	2.4	2.56	ms
Wait number of steps			1		256	steps

AC Electrical Characteristics, V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER†		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(SCL)}$	Clock frequency (I^2C only)		0		400	kHz
$t_{(BUF)}$	Bus free time between start and stop condition		1.3			µs
$t_{(HDSTA)}$	Hold time after (repeated) start condition. After this period, the first clock is generated.		0.6			µs
$t_{(SUSTA)}$	Repeated start condition setup time		0.6			µs
$t_{(SUSTO)}$	Stop condition setup time		0.6			µs
$t_{(HDDAT)}$	Data hold time		0			µs
$t_{(SUDAT)}$	Data setup time		100			ns
$t_{(LOW)}$	SCL clock low period		1.3			µs
$t_{(HIGH)}$	SCL clock high period		0.6			µs
t_F	Clock/data fall time				300	ns
t_R	Clock/data rise time				300	ns
C_i	Input pin capacitance				10	pF

† Specified by design and characterization; not production tested.

PARAMETER MEASUREMENT INFORMATION

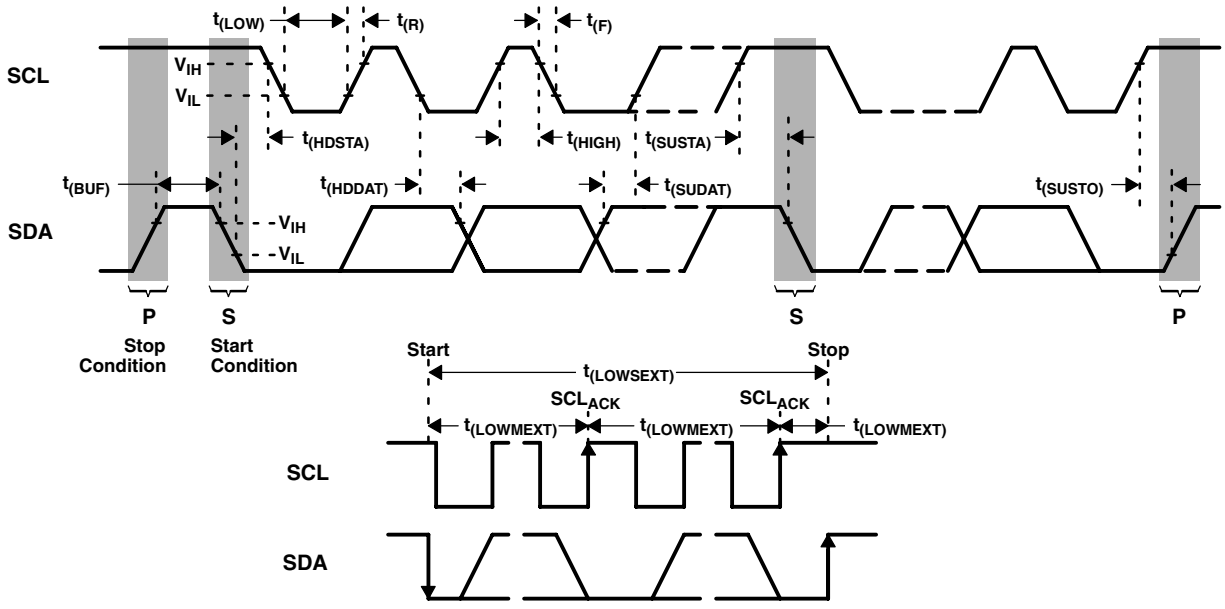


Figure 1. Timing Diagrams

TYPICAL CHARACTERISTICS

PHOTODIODE SPECTRAL RESPONSIVITY

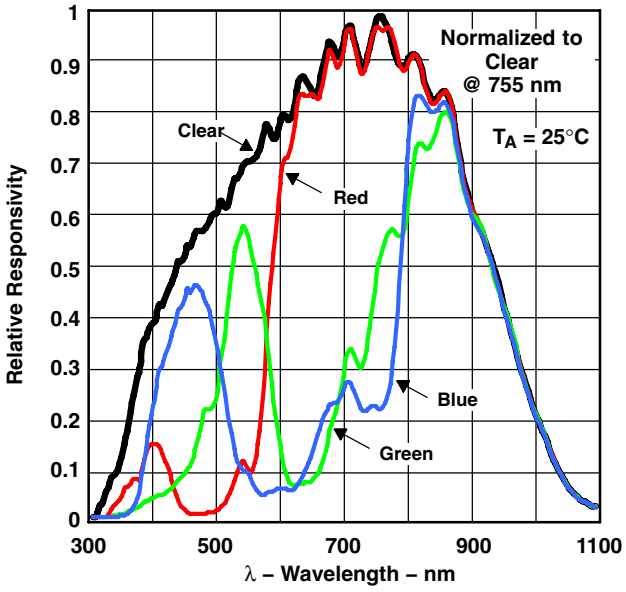


Figure 2

TYPICAL LDR CURRENT vs. VOLTAGE

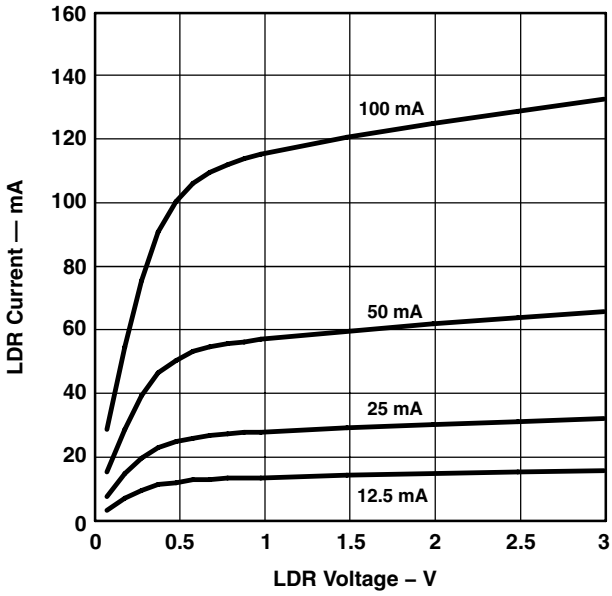


Figure 3

NORMALIZED I_{DD} vs. V_{DD} and TEMPERATURE

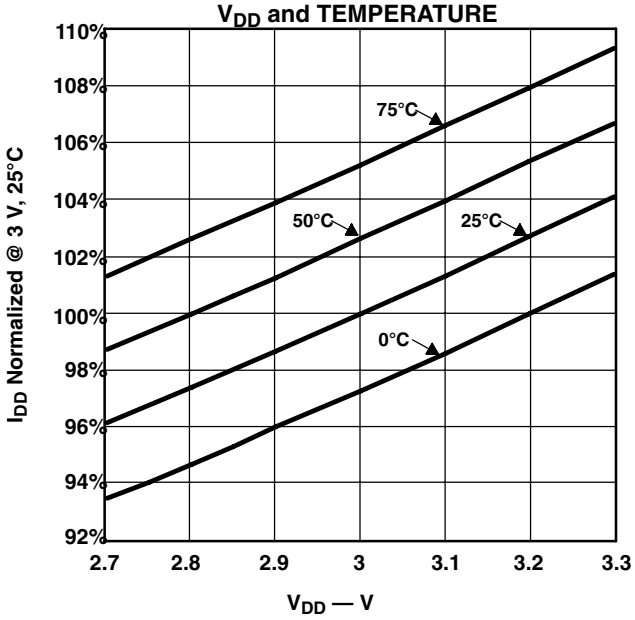


Figure 4

NORMALIZED RESPONSIVITY vs. ANGULAR DISPLACEMENT

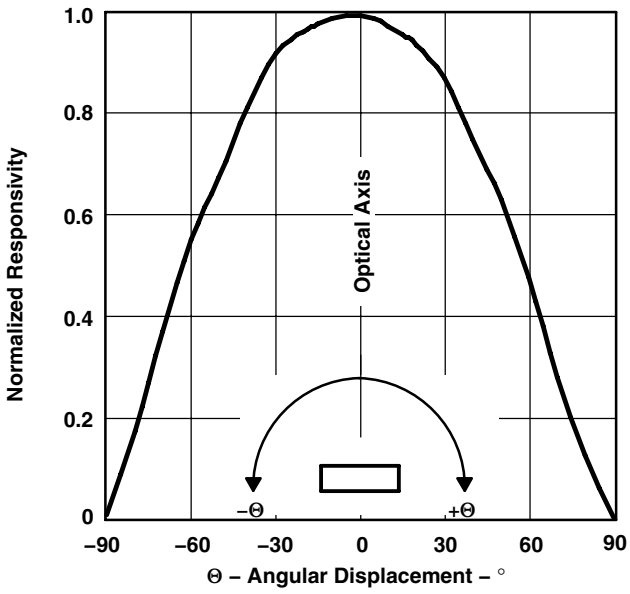


Figure 5

TYPICAL CHARACTERISTICS

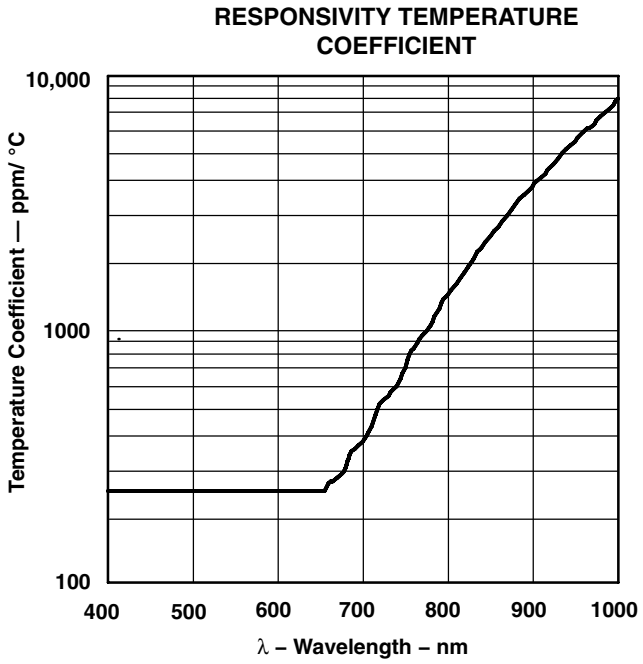


Figure 6

PRINCIPLES OF OPERATION

System State Machine

The TCS3771 provides control of RGBC, proximity detection, and power management functionality through an internal state machine (Figure 7). After a power-on-reset, the device is in the sleep mode. As soon as the PON bit is set, the device will move to the start state. It will then continue through the Prox, Wait, and RGBC states. If these states are enabled, the device will execute each function. If the PON bit is set to 0, the state machine will continue until all conversions are completed and then go into a low power sleep mode.

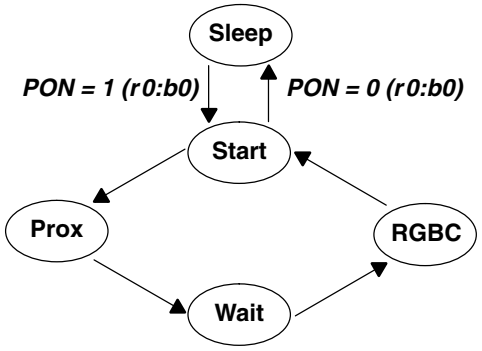


Figure 7. Simplified State Diagram

NOTE: In this document, the nomenclature uses the bit field name in italics followed by the register number and bit number to allow the user to easily identify the register and bit that controls the function. For example, the power on (PON) is in register 0, bit 0. This is represented as *PON (r0:b0)*.

RGBC Operation

The RGBC engine contains RGBC gain control (AGAIN) and four integrating analog-to-digital converters (ADC) for the RGBC photodiodes. The RGBC integration time (ATIME) impacts both the resolution and the sensitivity of the RGBC reading. Integration of all four channels occurs simultaneously and upon completion of the conversion cycle, the results are transferred to the color data registers. This data is also referred to as channel count. The transfers are double-buffered to ensure that invalid data is not read during the transfer. After the transfer, the device automatically moves to the next state in accordance with the configured state machine.

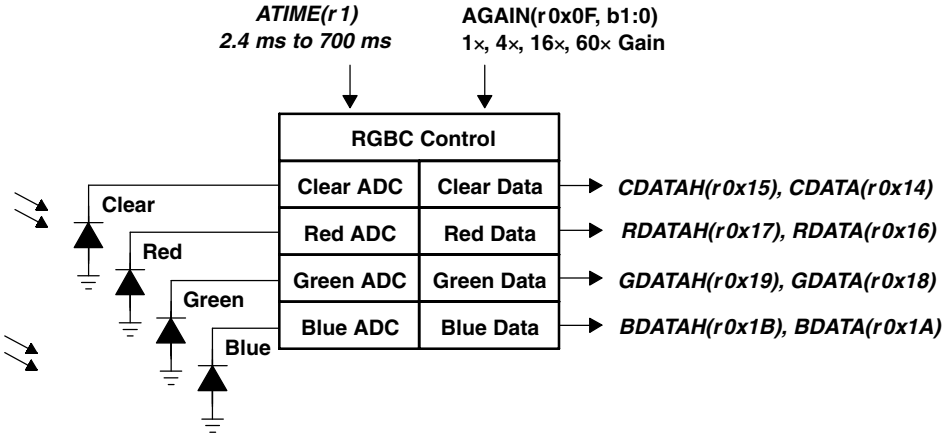


Figure 8. RGBC Operation

The registers for programming the integration and wait times are a 2's compliment values. The actual time can be calculated as follows:

ATIME = 256 – Integration Time / 2.4 ms

Inversely, the time can be calculated from the register value as follows:

Integration Time = 2.4 ms × (256 – ATIME)

For example, if a 100-ms integration time is needed, the device needs to be programmed to:

256 – (100 / 2.4) = 256 – 42 = 214 = 0xD6

Conversely, the programmed value of 0xC0 would correspond to:

(256 – 0xC0) × 2.4 = 64 × 2.4 = 154 ms.

Proximity Detection

Proximity sensing uses an external light source (generally an infrared emitter) to emit light, which is then viewed by the integrated light detector to measure the amount of reflected light when an object is in the light path (Figure 9). The amount of light detected from a reflected surface can then be used to determine an object's proximity to the sensor.

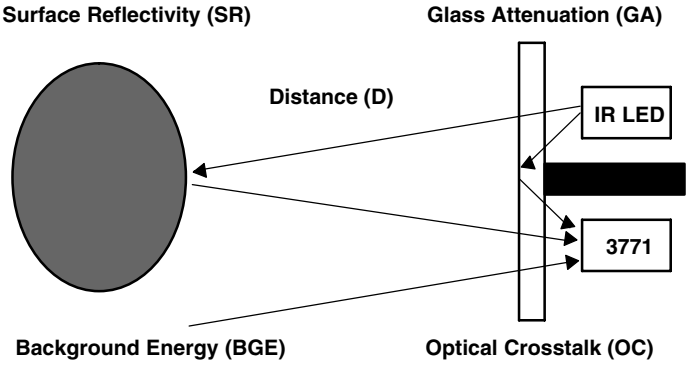


Figure 9. Proximity Detection

The TCS3771 has controls for the number of IR pulses (PPCOUNT), the integration time (PTIME), the LED drive current (PDRIVE) and the photodiode configuration (PDIODE). The photodiode configuration can be set to red diode (recommended), clear diode, or a combination of both diodes. At the end of the integration cycle, the results are latched into the proximity data (PDATA) register.

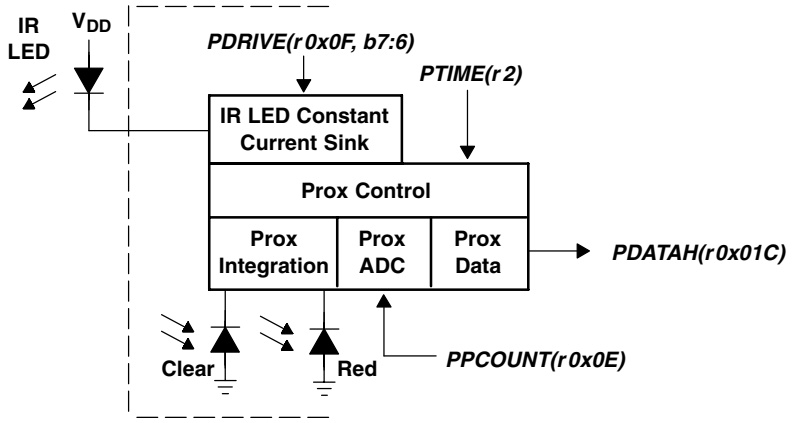


Figure 10. Proximity Detection Operation

The LED drive current is controlled by a regulated current sink on the LDR pin. This feature eliminates the need to use a current limiting resistor to control LED current. The LED drive current can be configured for 12.5 mA, 25 mA, 50 mA, or 100 mA. For higher LED drive requirements, an external P-FET transistor can be used to control the LED current.

The number of LED pulses can be programmed to any value between 1 and 255 pulses as needed. Increasing the number of LED pulses at a given current will increase the sensor sensitivity. Sensitivity grows by the square root of the number of pulses. Each pulse has a 14-µs period.

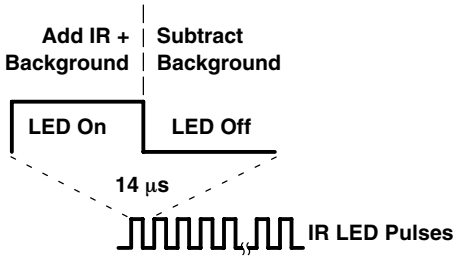


Figure 11. Proximity IR LED Waveform

The proximity integration time (PTIME) is the period of time that the internal ADC converts the analog signal to a digital count. It is recommend that this be set to a minimum of PTIME = 0xFF or 2.4 ms.

The combination of LED power and number of pulses can be used to control the distance at which the sensor can detect proximity. Figure 12 shows an example of the distances covered with settings such that each curve covers 2× the distance. Counts up to 64 pulses provide a 16× range.

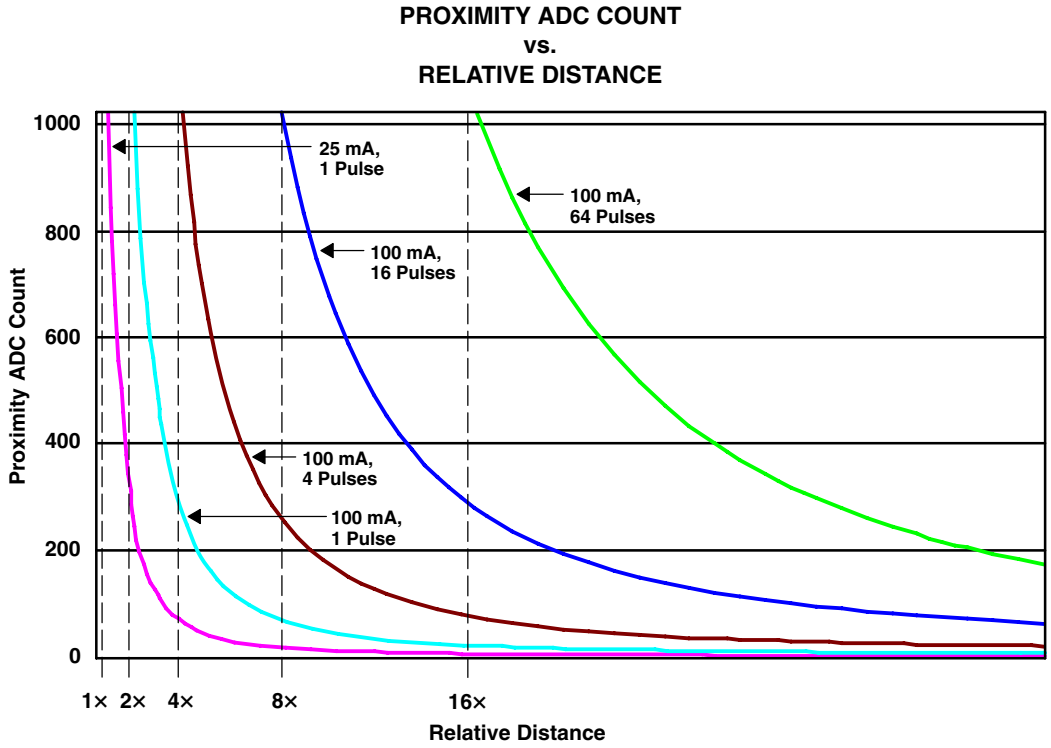


Figure 12

Interrupts

The interrupt feature simplifies and improves system efficiency by eliminating the need to poll the sensor for light intensity or proximity values outside of a user-defined range. While the interrupt function is always enabled and it's status is available in the status register (0x13), the output of the interrupt state can be enabled using the proximity interrupt enable (PIEN) or RGBC interrupt enable (AIEN) fields in the enable register (0x00).

Four 16-bit interrupt threshold registers allow the user to set limits below and above a desired light level and proximity range. An interrupt can be generated when the RGBC Clear data (CDATA) falls outside of the desired light level range, as determined by the values in the RGBC interrupt low threshold registers (AILTx) and RGBC interrupt high threshold registers (AIHTx). Likewise, an out-of-range proximity interrupt can be generated when the proximity data (PDATA) falls below the proximity interrupt low threshold (PILTx) or exceeds the proximity interrupt high threshold (PIHTx). It is important to note that the low threshold value must be less than the high threshold value for proper operation.

To further control when an interrupt occurs, the device provides a persistence filter. The persistence filter allows the user to specify the number of consecutive out-of-range RGBC or proximity occurrences before an interrupt is generated. The persistence register (0x0C) allows the user to set the RGBC persistence (APERS) and the proximity persistence (PPERS) values. See the persistence register for details on the persistence filter values. Once the persistence filter generates an interrupt, it will continue until a special function interrupt clear command is received (see command register).

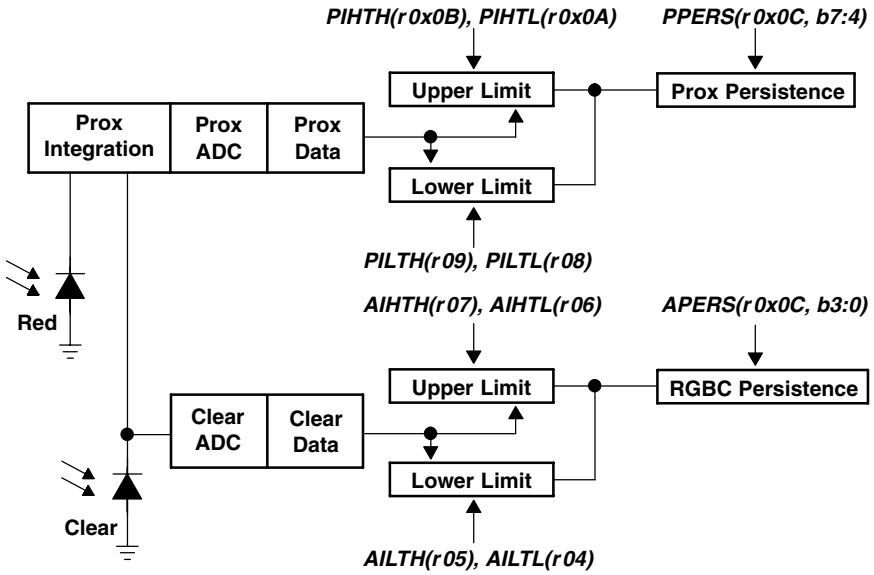


Figure 13. Programmable Interrupt

State Diagram

Figure 14 shows a more detailed flow for the state machine. The device starts in the sleep mode. The PON bit is written to enable the device. A 2.4-ms delay will occur before entering the start state. If the PEN bit is set, the state machine will step through the proximity states of proximity accumulate and then proximity ADC conversion. As soon as the conversion is complete, the state machine will move to the following state.

If the WEN bit is set, the state machine will then cycle through the wait state. If the WLONG bit is set, the wait cycles are extended by 12× over normal operation. When the wait counter terminates, the state machine will step to the RGBC state.

The AEN should always be set, even in proximity-only operation. In this case, a minimum of 1 integration time step should be programmed. The RGBC state machine will continue until it reaches the terminal count at which point the data will be latched in the RGBC register and the interrupt set, if enabled.

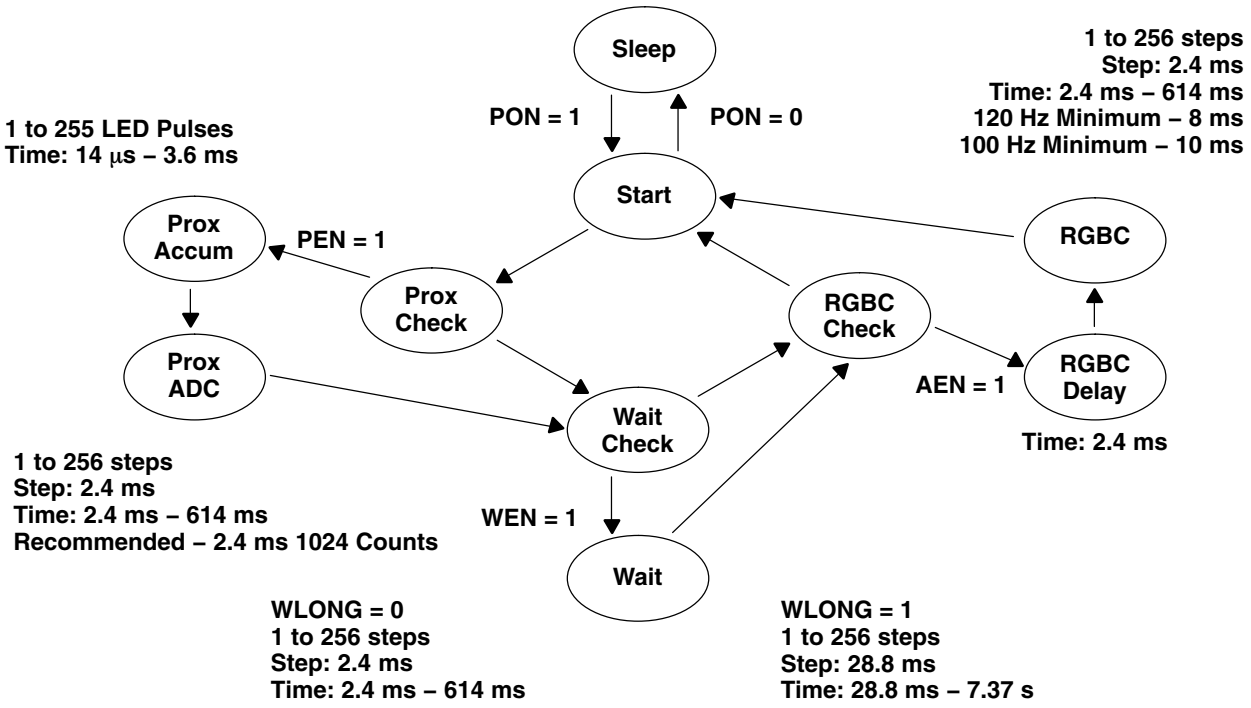


Figure 14. Expanded State Diagram

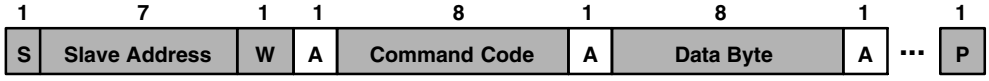
I²C Protocol

Interface and control are accomplished through an I²C serial compatible interface (standard or fast mode) to a set of registers that provide access to device control functions and output data. The devices support the 7-bit I²C addressing protocol.

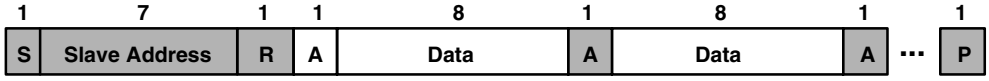
The I²C standard provides for three types of bus transaction: read, write, and a combined protocol (Figure 15). During a write operation, the first byte written is a command byte followed by data. In a combined protocol, the first byte written is the command byte followed by reading a series of bytes. If a read command is issued, the register address from the previous command will be used for data access. Likewise, if the MSB of the command is not set, the device will write a series of bytes at the address stored in the last valid command with a register address. The command byte contains either control information or a 5-bit register address. The control commands can also be used to clear interrupts.

The I²C bus protocol was developed by Philips (now NXP). For a complete description of the I²C protocol, please review the NXP I²C design specification at http://www.i2c–bus.org/references/.

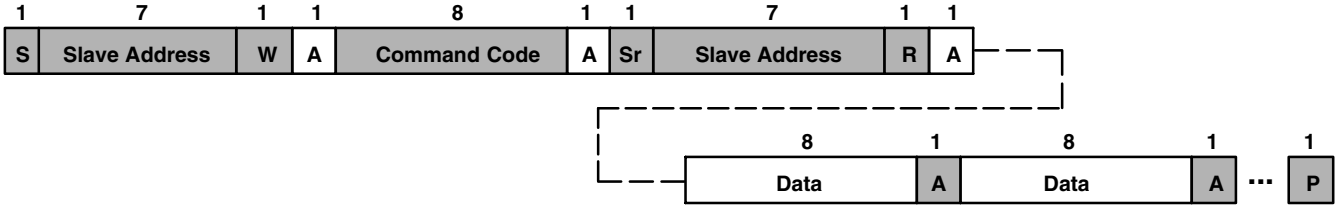
A Acknowledge (0)
N Not Acknowledged (1)
P Stop Condition
R Read (1)
S Start Condition
Sr Repeated Start Condition
W Write (0)
... Continuation of protocol
Master-to-Slave
Slave-to-Master



I²C Write Protocol



I²C Read Protocol



I²C Read Protocol — Combined Format

Figure 15. I²C Protocols

Register Set

The TCS3771 is controlled and monitored by data registers and a command register accessed through the serial interface. These registers provide for a variety of control functions and can be read to determine results of the ADC conversions. The register set is summarized in Table 1.

Table 1. Register Address

ADDRESS	RESISTER NAME	R/W	REGISTER FUNCTION	RESET VALUE
––	COMMAND	W	Specifies register address	0x00
0x00	ENABLE	R/W	Enables states and interrupts	0x00
0x01	ATIME	R/W	RGBC ADC time	0xFF
0x02	PTIME	R/W	Proximity ADC time	0xFF
0x03	WTIME	R/W	Wait time	0xFF
0x04	AILTL	R/W	RGBC interrupt low threshold low byte	0x00
0x05	AILTH	R/W	RGBC interrupt low threshold high byte	0x00
0x06	AIHTL	R/W	RGBC interrupt high threshold low byte	0x00
0x07	AIHTH	R/W	RGBC interrupt high threshold high byte	0x00
0x08	PILTL	R/W	Proximity interrupt low threshold low byte	0x00
0x09	PILTH	R/W	Proximity interrupt low threshold high byte	0x00
0x0A	PIHTL	R/W	Proximity interrupt high threshold low byte	0x00
0x0B	PIHTH	R/W	Proximity interrupt high threshold high byte	0x00
0x0C	PERS	R/W	Interrupt persistence filters	0x00
0x0D	CONFIG	R/W	Configuration	0x00
0x0E	PPCOUNT	R/W	Proximity pulse count	0x00
0x0F	CONTROL	R/W	Gain control register	0x00
0x12	ID	R	Device ID	ID
0x13	STATUS	R	Device status	0x00
0x14	CDATA	R	Clear ADC low data register	0x00
0x15	CDATAH	R	Clear ADC high data register	0x00
0x16	RDATA	R	Red ADC low data register	0x00
0x17	RDATAH	R	Red ADC high data register	0x00
0x18	GDATA	R	Green ADC low data register	0x00
0x19	GDATAH	R	Green ADC high data register	0x00
0x1A	BDATA	R	Blue ADC low data register	0x00
0x1B	BDATAH	R	Blue ADC high data register	0x00
0x1C	PDATA	R	Proximity ADC low data register	0x00
0x1D	PDATAH	R	Proximity ADC high data register	0x00

The mechanics of accessing a specific register depends on the specific protocol used. See the section on I^2C protocols on the previous pages. In general, the COMMAND register is written first to specify the specific control/status register for following read/write operations.

Command Register

The command registers specifies the address of the target register for future write and read operations.

Table 2. Command Register

	7	6	5	4	3	2	1	0	
COMMAND	COMMAND	TYPE		ADD					– –

FIELD	BITS	DESCRIPTION	
COMMAND	7	Select Command Register. Must write as 1 when addressing COMMAND register.	
TYPE	6:5	Selects type of transaction to follow in subsequent data transfers:	
		FIELD VALUE	**INTEGRATION TIME**
		00	Repeated byte protocol transaction
		01	Auto-increment protocol transaction
		10	Reserved — Do not use
		11	Special function — See description below
		Byte protocol will repeatedly read the same register with each data access. Block protocol will provide auto-increment function to read successive bytes.	
ADD	4:0	Address field/special function field. Depending on the transaction type, see above, this field either specifies a special function command or selects the specific control–status–register for following write and read transactions. The field values listed below apply only to special function commands:	
		FIELD VALUE	**READ VALUE**
		00000	Normal — no action
		00101	Proximity interrupt clear
		00110	RGBC interrupt clear
		00111	Proximity and RGBC interrupt clear
		other	Reserved — Do not write
		RGBC/Proximity Interrupt Clear. Clears any pending RGBC/Proximity interrupt. This special function is self clearing.	

Enable Register (0x00)

The Enable register is used primarily to power the TCS3771 device on and off, and enable functions and interrupts as shown in Table 3.

Table 3. Enable Register

	7	6	5	4	3	2	1	0	
ENABLE	**Reserved**		**PIEN**	**AIEN**	**WEN**	**PEN**	**AEN**	**PON**	**Address 0x00**

FIELD	BITS	DESCRIPTION
Reserved	7:6	Reserved. Write as 0.
PIEN	5	Proximity interrupt enable. When asserted, permits proximity interrupts to be generated.
AIEN	4	RGBC interrupt enable. When asserted, permits RGBC interrupts to be generated.
WEN	3	Wait enable. This bit activates the wait feature. Writing a 1 activates the wait timer. Writing a 0 disables the wait timer.
PEN	2	Proximity enable. This bit activates the proximity function. Writing a 1 enables proximity. Writing a 0 disables proximity.
AEN	1	RGBC enable. This bit actives the two-channel ADC. Writing a 1 activates the RGBC. Writing a 0 disables the RGBC.
PON [1]	0	Power ON. This bit activates the internal oscillator to permit the timers and ADC channels to operate. Writing a 1 activates the oscillator. Writing a 0 disables the oscillator. During reads and writes over the I^2C interface, this bit is temporarily overridden and the oscillator is enabled, independent of the state of PON.

NOTE 1: A minimum interval of 2.4 ms must pass after PON is asserted before either a proximity or an RGBC can be initiated. This required time is enforced by the hardware in cases where the firmware does not provide it.

RGBC Timing Register (0x01)

The RGBC timing register controls the internal integration time of the RGBC clear and IR channel ADCs in 2.4-ms increments.

Table 4. RGBC Timing Register

FIELD	BITS	DESCRIPTION			
ATIME	7:0	VALUE	INTEG_CYCLES	TIME	MAX COUNT
		0xFF	1	2.4 ms	1024
		0xF6	10	24 ms	10240
		0xD6	42	101 ms	43008
		0xAD	64	154 ms	65535
		0x00	256	614 ms	65535

Proximity Time Control Register (0x02)

The proximity timing register controls the integration time of the proximity ADC in 2.4 ms increments. It is recommended that this register be programmed to a value of 0xFF (1 cycle, 1023 bits).

$$\text{Max Prox Count} = ((256 - \text{PTIME}) \times 1024)) - 1 \quad \text{up to a maximum of } 65535$$

Table 5. Proximity Time Control Register

FIELD	BITS	DESCRIPTION			
PTIME	7:0	VALUE	INTEG_CYCLES	TIME	MAX COUNT
		0xFF	1	2.4 ms	1023

Wait Time Register (0x03)

Wait time is set 2.4 ms increments unless the WLONG bit is asserted in which case the wait times are 12× longer. WTIME is programmed as a 2's complement number.

Table 6. Wait Time Register

FIELD	BITS	DESCRIPTION			
WTIME	7:0	REGISTER VALUE	WAIT TIME	TIME (WLONG = 0)	TIME (WLONG = 1)
		0xFF	1	2.4 ms	0.029 sec
		0xAB	85	204 ms	2.45 sec
		0x00	256	614 ms	7.4 sec

RGBC Interrupt Threshold Registers (0x04 – 0x07)

The RGBC interrupt threshold registers provides the values to be used as the high and low trigger points for the comparison function for interrupt generation. If the value generated by the clear channel crosses below the lower threshold specified, or above the higher threshold, an interrupt is asserted on the interrupt pin.

Table 7. RGBC Interrupt Threshold Registers

REGISTER	ADDRESS	BITS	DESCRIPTION
AILTL	0x04	7:0	RGBC clear channel low threshold lower byte
AILTH	0x05	7:0	RGBC clear channel low threshold upper byte
AIHTL	0x06	7:0	RGBC clear channel high threshold lower byte
AIHTH	0x07	7:0	RGBC clear channel high threshold upper byte

Proximity Interrupt Threshold Registers (0x08 – 0x0B)

The proximity interrupt threshold registers provide the values to be used as the high and low trigger points for the comparison function for interrupt generation. If the value generated by proximity channel crosses below the lower threshold specified, or above the higher threshold, an interrupt is signaled to the host processor.

Table 8. Proximity Interrupt Threshold Registers

REGISTER	ADDRESS	BITS	DESCRIPTION
PILTL	0x08	7:0	Proximity ADC channel low threshold lower byte
PILTH	0x09	7:0	Proximity ADC channel low threshold upper byte
PIHTL	0x0A	7:0	Proximity ADC channel high threshold lower byte
PIHTH	0x0B	7:0	Proximity ADC channel high threshold upper byte

Persistence Register (0x0C)

The persistence register controls the filtering interrupt capabilities of the device. Configurable filtering is provided to allow interrupts to be generated after each integration cycle or if the integration has produced a result that is outside of the values specified by the threshold register for some specified amount of time. Separate filtering is provided for proximity and the RGBC clear channel.

Table 9. Persistence Register

	7	6	5	4	3	2	1	0	
PERS	PPERS				APERS				Address 0x0C

FIELD	BITS	DESCRIPTION		
PPERS	7:4	Proximity interrupt persistence. Controls rate of proximity interrupt to the host processor.		
		FIELD VALUE	MEANING	INTERRUPT PERSISTENCE FUNCTION
		0000	–––	Every proximity cycle generates an interrupt
		0001	1	1 proximity value out of range
		0010	2	2 consecutive proximity values out of range
		...	...	...
		1111	15	15 consecutive proximity values out of range
APERS	3:0	Interrupt persistence. Controls rate of interrupt to the host processor.		
		FIELD VALUE	MEANING	INTERRUPT PERSISTENCE FUNCTION
		0000	Every	Every RGBC cycle generates an interrupt
		0001	1	1 clear channel value outside of threshold range
		0010	2	2 clear channel consecutive values out of range
		0011	3	3 clear channel consecutive values out of range
		0100	5	5 clear channel consecutive values out of range
		0101	10	10 clear channel consecutive values out of range
		0110	15	15 clear channel consecutive values out of range
		0111	20	20 clear channel consecutive values out of range
		1000	25	25 clear channel consecutive values out of range
		1001	30	30 clear channel consecutive values out of range
		1010	35	35 clear channel consecutive values out of range
		1011	40	40 clear channel consecutive values out of range
		1100	45	45 clear channel consecutive values out of range
		1101	50	50 clear channel consecutive values out of range
		1110	55	55 clear channel consecutive values out of range
		1111	60	60 clear channel consecutive values out of range

Configuration Register (0x0D)

The configuration register sets the wait long time.

Table 10. Configuration Register

	7	6	5	4	3	2	1	0	
CONFIG	Reserved						WLONG	Reserved	Address 0x0D

FIELD	BITS	DESCRIPTION
Reserved	7:2	Reserved. Write as 0.
WLONG	1	Wait Long. When asserted, the wait cycles are increased by a factor 12× from that programmed in the WTIME register.
Reserved	0	Reserved. Write as 0.

Proximity Pulse Count Register (0x0E)

The proximity pulse count register sets the number of proximity pulses that will be transmitted. When proximity detection is enabled, a proximity detect cycle occurs after each RGBC cycle. PPULSE defines the number of pulses to be transmitted.

NOTE: The ATIME register will be used to time the interval between proximity detection events even if the RGBC function is disabled.

Table 11. Proximity Pulse Count Register

	7	6	5	4	3	2	1	0	
PPULSE	PPULSE								Address 0x0E

FIELD	BITS	DESCRIPTION
PPULSE	7:0	Proximity Pulse Count. Specifies the number of proximity pulses to be generated.

Control Register (0x0F)

The Control register provides eight bits of miscellaneous control to the analog block. These bits typically control functions such as gain settings and/or diode selection.

Table 12. Control Register

	7	6	5	4	3	2	1	0	
CONTROL	PDRIVE		PDIODE		Reserved		AGAIN		Address 0x0F

FIELD	BITS	DESCRIPTION	
PDRIVE	7:6	LED Drive Strength.	
		FIELD VALUE	LED STRENGTH
		00	100 mA
		01	50 mA
		10	25 mA
		11	12.5 mA
PDIODE	5:4	Proximity Diode Select.	
		FIELD VALUE	DIODE SELECTION
		00	Reserved
		01	Proximity uses the clear (broadband) diode
		10	Proximity uses the IR diode
		11	Proximity uses both the clear diode and the red diode
Reserved	3:2	Reserved. Write bits as 0	
AGAIN	1:0	RGBC Gain Control.	
		FIELD VALUE	RGBC GAIN VALUE
		00	1× gain
		01	4× gain
		10	16× gain
		11	60× gain

ID Register (0x12)

The ID Register provides the value for the part number. The ID register is a read-only register.

Table 13. ID Register

	7	6	5	4	3	2	1	0	
ID	ID								Address 0x12

FIELD	BITS	DESCRIPTION	
ID	7:0	Part number identification	0x18 = TCS37711 &TCS37715
			0x19 = TCS37713 & TCS37717

Status Register (0x13)

The Status Register provides the internal status of the device. This register is read only.

Table 14. Status Register

	7	6	5	4	3	2	1	0	
STATUS	Reserved		PINT	AINT	Reserved		PVALID	AVALID	Address 0x13

FIELD	BIT	DESCRIPTION
Reserved	7:6	Reserved.
PINT	5	Proximity Interrupt.
AINT	4	RGBC clear channel Interrupt.
Reserved	3:2	Reserved.
PVALID	1	Proximity Valid. Indicates that a RGBC cycle has completed since AEN was asserted.
AVALID	0	RGBC Valid. Indicates that the RGBC channels have completed an integration cycle.

RGBC Channel Data Registers (0x14 – 0x1B)

Clear, red, green, and blue data is stored as 16-bit values. To ensure the data is read correctly, a two-byte read I^2C transaction should be used with a read word protocol bit set in the command register. With this operation, when the lower byte register is read, the upper eight bits are stored into a shadow register, which is read by a subsequent read to the upper byte. The upper register will read the correct value even if additional ADC integration cycles end between the reading of the lower and upper registers.

Table 15. ADC Channel Data Registers

REGISTER	ADDRESS	BITS	DESCRIPTION
CDATA	0x14	7:0	Clear data low byte
CDATAH	0x15	7:0	Clear data high byte
RDATA	0x16	7:0	Red data low byte
RDATAH	0x17	7:0	Red data high byte
GDATA	0x18	7:0	Green data low byte
GDATAH	0x19	7:0	Green data high byte
BDATA	0x1A	7:0	Blue data low byte
BDATAH	0x1B	7:0	Blue data high byte

Proximity Data Registers (0x1C – 0x1D)

Proximity data is stored as a 16-bit value. To ensure the data is read correctly, a two-byte read I^2C transaction should be used with a read word protocol bit set in the command register. With this operation, when the lower byte register is read, the upper eight bits are stored into a shadow register, which is read by a subsequent read to the upper byte. The upper register will read the correct value even if additional ADC integration cycles end between the reading of the lower and upper registers.

Table 16. PDATA Registers

REGISTER	ADDRESS	BITS	DESCRIPTION
PDATA	0x1C	7:0	Proximity data low byte
PDATAH	0x1D	7:0	Proximity data high byte

APPLICATION INFORMATION: HARDWARE

LED Driver Pin with Proximity Detection

In a proximity sensing system, the IR LED can be pulsed by the TCS3771 with more than 100 mA of rapidly switching current, therefore, a few design considerations must be kept in mind to get the best performance. The key goal is to reduce the power supply noise coupled back into the device during the LED pulses.

The first recommendation is to use two power supplies; one for the device V_{DD} and the other for the IR LED. In many systems, there is a quiet analog supply and a noisy digital supply. By connecting the quiet supply to the V_{DD} pin and the noisy supply to the LED, the key goal can be meet. Place a 1-μF low-ESR decoupling capacitor as close as possible to the V_{DD} pin and another at the LED anode, and a 22-μF capacitor at the output of the LED voltage regulator to supply the 100-mA current surge.

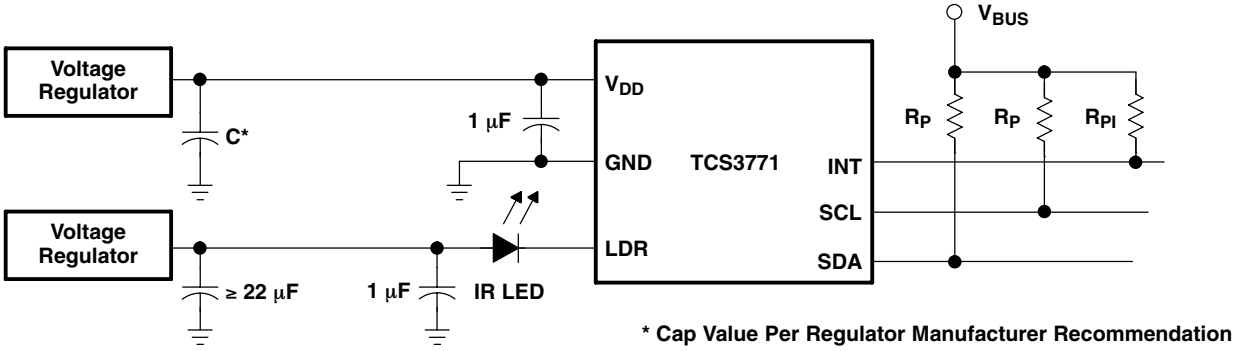


Figure 16. Proximity Sensing Using Separate Power Supplies

If it is not possible to provide two separate power supplies, the device can be operated from a single supply. A 22-Ω resistor in series with the V_{DD} supply line and a 1-μF low ESR capacitor effectively filter any power supply noise. The previous capacitor placement considerations apply.

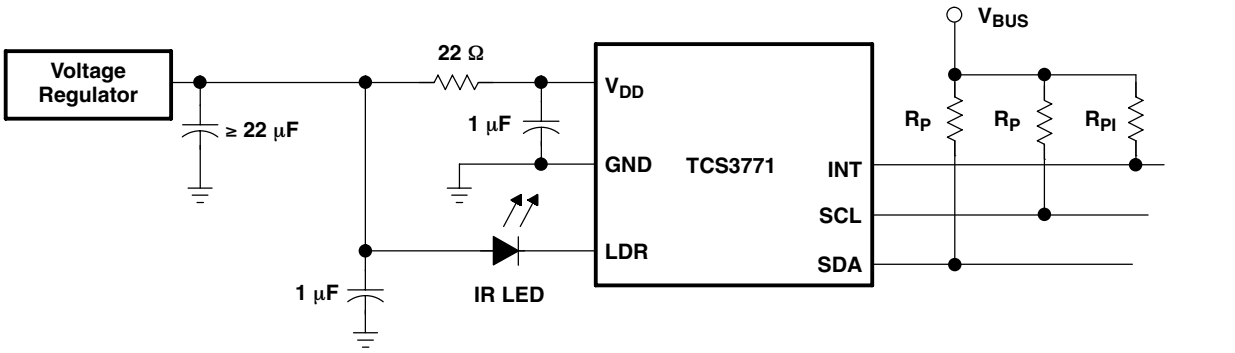


Figure 17. Proximity Sensing Using Single Power Supply

V_{BUS} in the above figures refers to the I^2C bus voltage which is either V_{DD} or 1.8 V. Be sure to apply the specified I^2C bus voltage shown in the Available Options table for the specific device being used.

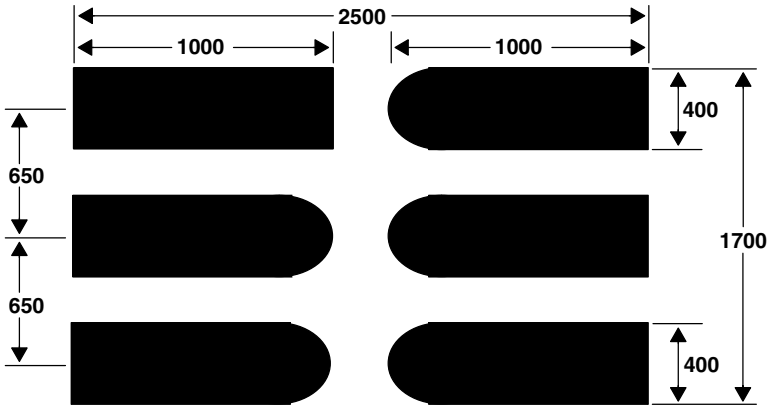
The I^2C signals and the Interrupt are open-drain outputs and require pull–up resistors. The pull-up resistor (R_P) value is a function of the I^2C bus speed, the I^2C bus voltage, and the capacitive load. The TAOS EVM running at 400 kbps, uses 1.5-kΩ resistors. A 10-kΩ pull-up resistor (R_{PI}) can be used for the interrupt line.

APPLICATION INFORMATION: HARDWARE

PCB Pad Layout

Suggested PCB pad layout guidelines for the Dual Flat No-Lead (FN) surface mount package are shown in Figure 18.

Note: Pads can be extended further if hand soldering is needed.

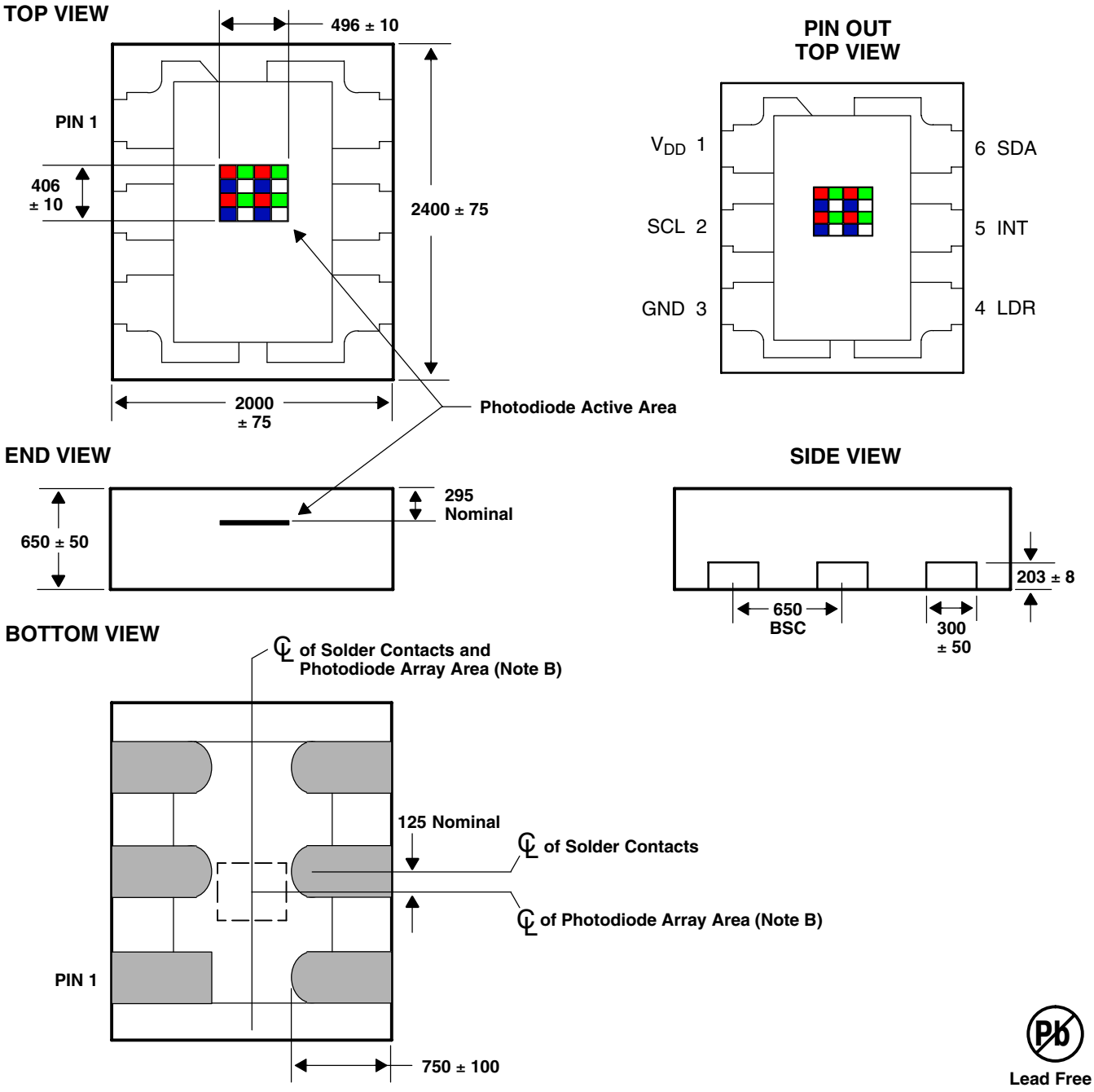


NOTES: A. All linear dimensions are in micrometers.
B. This drawing is subject to change without notice.

Figure 18. Suggested FN Package PCB Layout

MECHANICAL DATA

PACKAGE FN — **Dual Flat No-Lead**



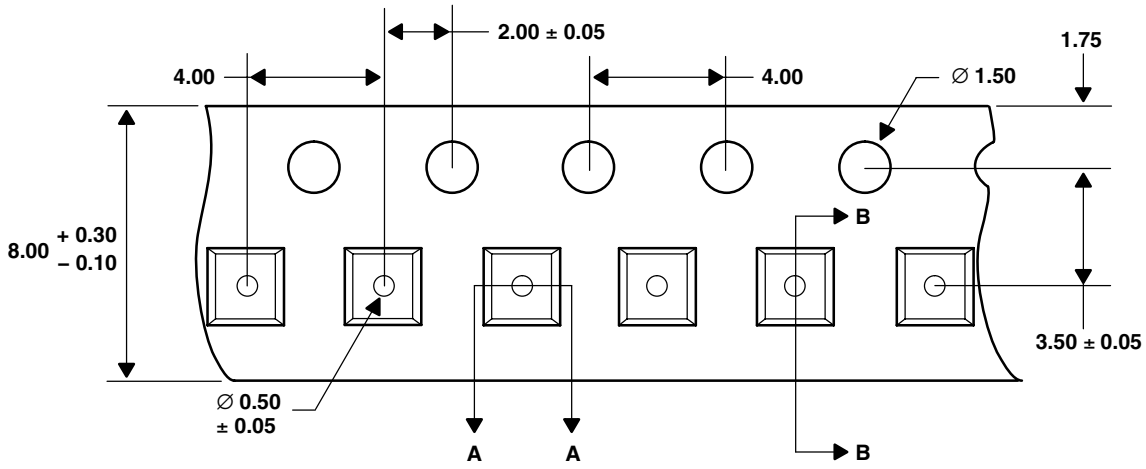
Lead Free

NOTES: A. All linear dimensions are in micrometers.
B. The die is centered within the package within a tolerance of ± 75 µm.
C. Package top surface is molded with an electrically nonconductive clear plastic compound having an index of refraction of 1.55.
D. Contact finish is copper alloy A194 with pre-plated NiPdAu lead finish.
E. This package contains no lead (Pb).
F. This drawing is subject to change without notice.

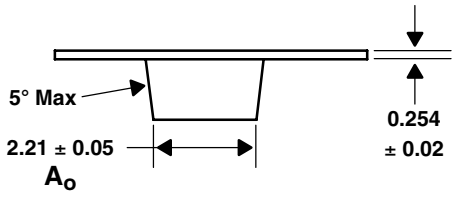
Figure 19. Package FN — Dual Flat No-Lead Packaging Configuration

MECHANICAL DATA

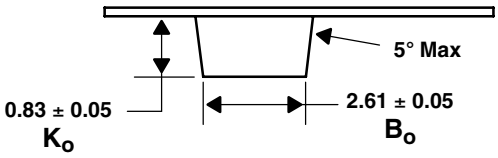
TOP VIEW

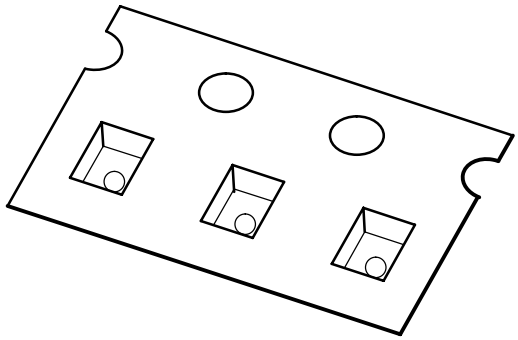


DETAIL A



DETAIL B





NOTES: A. All linear dimensions are in millimeters. Dimension tolerance is ± 0.10 mm unless otherwise noted.
B. The dimensions on this drawing are for illustrative purposes only. Dimensions of an actual carrier may vary slightly.
C. Symbols on drawing A_o, B_o, and K_o are defined in ANSI EIA Standard 481–B 2001.
D. Each reel is 178 millimeters in diameter and contains 3500 parts.
E. TAOS packaging tape and reel conform to the requirements of EIA Standard 481–B.
F. In accordance with EIA standard, device pin 1 is located next to the sprocket holes in the tape.
G. This drawing is subject to change without notice.

Figure 20. Package FN Carrier Tape

MANUFACTURING INFORMATION

The FN package has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate.

The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

Table 17. Solder Reflow Profile

PARAMETER	REFERENCE	TCS3771
Average temperature gradient in preheating		2.5°C/sec
Soak time	t_{soak}	2 to 3 minutes
Time above 217°C (T1)	t_1	Max 60 sec
Time above 230°C (T2)	t_2	Max 50 sec
Time above T_{peak} –10°C (T3)	t_3	Max 10 sec
Peak temperature in reflow	T_{peak}	260°C
Temperature gradient in cooling		Max –5°C/sec

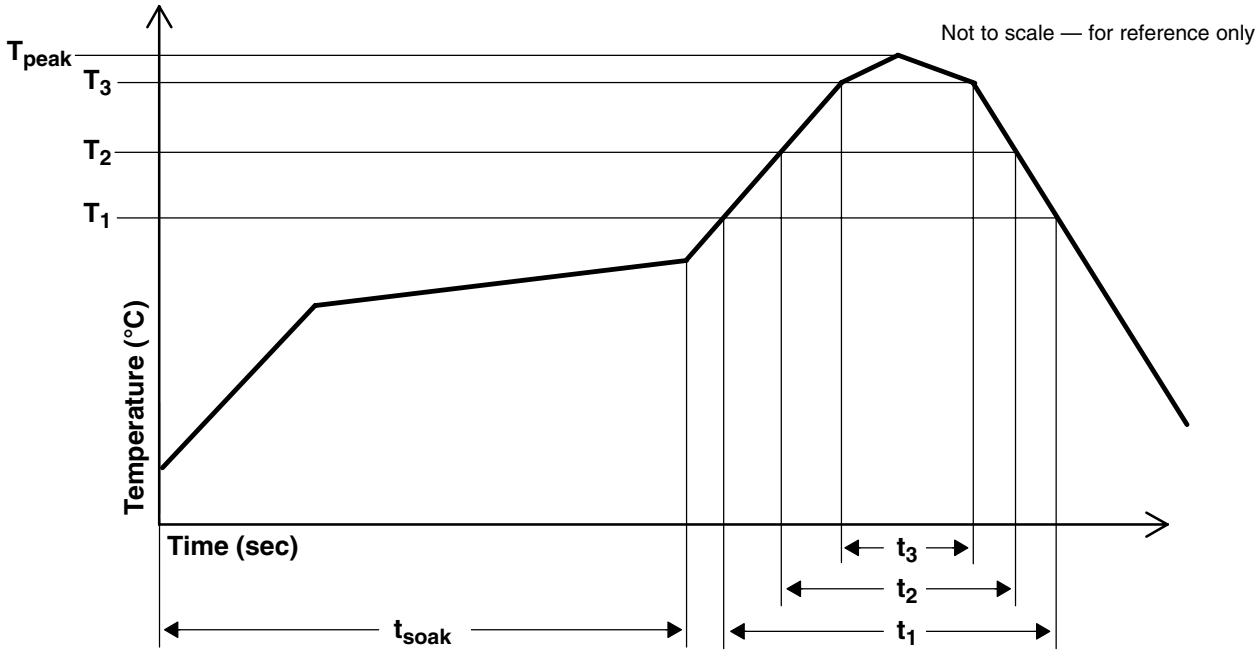


Figure 21. Solder Reflow Profile Graph

MANUFACTURING INFORMATION

Moisture Sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package. To ensure the package contains the smallest amount of absorbed moisture possible, each device is dry-baked prior to being packed for shipping. Devices are packed in a sealed aluminized envelope called a moisture barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

The FN package has been assigned a moisture sensitivity level of MSL 3 and the devices should be stored under the following conditions:

Temperature Range	5°C to 50°C
Relative Humidity	60% maximum
Total Time	12 months from the date code on the aluminized envelope — if unopened
Opened Time	168 hours or fewer

Rebaking will be required if the devices have been stored unopened for more than 12 months or if the aluminized envelope has been open for more than 168 hours. If rebaking is required, it should be done at 50°C for 12 hours.

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