ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage [1]	6	V
V_i	Input Voltage [2]	G_{ND} to V_{CC}	V
T_{oper}	Operating Free Air Temperature Range	-40 to + 85	°C
T_{stg}	Storage Temperature	-65 to +150	°C
T_j	Maximum Junction Temperature	150	°C
R_{thja}	Thermal Resistance Junction to Ambient [3] SO8 MiniSO8	 175 215	°C/W
Pd	Power Dissipation [4]	See the power derating curves Fig 20.	
ESD	Human Body Model	2	kV
ESD	Machine Model	200	V
Latch-up	Latch-up Immunity	Class A	
	Lead Temperature (soldering, 10sec)	250	°C

1. All voltages values are measured with respect to the ground pin.
2. The magnitude of input signal must never exceed V_{CC} + 0.3V / G_{ND} - 0.3V
3. Device is protected in case of over temperature by a thermal shutdown active @ 150°C.
4. Exceeding the power derating curves during a long period, will cause abnormal operation.

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2.2 to 5.5	V
V_{ICM}	Common Mode Input Voltage Range	G_{ND} to V_{CC} - 1.5V	V
V_{STB}	Standby Voltage Input : Device ON Device OFF	 $1.5 \leq V_{STB} \leq V_{CC}$ $GND \leq V_{STB} \leq 0.5$	V
R_L	Load Resistor	4 - 32	Ω
R_{thja}	Thermal Resistance Junction to Ambient [1] SO8 MiniSO8	 150 190	°C/W

1. This thermal resistance can be reduced with a suitable PCB layout (see Power Derating Curves)

ELECTRICAL CHARACTERISTICS

V_{CC} = **+5V**, GND = **0V**, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		6	8	mA
$I_{STANDBY}$	Standby Current [1] No input signal, Vstdby = GND, RL = 8Ω		10	1000	nA
Voo	Output Offset Voltage No input signal, RL = 8Ω		5	20	mV
Po	Output Power THD = 1% Max, f = 1kHz, RL = 8Ω		0.7		W
THD + N	Total Harmonic Distortion + Noise Po = 250mW rms, Gv = 2, 20Hz < f < 20kHz, RL = 8Ω		0.15		%
PSRR	Power Supply Rejection Ratio [2] f = 217Hz, RL = 8Ω, RFeed = 22KΩ, Vripple = 200mV rms		77		dB
Φ_M	Phase Margin at Unity Gain R_L = 8Ω, C_L = 500pF		70		Degrees
GM	Gain Margin R_L = 8Ω, C_L = 500pF		20		dB
GBP	Gain Bandwidth Product R_L = 8Ω		2		MHz

1. Standby mode is actived when Vstdby is tied to GND
2. Dynamic measurements - 20*log(rms(Vout)/rms(Vripple)). Vripple is the surimposed sinus signal to Vcc @ f = 217Hz

V_{CC} = **+3.3V**, GND = **0V**, T_{amb} = 25°C (unless otherwise specified)[3]

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		5.5	8	mA
$I_{STANDBY}$	Standby Current [1] No input signal, Vstdby = GND, RL = 8Ω		10	1000	nA
Voo	Output Offset Voltage No input signal, RL = 8Ω		5	20	mV
Po	Output Power THD = 1% Max, f = 1kHz, RL = 8Ω		300		mW
THD + N	Total Harmonic Distortion + Noise Po = 250mW rms, Gv = 2, 20Hz < f < 20kHz, RL = 8Ω		0.15		%
PSRR	Power Supply Rejection Ratio [2] f = 217Hz, RL = 8Ω, RFeed = 22KΩ, Vripple = 200mV rms		77		dB
Φ_M	Phase Margin at Unity Gain R_L = 8Ω, C_L = 500pF		70		Degrees
GM	Gain Margin R_L = 8Ω, C_L = 500pF		20		dB
GBP	Gain Bandwidth Product R_L = 8Ω		2		MHz

1. Standby mode is actived when Vstdby is tied to GND
2. Dynamic measurements - 20*log(rms(Vout)/rms(Vripple)). Vripple is the surimposed sinus signal to Vcc @ f = 217Hz
3. All electrical values are made by correlation between 2.6V and 5V measurements

ELECTRICAL CHARACTERISTICS

V_{CC} = **2.6V**, GND = **0V**, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		5.5	8	mA
$I_{STANDBY}$	Standby Current [1] No input signal, Vstdby = GND, RL = 8Ω		10	1000	nA
Voo	Output Offset Voltage No input signal, RL = 8Ω		5	20	mV
Po	Output Power THD = 1% Max, f = 1kHz, RL = 8Ω		180		mW
THD + N	Total Harmonic Distortion + Noise Po = 200mW rms, Gv = 2, 20Hz < f < 20kHz, RL = 8Ω		0.15		%
PSRR	Power Supply Rejection Ratio [2] f = 217Hz, RL = 8Ω, RFeed = 22KΩ, Vripple = 200mV rms		77		dB
Φ_M	Phase Margin at Unity Gain R_L = 8Ω, C_L = 500pF		70		Degrees
GM	Gain Margin R_L = 8Ω, C_L = 500pF		20		dB
GBP	Gain Bandwidth Product R_L = 8Ω		2		MHz

1. Standby mode is actived when Vstdby is tied to GND
2. Dynamic measurements - 20*log(rms(Vout)/rms(Vripple)). Vripple is the surimposed sinus signal to Vcc @ f = 217Hz

Components	Functional Description
Rin	Inverting input resistor which sets the closed loop gain in conjunction with Rfeed. This resistor also forms a high pass filter with Cin (fc = 1 / (2 x Pi x Rin x Cin))
Cin	Input coupling capacitor which blocks the DC voltage at the amplifier input terminal
Rfeed	Feed back resistor which sets the closed loop gain in conjunction with Rin
Cs	Supply Bypass capacitor which provides power supply filtering
Cb	Bypass pin capacitor which provides half supply filtering
Cfeed	Low pass filter capacitor allowing to cut the high frequency (low pass filter cut-off frequency 1 / (2 x Pi x Rfeed x Cfeed))
Rstb	Pull-up resistor which fixes the right supply level on the standby pin
Gv	Closed loop gain in BTL configuration = 2 x (Rfeed / Rin)

REMARKS

1. All measurements, except PSRR measurements, are made with a supply bypass capacitor Cs = 100µF.

2. The standby response time is about 1µs.

Fig. 1 : Open Loop Frequency Response

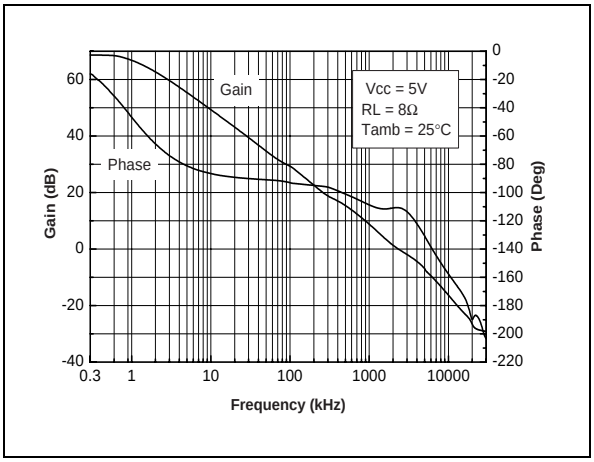


Fig. 2 : Open Loop Frequency Response

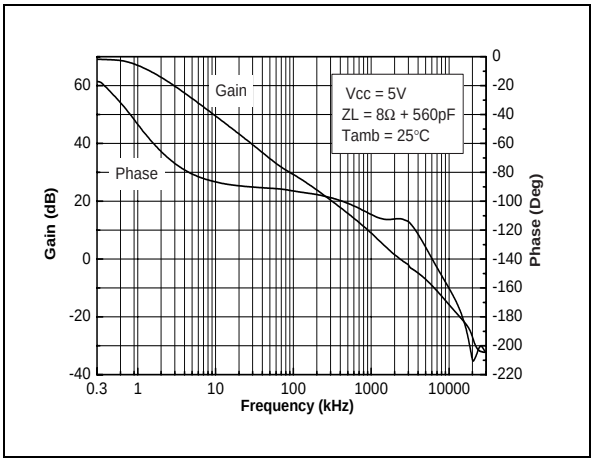


Fig. 3 : Open Loop Frequency Response

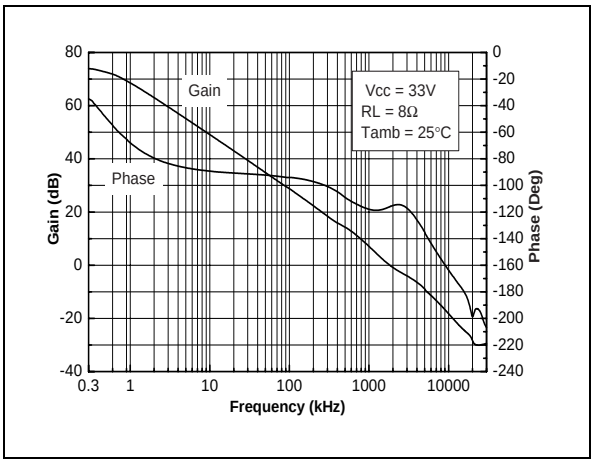


Fig. 4 : Open Loop Frequency Response

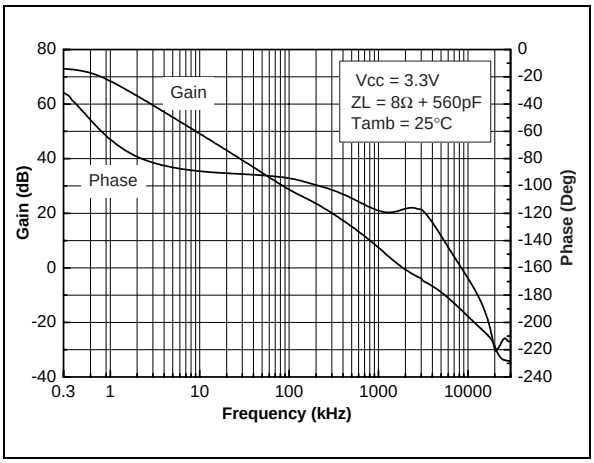


Fig. 5 : Open Loop Frequency Response

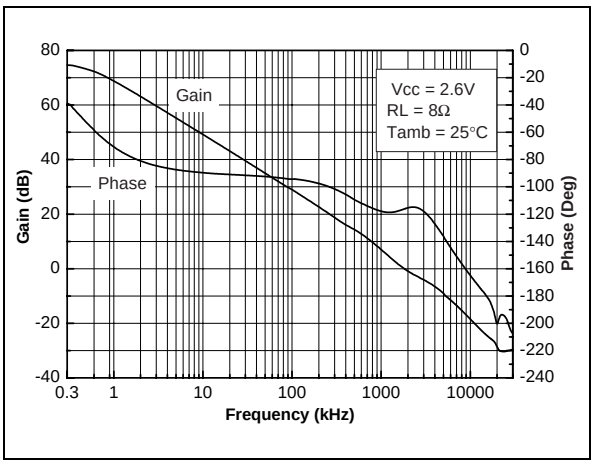


Fig. 6 : Open Loop Frequency Response

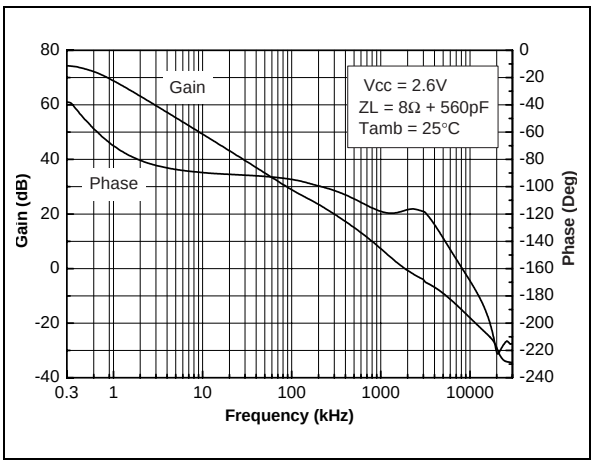


Fig. 7 : Open Loop Frequency Response

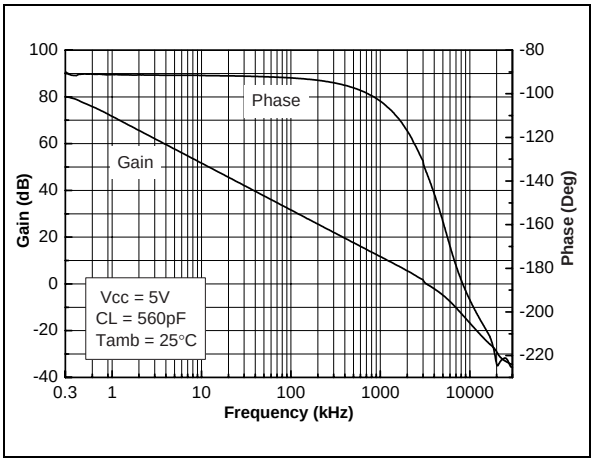


Fig. 8 : Open Loop Frequency Response

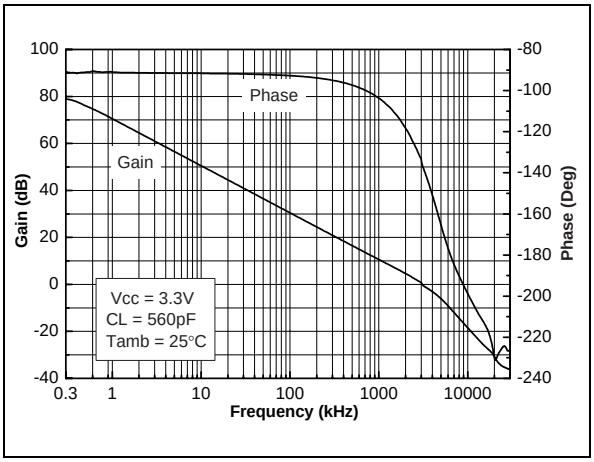


Fig. 9 : Open Loop Frequency Response

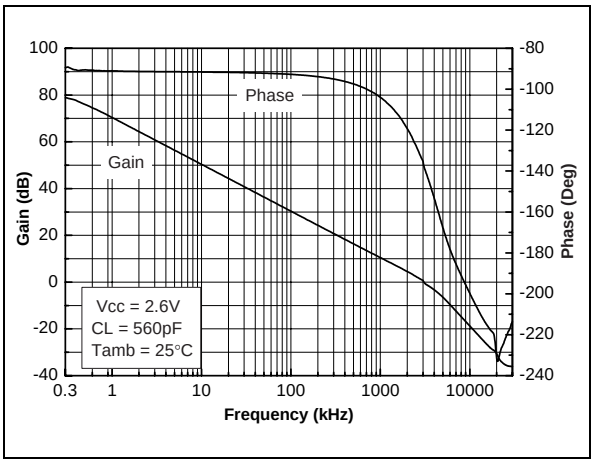


Fig. 10 : Power Supply Rejection Ratio (PSRR) vs Power supply

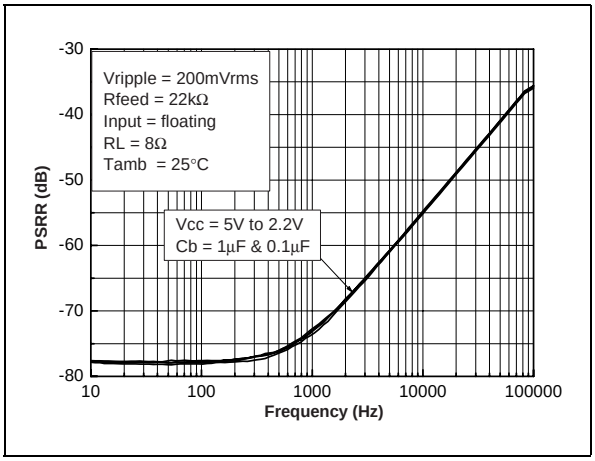


Fig. 11 : Power Supply Rejection Ratio (PSRR) vs Feedback Capacitor

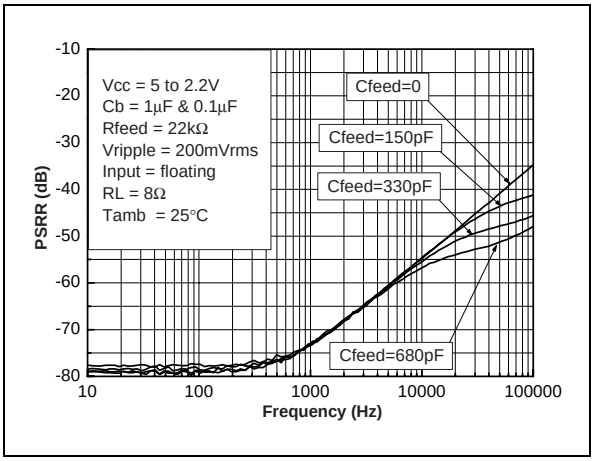


Fig. 12 : Power Supply Rejection Ratio (PSRR) vs Bypass Capacitor

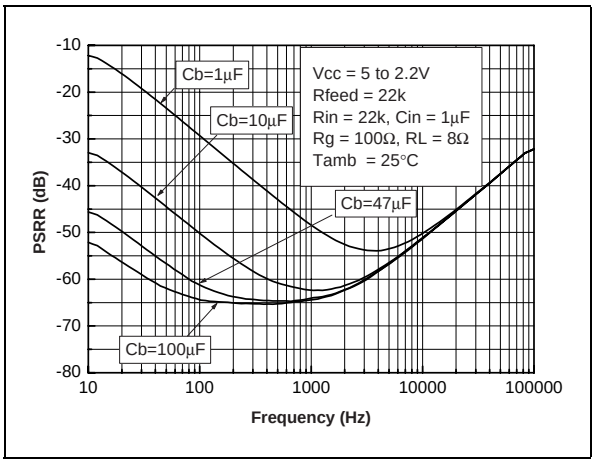


Fig. 13 : Power Supply Rejection Ratio (PSRR) vs Input Capacitor

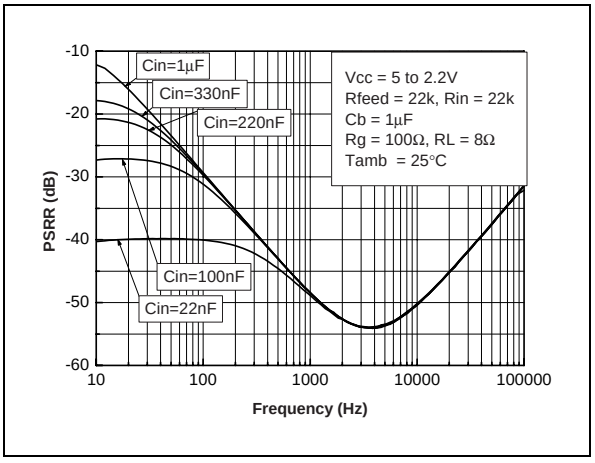


Fig. 14 : Power Supply Rejection Ratio (PSRR) vs Feedback Resistor

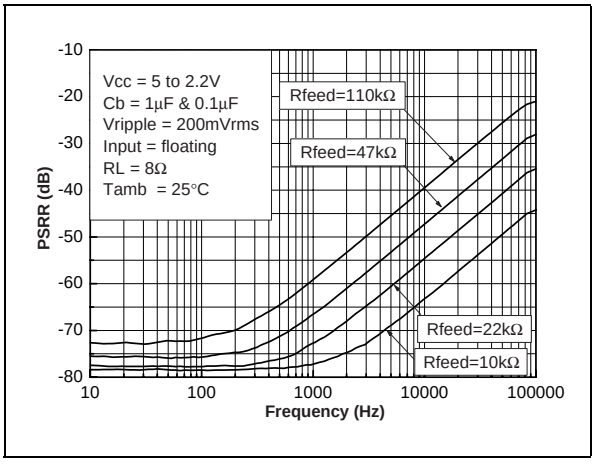


Fig. 15 : Pout @ THD + N = 1% vs Supply Voltage vs RL

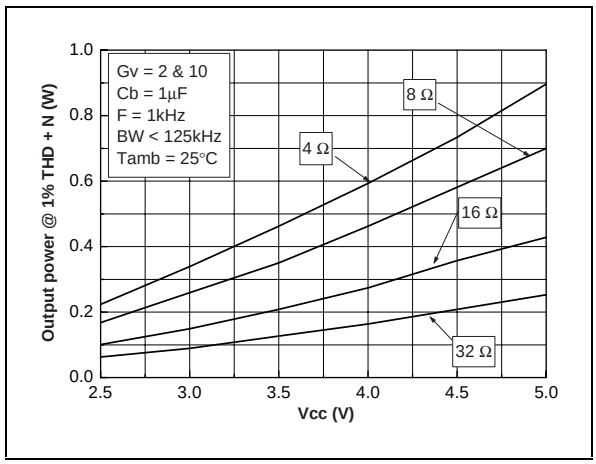


Fig. 16 : Pout @ THD + N = 10% vs Supply Voltage vs RL

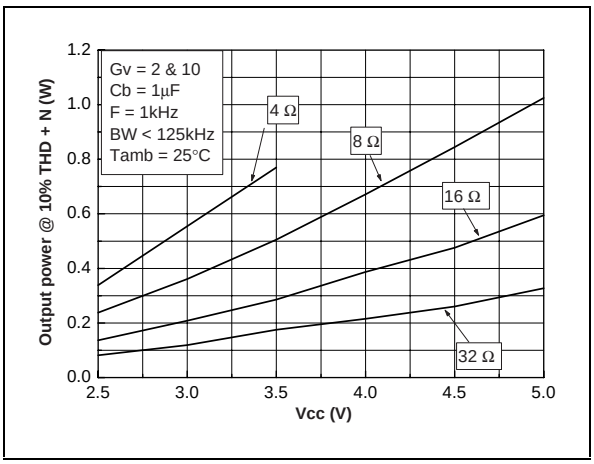


Fig. 17 : Power Dissipation vs Pout

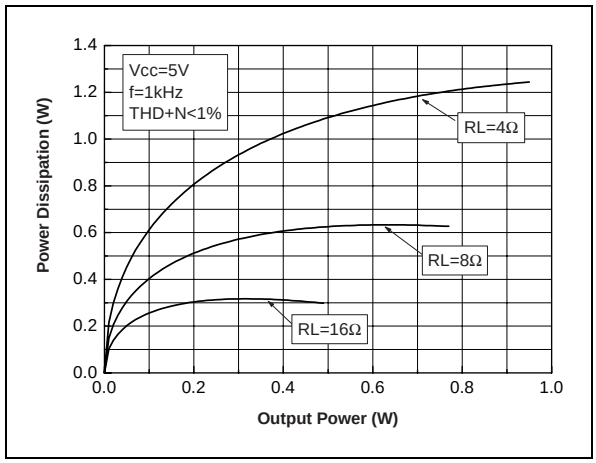


Fig. 18 : Power Dissipation vs Pout

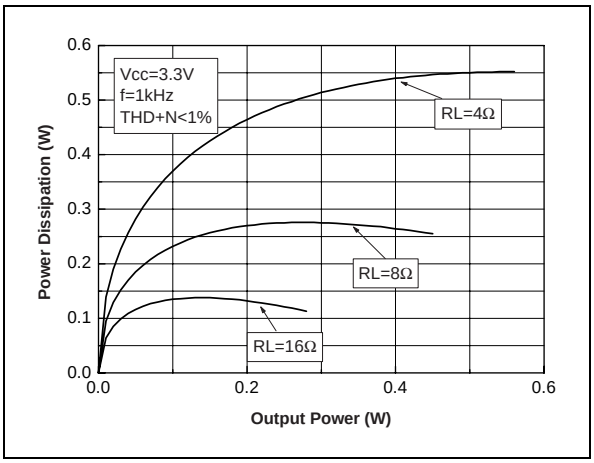


Fig. 19 : Power Dissipation vs Pout

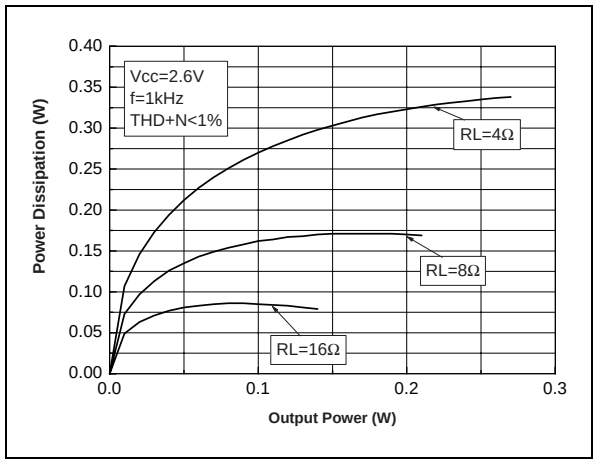


Fig. 20 : Power Derating Curves

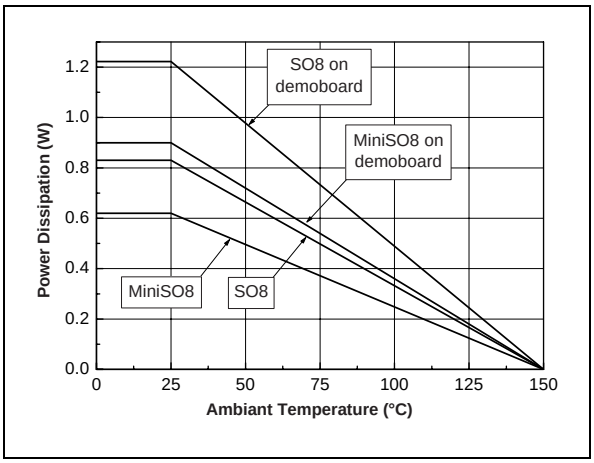


Fig. 21 : Output Power vs Load Resistance

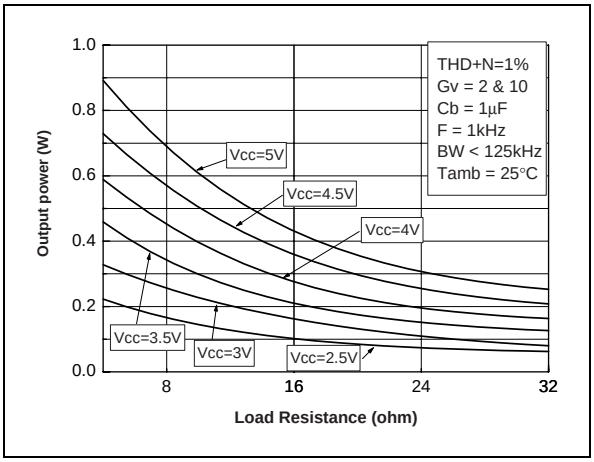


Fig. 22 : Output Power vs Load Resistance

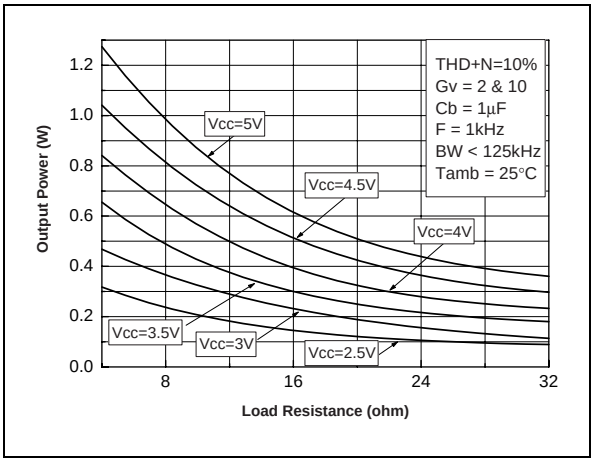


Fig. 23 : Clipping Voltage vs Supply Voltage

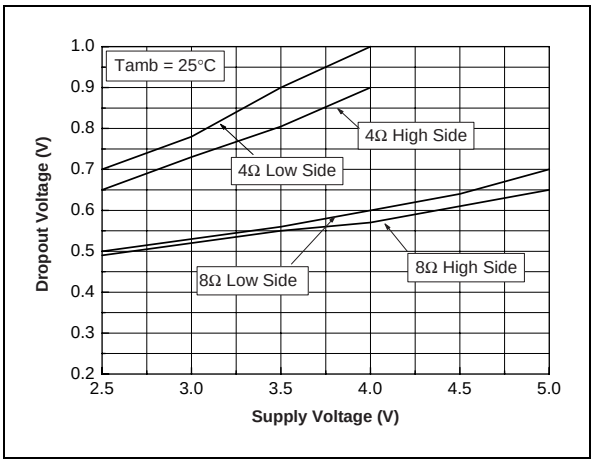


Fig. 24 : Frequency response vs Cin & Cfeed

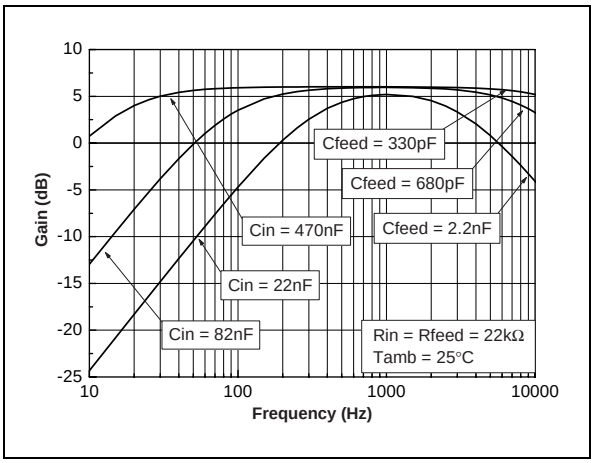


Fig. 25 : Noise Floor

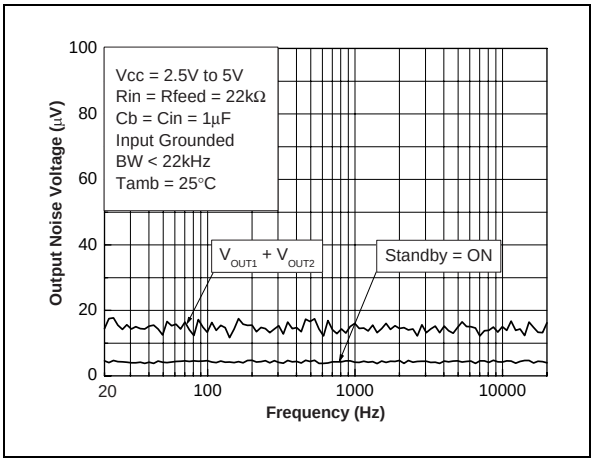


Fig. 26 : THD + N vs Output Power

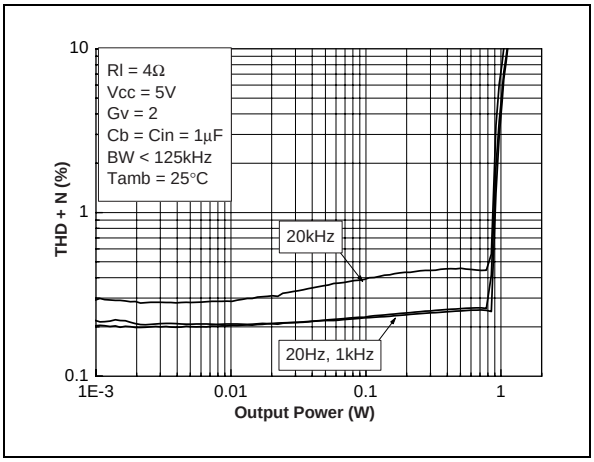


Fig. 27 : THD + N vs Output Power

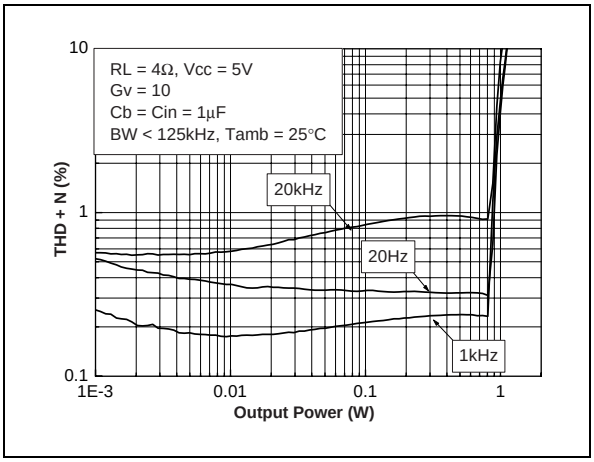


Fig. 28 : THD + N vs Output Power

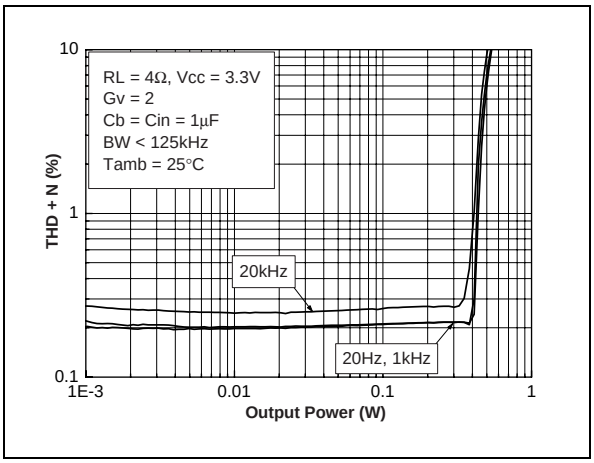


Fig. 29 : THD + N vs Output Power

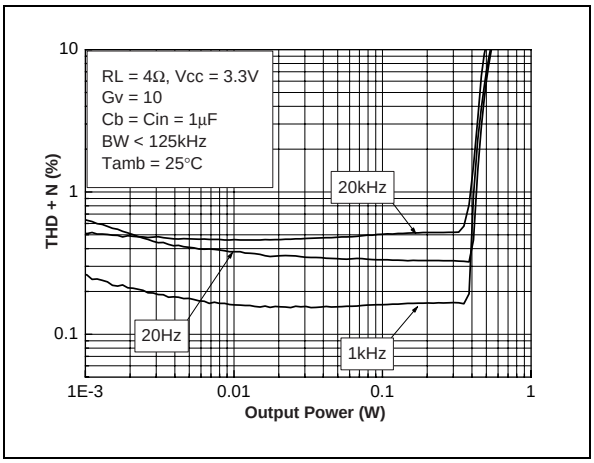


Fig. 30 : THD + N vs Output Power

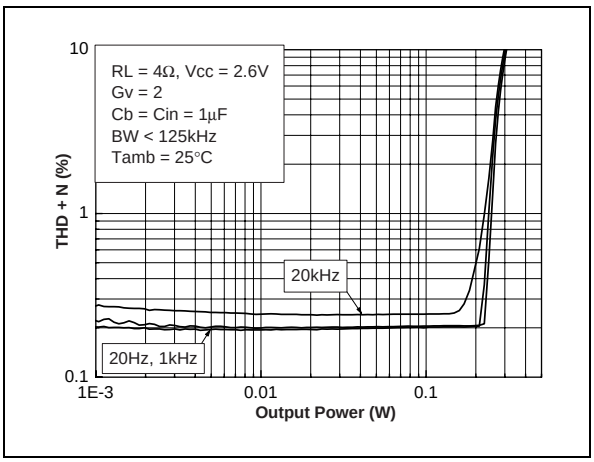


Fig. 31 : THD + N vs Output Power

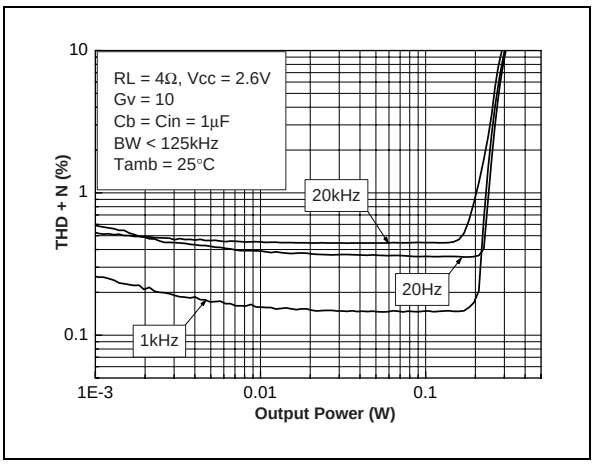


Fig. 32 : THD + N vs Output Power

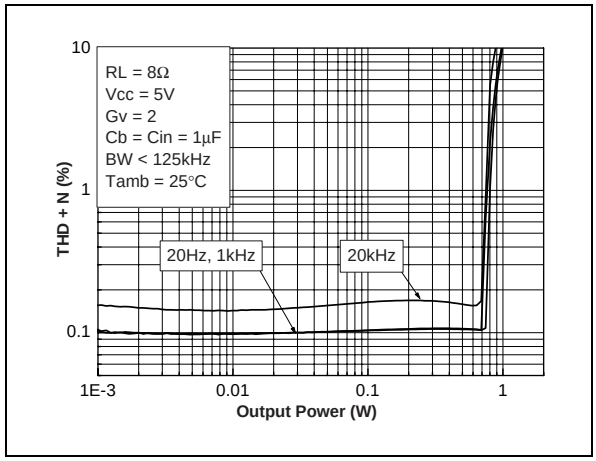


Fig. 33 : THD + N vs Output Power

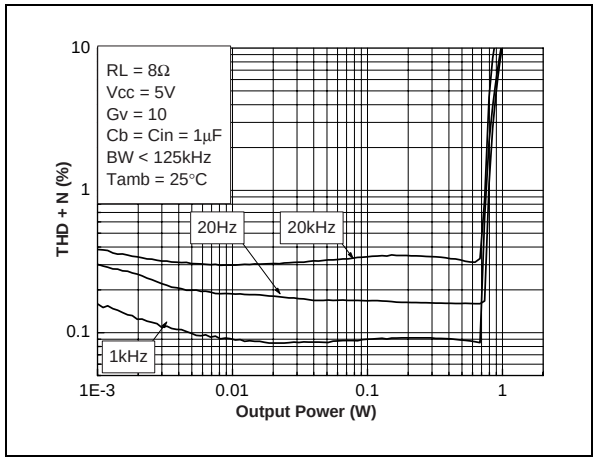


Fig. 34 : THD + N vs Output Power

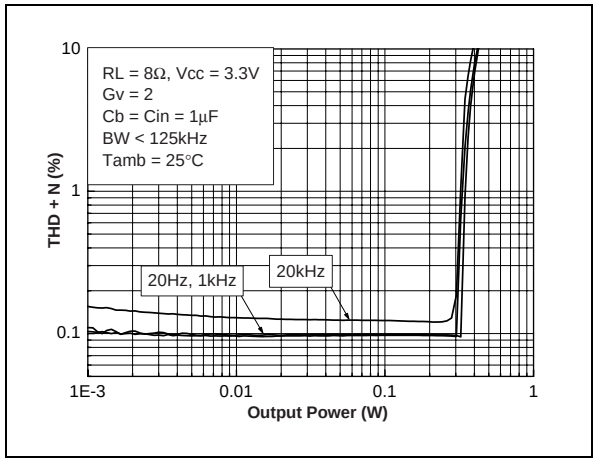


Fig. 35 : THD + N vs Output Power

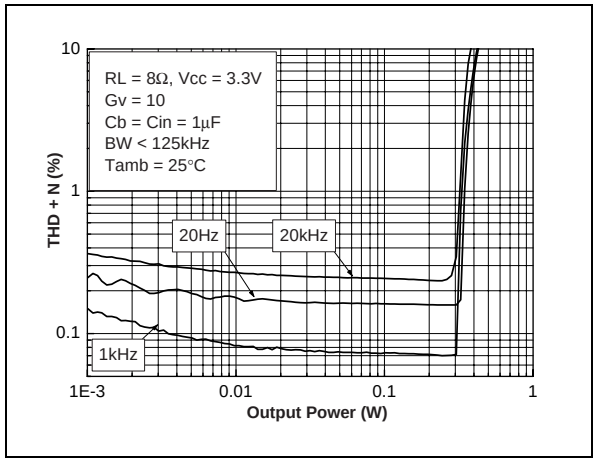


Fig. 36 : THD + N vs Output Power

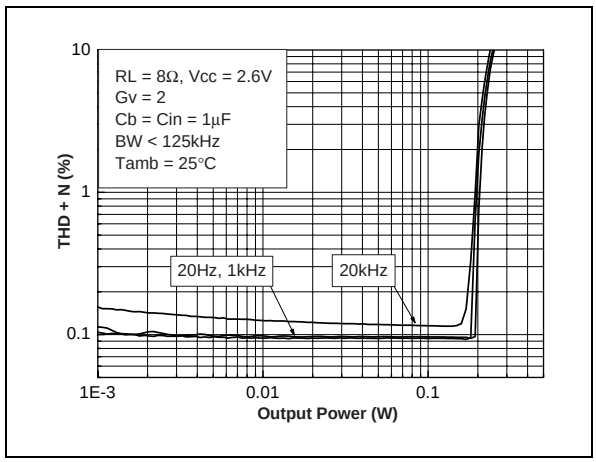


Fig. 37 : THD + N vs Output Power

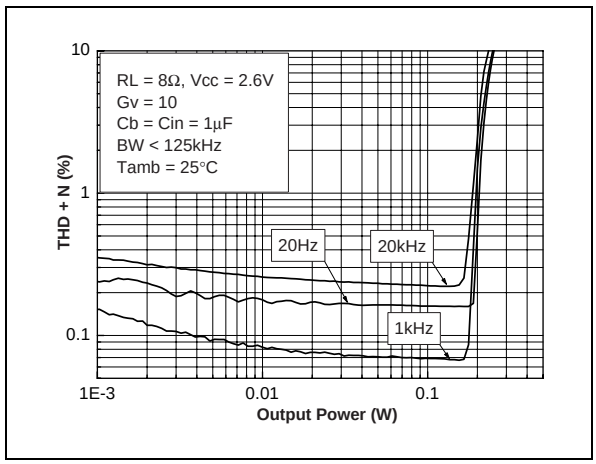


Fig. 38 : THD + N vs Output Power

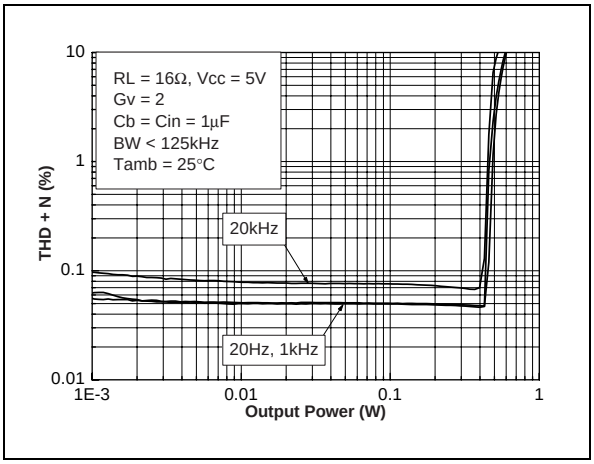


Fig. 39 : THD + N vs Output Power

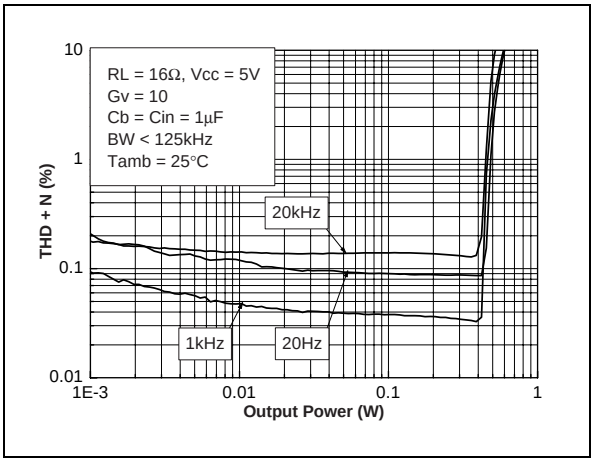


Fig. 40 : THD + N vs Output Power

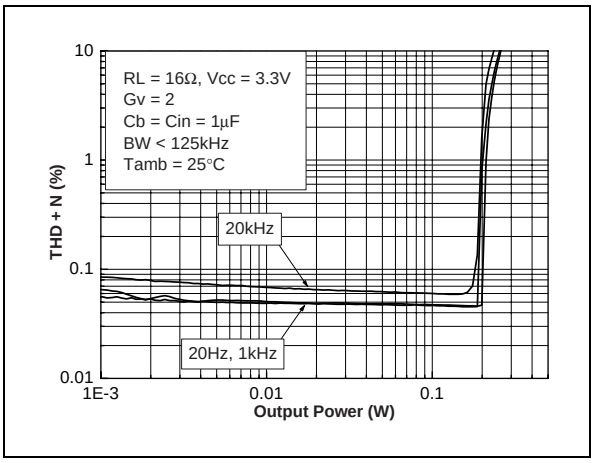


Fig. 41 : THD + N vs Output Power

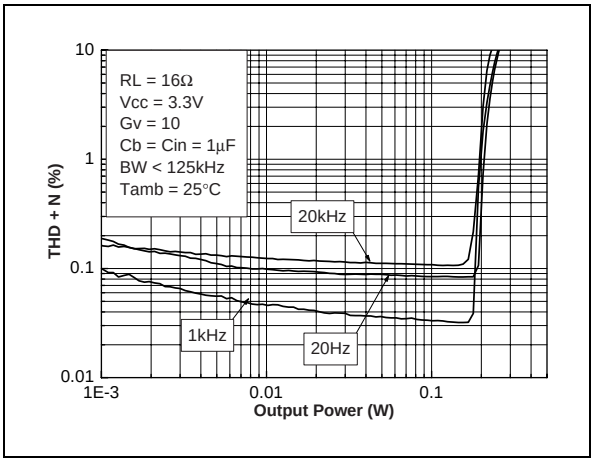


Fig. 42 : THD + N vs Output Power

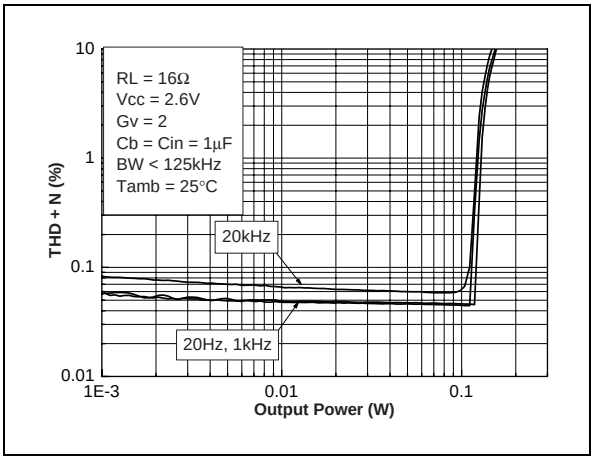


Fig. 43 : THD + N vs Output Power

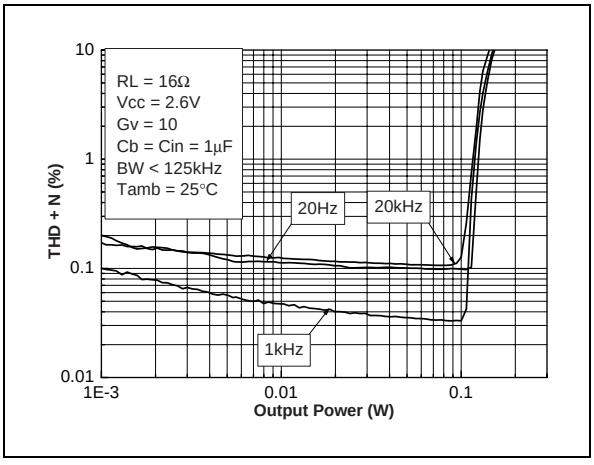


Fig. 44 : Signal to Noise Ratio vs Power Supply with Unweighted Filter (20Hz to 20kHz)

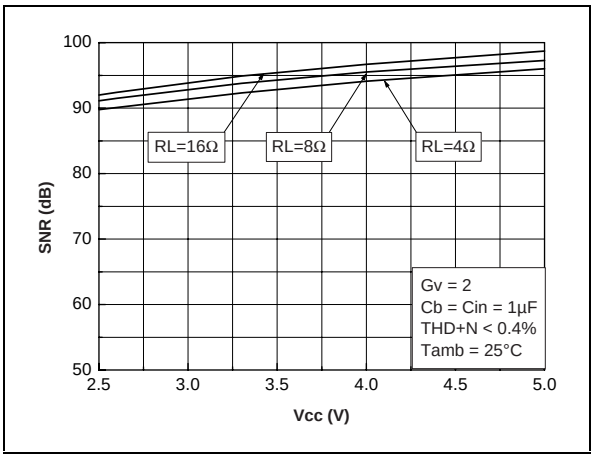


Fig. 45 : Signal to Noise Ratio Vs Power Supply with Unweighted Filter (20Hz to 20kHz)

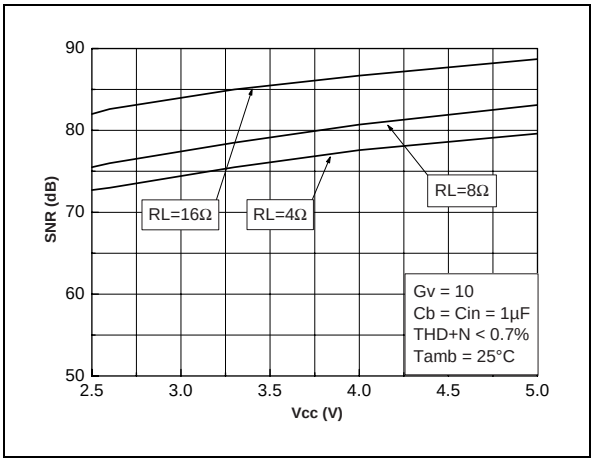


Fig. 46 : Signal to Noise Ratio vs Power Supply with Weighted Filter type A

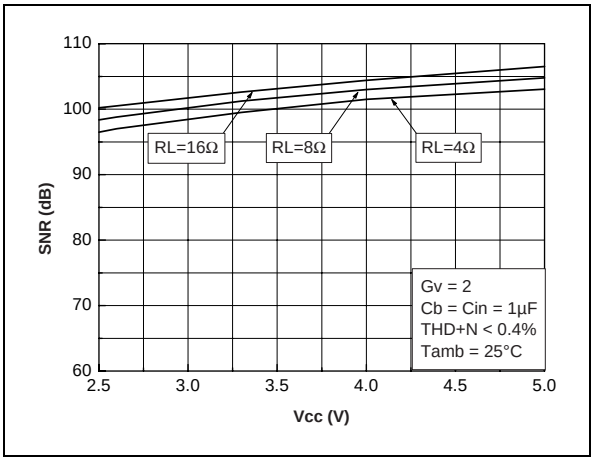


Fig. 47 : Signal to Noise Ratio vs Power Supply with Weighted Filter Type A

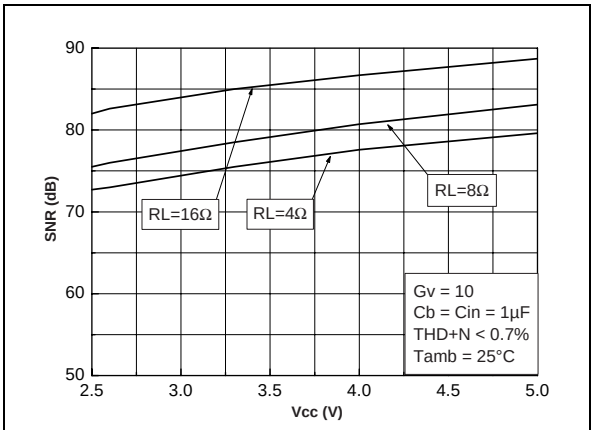


Fig. 48 : Current Consumption vs Power Supply Voltage

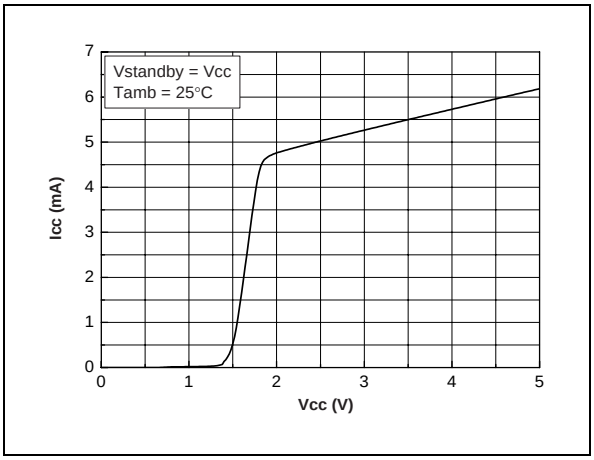


Fig. 49 : Current Consumption vs Standby Voltage @ Vcc = 5V

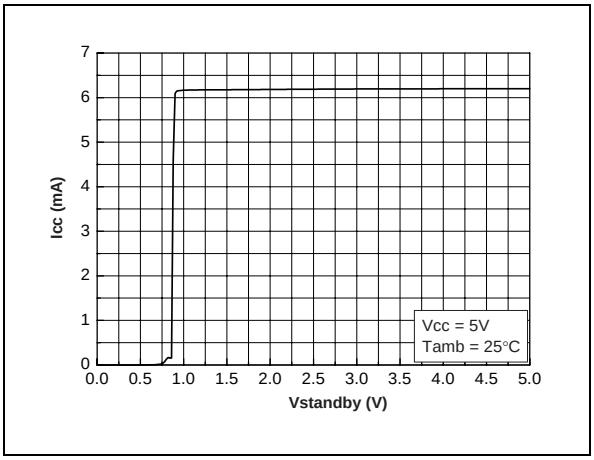


Fig. 50 : Current Consumption vs Standby Voltage @ Vcc = 3.3V

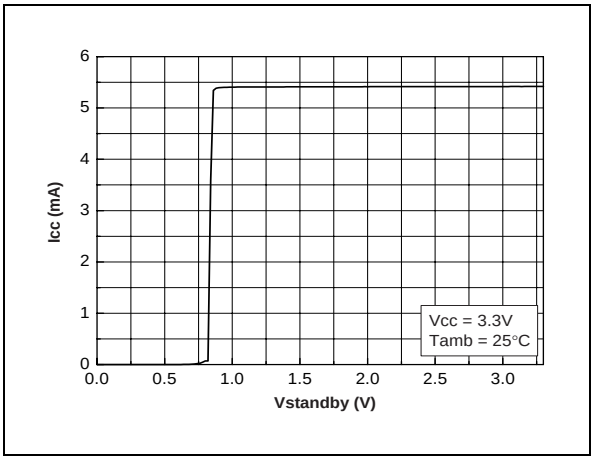
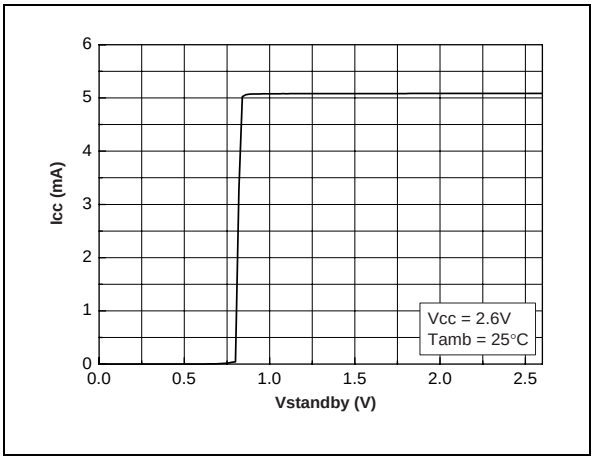


Fig. 51 : Current Consumption vs Standby Voltage @ Vcc = 2.6V



■ BTL Configuration Principle

The TS4902 is a monolithic power amplifier with a BTL (Bridge Tied Load) output configuration. BTL means that each end of the load is connected to two single ended output amplifiers. Thus, we have:

Single ended output 1 = Vout1 = Vout (V)
Single ended output 2 = Vout2 = -Vout (V)

And Vout1 - Vout2 = 2Vout (V)

The output power is :

$$Pout = \frac{(2\,Vout_{RMS})^2}{R_L} (W)$$

For the same power supply voltage, the output power in BTL configuration is four times higher than the output power in single ended configuration.

■ Gain In Typical Application Schematic (cf. page 1)

In flat region (no effect of Cin), the output voltage of the first stage is :

$$Vout1 = -Vin \frac{Rfeed}{Rin} (V)$$

For the second stage : Vout2 = -Vout1 (V)

The differential output voltage is

$$Vout2 - Vout1 = 2Vin \frac{Rfeed}{Rin} (V)$$

The differential gain named gain (Gv) for more convenient usage is :

$$Gv = \frac{Vout2 - Vout1}{Vin} = 2 \frac{Rfeed}{Rin}$$

Remark : Vout2 is in phase with Vin and Vout1 is 180 phased with Vin. It means that the positive terminal of the loudspeaker should be connected to Vout2 and the negative to Vout1.

■ Low and high frequency response

In low frequency region, the effect of Cin starts. Cin with Rin forms a high pass filter with a -3dB cut off frequency

$$F_{CL} = \frac{1}{2\pi\, Rin\, Cin} (Hz)$$

In high frequency region, you can limit the bandwidth by adding a capacitor (Cfeed) in parallel with Rfeed. Its form a low pass filter with a -3dB cut off frequency

$$F_{CH} = \frac{1}{2\pi\, Rfeed\, Cfeed} (Hz)$$

■ Power dissipation and efficiency

Hypothesis :

• Voltage and current in the load are sinusoidal (Vout and Iout)
• Supply voltage is a pure DC source (Vcc)

Regarding the load we have :

$$V_{OUT} = V_{PEAK} \sin\omega t (V)$$

and

$$I_{OUT} = \frac{V_{OUT}}{R_L} (A)$$

and

$$P_{OUT} = \frac{V_{PEAK}^2}{2R_L} (W)$$

Then, the average current delivered by the supply voltage is:

$$I_{CC\,AVG} = 2\frac{V_{PEAK}}{\pi R_L} (A)$$

The power delivered by the supply voltage is $Psupply = Vcc\ Icc_{AVG}$ (W)

Then, the **power dissipated by the amplifier** is Pdiss = Psupply - Pout (W)

$$P_{diss} = \frac{2\sqrt{2Vcc}}{\pi\sqrt{R_L}} \sqrt{P_{OUT}} - P_{OUT} (W)$$

and the maximum value is obtained when

$$\frac{\partial Pdiss}{\partial P_{OUT}} = 0$$

and its value is:

$$Pdissmax = \frac{2Vcc^2}{\pi^2 R_L} (W)$$

Remark : This maximum value is only depending on power supply voltage and load values.

The **efficiency** is the ratio between the output power and the power supply

$$\eta = \frac{P_{OUT}}{Psupply} = \frac{\pi V_{PEAK}}{4V_{CC}}$$

The maximum theoretical value is reached when Vpeak = Vcc, so

$$\frac{\pi}{4} = 78.5\%$$

■ Decoupling of the circuit

Two capacitors are needed to bypass properly the TS4902, a power supply bypass capacitor Cs and a bias voltage bypass capacitor Cb.

Cs has especially an influence on the THD+N in high frequency (above 7kHz) and indirectly on the power supply disturbances.
With 100µF, you can expect similar THD+N performances like shown in the datasheet.

If Cs is lower than 100µF, in high frequency increases, THD+N and disturbances on the power supply rail are less filtered.
To the contrary, if Cs is higher than 100µF, those disturbances on the power supply rail are more filtered.

Cb has an influence on THD+N in lower frequency, but its function is critical on the final result of PSRR with input grounded in lower frequency.

If Cb is lower than 1µF, THD+N increase in lower frequency (see THD+N vs frequency curves) and the PSRR worsens up
If Cb is higher than 1µF, the benefit on THD+N in lower frequency is small but the benefit on PSRR is substantial (see PSRR vs. Cb curve : fig.12).

Note that Cin has a non-negligible effect on PSRR in lower frequency. Lower is its value, higher is the PSRR (see fig. 13).

■ Pop and Click performance

Pop and Click performance is intimately linked with the size of the input capacitor Cin and the bias voltage bypass capacitor Cb.

Size of Cin is due to the lower cut-off frequency and PSRR value requested. Size of Cb is due to THD+N and PSRR requested always in lower frequency.

Moreover, Cb determines the speed that the amplifier turns ON. The slower the speed is, the softer the turn ON noise is.

The charge time of Cb is directly proportional to the internal generator resistance 50kΩ.
Then, the charge time constant for Cb is
τ**b = 50kΩxCb** (s)
As Cb is directly connected to the non-inverting input (pin 2 & 3) and if we want to minimize, in amplitude and duration, the output spike on Vout1 (pin 5), Cin must be charged faster than Cb. The charge time constant of Cin is
τ**in = (Rin+Rfeed)xCin** (s)

Thus we have the relation
τ**in << τb** (s)

The respect of this relation permits to minimize the pop and click noise.

Remark : Minimize Cin and Cb has a benefit on pop and click phenomena but also on cost and size of the application.

Example : your target for the -3dB cut off frequency is 100 Hz. With Rin=Rfeed=22 kΩ, Cin=72nF (in fact 82nF or 100nF).
With Cb=1µF, if you choose the one of the latest two values of Cin, the pop and click phenomena at power supply ON or standby function ON/OFF will be very small
50 kΩx1µF >> 44kΩx100nF (50ms >> 4.4ms).
Increasing Cin value increases the pop and click phenomena to an unpleasant sound at power supply ON and standby function ON/OFF.

Why Cs is not important in pop and click consideration ?

Hypothesis :
- Cs = 100µF
- Supply voltage = 5V
- Supply voltage internal resistor = 0.1Ω
- Supply current of the amplifier Icc = 6mA

At power ON of the supply, the supply capacitor is charged through the internal power supply resistor. So, to reach 5V you need about five to ten times the charging time constant of Cs (τs = 0.1xCs (s)).
Then, this time equal 50µs to 100µs << τb in the majority of application.

At power OFF of the supply, Cs is discharged by a constant current Icc. The discharge time from 5V to 0V of Cs is

$$t_{DischCs} = \frac{5Cs}{Icc} = 83\ ms$$

Now, we must consider the discharge time of Cb. At power OFF or standby ON, Cb is discharged by a 100kΩ resistor. So the discharge time is about $\tau b_{Disch} \approx 3xCbx100k\Omega$ (s).
In the majority of application, Cb=1µF, then $\tau b_{Disch} \approx 300ms >> t_{dischCs}$.

■ How to use the PSRR curves (page 7)

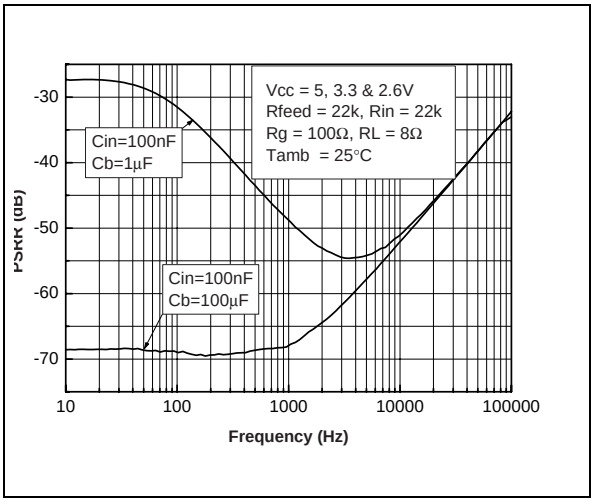
We have finished a design and we have chosen the components values :

• Rin=Rfeed=22kΩ, Cin=100nF, Cb=1µF

Now, on fig. 13, we can see the PSRR (input grounded) vs frequency curves. At 217Hz we have a PSRR value of -36dB.
In fact, we want a value of about -70dB. So, we need a gain of +34dB !
Now, on fig. 12 we can see the effect of Cb on the PSRR (input grounded) vs. frequency. With Cb=100µF, we can reach the -70dB value.

The process to obtain the final curve (Cb=100µF, Cin=100nF, Rin=Rfeed=22kΩ) is a simple transfer point by point on each frequency of the curve on fig. 13 to the curve on fig. 12.
The measurement result is shown on figure A.

Fig. A : PSRR changes with Cb



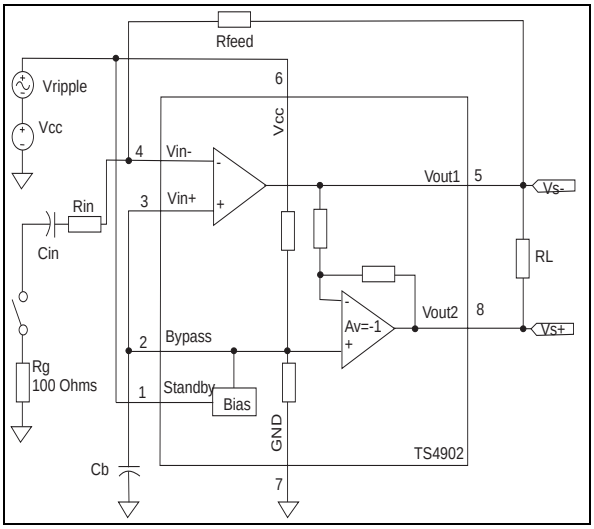
■ Remark on PSRR measurement conditions

What is the PSRR ?

The PSRR is the Power Supply Rejection Ratio. It's a kind of SVR in a determined frequency range. The PSRR of a device is the ratio between the power supply disturbance and the result on the output. We can say that the PSRR is the ability of a device to minimize the impact of power supply disturbances to the output.

How do we measure the PSRR ?

Fig. B : PSRR measurement schematic



■ Measurement process:

• Fix the DC voltage supply (Vcc)
• Fix the AC sinusoidal ripple voltage (Vripple)
• No bypass capacitor Cs is used

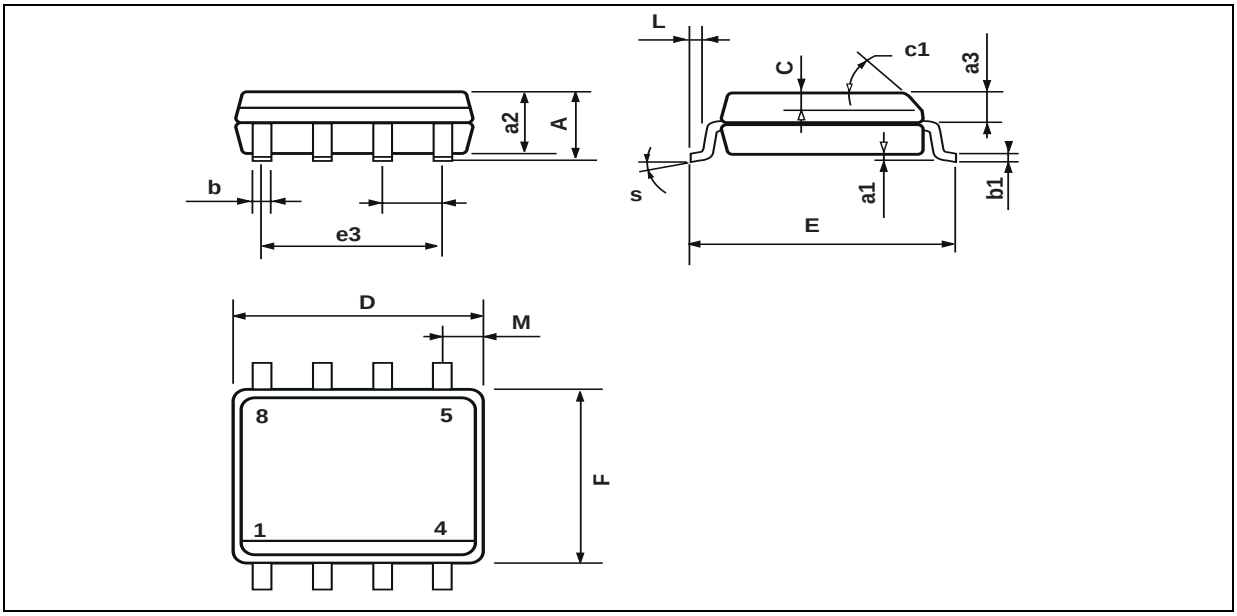
The PSRR value for each frequency is :

$$PSRR(dB) = 20 \times Log_{10}\left[\frac{Rms(V_{ripple})}{Rms(Vs_+ - Vs_-)}\right]$$

Remark : The measurement of the RMS voltage is not a selective RMS measurement but a full range (2 Hz to 125 kHz) RMS measurement. This means we have: the effective RMS signal + the noise.

PACKAGE MECHANICAL DATA

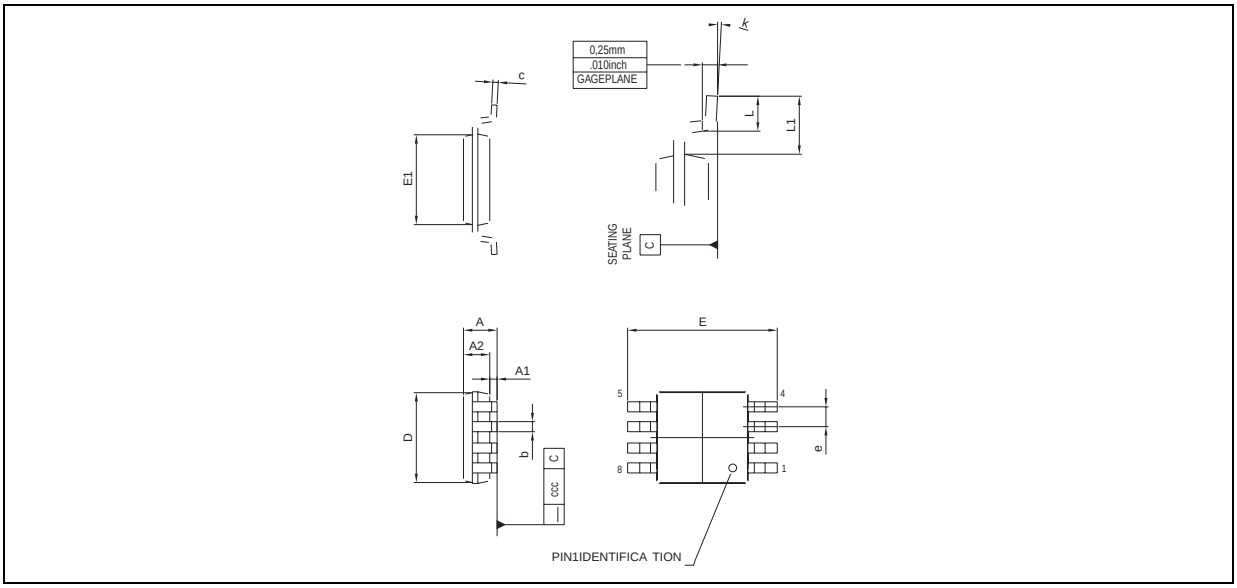
8 PINS - PLASTIC MICROPACKAGE (SO)



Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ.)					
D	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.150		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max.)					

PACKAGE MECHANICAL DATA

8 PINS - PLASTIC MICROPACKAGE (miniSO)



Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.100			0.043
A1	0.050	0.100	0.150	0.002	0.004	0.006
A2	0.780	0.860	0.940	0.031	0.034	0.037
b	0.250	0.330	0.400	0.010	0.013	0.016
c	0.130	0.180	0.230	0.005	0.007	0.009
D	2.900	3.000	3.100	0.114	0.118	0.122
E	4.750	4.900	5.050	0.187	0.193	0.199
E1	2.900	3.000	3.100	0.114	0.118	0.122
e		0.650			0.026	
L	0.400	0.550	0.700	0.016	0.022	0.028
L1		0.950			0.037	
k	0d	3d	6d	0d	3d	6d
ccc			0.100			0.004

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