

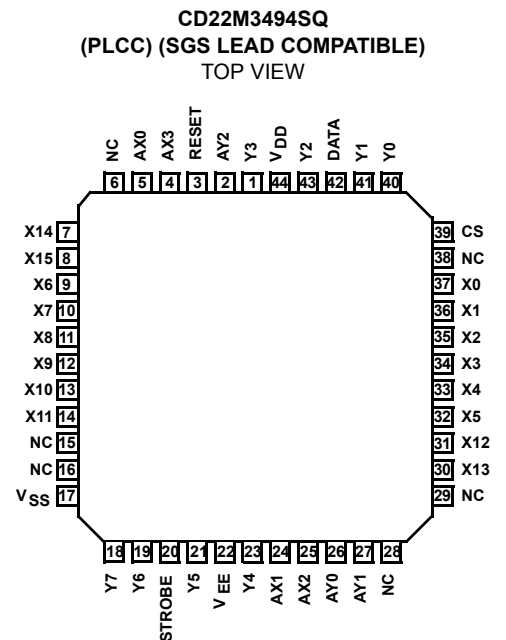
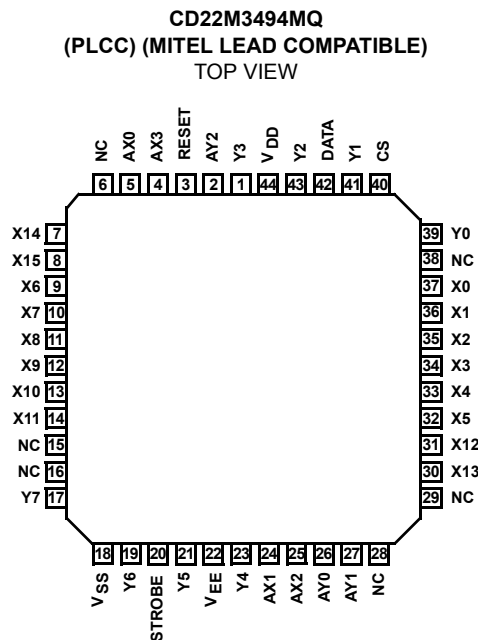
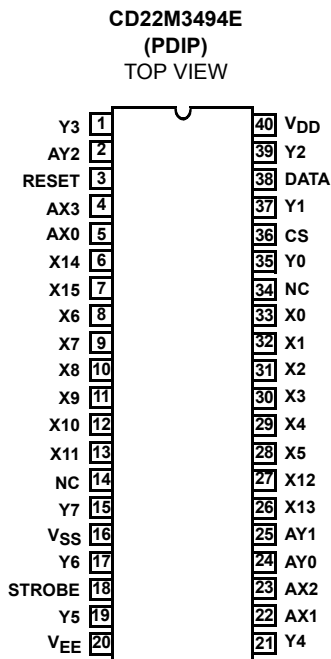
### Ordering Information

PART NUMBER (Note 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
CD22M3494EZ	CD22M3494EZ	-40 to 85	40 Ld PDIP (Note 2)	E40.6
CD22M3494MQZ (Note 1)	CD22M3494MQZ	-40 to 85	44 Ld PLCC (Mitel Ld Compatible)	N44.65
CD22M3494MQAZ (Note 1)	CD22M3494MQAZ	-40 to 85	44 Ld PLCC (Mitel Ld Compatible)	N44.65
CD22M3494SQZ (Note 1)	CD22M3494SQZ	-40 to 85	44 Ld PLCC (SGS Ld Compatible)	N44.65

NOTES:

1. Add "96" suffix for tape and reel. At one time the "QZ" and "QAZ" were different products, but since 1994 these parts have been **exactly** the same.
2. Pb-free PDIPs can be used for through-hole wave solder processing only. They are not intended for use in Reflow solder processing applications.
3. Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

### Pinouts



## Pin Descriptions

SYMBOL	40 LD PDIP PIN NO.	44 LD PLCC PIN NO.		DESCRIPTION
		MQ	SQ	
<b>POWER SUPPLIES</b>				
V <sub>DD</sub>	40	44	44	Positive Supply.
V <sub>SS</sub>	16	18	17	Negative Supply (Digital).
V <sub>EE</sub>	20	22	22	Negative Supply (Analog).
<b>ADDRESS</b>				
AX0 - AX3	5, 22, 23 and 4	5, 24, 25 and 4		X Address Lines. These pins select one of the 16 rows of switches. See the Truth Table on <a href="#">page 7</a> for the valid addresses.
AY0 - AY2	24, 25 and 2	26, 27 and 2		Y Address Lines. These pins select one of the 8 columns of switches. See the Truth Table on <a href="#">page 7</a> for the valid addresses.
<b>CONTROL</b>				
DATA	38	42		DATA Input determines the state of the addressed switch. A high or one will close the switch. A low or zero will open the switch.
STROBE	18	20		STROBE Input enables the action defined by the DATA and ADDRESS Inputs. A low or zero results in no action. The ADDRESS Input must be stable before the STROBE Input goes to the active high level. The DATA Input must be stable on the falling edge of the STROBE.
RESET	3	3		MASTER RESET. A high or one on this line opens all switches.
CS	36	40	39	CHIP SELECT. Device is selected when CS is at a high level, allows the crosspoint array to be cascaded for matrix expansion.
<b>INPUTS/OUTPUTS</b>				
X0 - X5 X6 - X11 X12 - X15	33-28, 8-13, 27, 26, 6, 7	37-32, 9-14, 31, 30, 7, 8		Analog or Digital Inputs/Outputs. These pins are the rows X0 - X15.
Y0 - Y7 I/O	35, 37, 39, 1, 21, 19, 17, 15	39, 41, 43, 1, 23, 21, 19, 17	40, 41, 43, 1, 23, 21, 19, 18	Analog or Digital Inputs/Outputs. These pins are the columns Y0 - Y7.

**Absolute Maximum Ratings**

DC Supply Voltage ( $V_{DD}$ )  
 Voltages Referenced to  $V_{EE}$  ..... -0.5V to 16V

DC Supply Voltage ( $V_{DD}$ )  
 Voltages Referenced to  $V_{SS}$  ..... -0.5V to 16V

DC Input Diode Current,  $I_{IN}$   
 For  $V_I$ , Digital <  $V_{SS}$  -0.5V or  $V_I$ ,  
 Analog <  $V_{EE}$  -0.5V or  $V_I > V_{DD}$  0.5V .....  $\pm 20$ mA

DC Output Diode Current,  $I_{OK}$   
 For  $V_O$ , Digital <  $V_{SS}$  -0.5V or  $V_O$ ,  
 Analog <  $V_{EE}$  -0.5V or  $V_O > V_{DD}$  0.5V .....  $\pm 20$ mA

DC Transmission Gate Current .....  $\pm 25$ mA

Power Dissipation Per Package ( $P_o$ )  
 For  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$  (PDIP) ..... 500mW  
 For  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$  (PLCC) ..... 600mW

**Thermal Information**

Thermal Resistance (Typical, [Note 4](#))  $\theta_{JA}$  ( $^\circ\text{C}/\text{W}$ )

PDIP Package\* ..... 55  
 PLCC Package ..... 43

Maximum Junction Temperature Plastic Package .....  $+150^\circ\text{C}$   
 Maximum Storage Temperature Range ( $T_{STG}$ ) .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Pb-Free Reflow Profile ..... see [TB493](#)  
 \*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

**Operating Conditions**

Operating Temperature Range ( $T_A$ )  
 Package Type E and Q .....  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$

Supply Voltage Range  
 For  $T_A =$  Full Package Temperature Range  
 $V_{SS} = 0\text{V}$ ,  $V_{EE} = 0\text{V}$ ,  $V_{DD}$  ..... 4V to 15V

DC Input or Output Voltage  $V_I$  or  $V_O$  .....  $V_{EE}$  to  $V_{DD}$   
 Digital Input Voltage .....  $V_{SS}$  to  $V_{DD}$

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTE:

- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

**Electrical Specifications**  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{DD} = 5\text{V}$ ,  $V_{SS} = 0\text{V}$ ,  $V_{EE} = 0\text{V}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>STATIC CONTROLS</b>						
Supply Current	$I_{DD}$	$V_{DD} = 5\text{V}$ , Logic Inputs = $V_{DD}$	-	-	2	mA
		$V_{DD} = 15\text{V}$ , Logic Inputs = $V_{DD}$	-	-	5	mA
High-Level Input Voltage	$V_{IH}$	$V_{DD} = 5\text{V}$	2.4 <a href="#">(Note 5)</a>	-	-	V
Low-Level Input Voltage	$V_{IL}$		-	-	0.8 <a href="#">(Note 5)</a>	V
Input Leakage Current, Digital	$I_{IN}$	Reset = Low <a href="#">(Note 6)</a>	-	-	$\pm 10$ <a href="#">(Note 7)</a>	$\mu\text{A}$

**Electrical Specifications**  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{DD} = 12\text{V}$ ,  $V_{SS} = 0\text{V}$ ,  $V_{EE} = 0\text{V}$ , Unless Otherwise Specified.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
<b>STATIC CROSSPOINTS</b>							
ON Resistance	$r_{ON}$	$V_{SS} = V_{EE} = 0\text{V}$ , $T_A = +25^\circ\text{C}$ , $V_{IN} = V_{DD}/2$ , $V_X - V_Y = 0.2\text{V}$	$V_{DD} = 10\text{V}$	-	40	75	$\Omega$
			$V_{DD} = 12\text{V}$	-	36	65	$\Omega$
ON Resistance	$r_{ON}$	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ , $V_{IN} = V_{DD}/2$ , $V_X - V_Y = 0.2\text{V}$ , $V_{SS} = V_{EE} = 0\text{V}$	$V_{DD} = 10\text{V}$	-	50	75	$\Omega$
			$V_{DD} = 12\text{V}$	-	45	65	$\Omega$
Difference in ON Resistance Between Any Two Switches	$\Delta r_{ON}$	$T_A = +25^\circ\text{C}$ , $V_{IN} = V_{DD}/2$ , $V_X - V_Y = 0.2\text{V}$ , $V_{SS} = V_{EE} = 0\text{V}$ , $V_{DD} = 12\text{V}$	-	6	10	$\Omega$	

**Electrical Specifications**  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{DD} = 12\text{V}$ ,  $V_{SS} = 0\text{V}$ ,  $V_{EE} = 0\text{V}$ , Unless Otherwise Specified. (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Difference in ON Resistance Between Any Two Switches	$\Delta r_{ON}$	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ , $V_{IN} = V_{DD}/2$ , $V_X - V_Y = 0.2\text{V}$ , $V_{DD} = 12\text{V}$ $V_{SS} = V_{EE} = 0\text{V}$ , $V_{DD} = 12\text{V}$	-	-	10	$\Omega$
OFF-State Leakage Current	$I_L$	$ V_X - V_Y  = 12\text{V}$	-	-	$\pm 10$ (Note 7)	$\mu\text{A}$

**Electrical Specifications**  $T_A = +25^\circ\text{C}$ ,  $V_{SS} = 0\text{V}$ ,  $V_{EE} = 0\text{V}$ ,  $V_{DD} = 14\text{V}$ ,  $C_L = 50\text{pF}$ , Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
<b>DYNAMIC CROSSPOINTS</b>						
Switch I/O Capacitance	$V_{IN} = V_{DD}/2$ , $f = 1\text{MHz}$	-	-	20	$\text{pF}$	
Switch Feedthrough Capacitance	$V_{IN} = V_{DD}/2$ , $f = 1\text{MHz}$	-	0.3	-	$\text{pF}$	
Propagation Delay Time (Switch ON) Signal Input to Output, $t_{PHL}$ or $t_{PLH}$		-	5	30	$\text{ns}$	
Frequency Response Channel ON $f = 20\log(V_X/V_Y) = -3\text{dB}$	$C_L = 3\text{pF}$ , $R_L = 75\Omega$ , $V_{IN} = 2V_{P-P}$	-	50	-	$\text{MHz}$	
Total Harmonic, THD	$V_{IN} = 2V_{P-P}$ , $f = 1\text{kHz}$	-	0.01	-	%	
Feedthrough Channel OFF Feedthrough = $20\log(V_X/V_Y) = F_{DT}$	$V_{IN} = 2V_{P-P}$ , $f = 1\text{kHz}$	-	-95	-	$\text{dB}$	
Frequency for Signal Crosstalk, $f_{CT}$ Attenuation of:	40dB	$V_{IN} = 2V_{P-P}$ , $R_L = 75\Omega$	-	10	-	$\text{MHz}$
	110dB	$V_{IN} = 2V_{P-P}$ , $R_L = 1\text{k}\Omega \parallel 10\text{pF}$	-	5	-	$\text{kHz}$
Control Crosstalk DATA-Input, ADDRESS, or STROBE to Output	Control Input = $3V_{P-P}$ Square Wave, $t_R = t_F = 10\text{ns}$ $R_{IN} = 1\text{K}$ , $R_{OUT} = 10\text{k}\Omega \parallel 10\text{pF}$	-	75	-	$\text{mV}_{PEAK}$	

**Electrical Specifications**  $T_A = +25^\circ\text{C}$ ,  $V_{SS} = 0\text{V}$ ,  $V_{EE} = 0\text{V}$ ,  $V_{DD} = 14\text{V}$ ,  $R_L = 1\text{k}\Omega \parallel 50\text{pF}$ , Unless Otherwise Specified.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>DYNAMIC CONTROLS</b>						
Digital Input Capacitance	$C_{IN}$	$V_{IN} = 5\text{V}$ , $f = 1\text{MHz}$	-	5	-	$\text{pF}$
Propagation Delay Time STROBE to Output						
Switch Turn-ON	$t_{PSN}$		-	50	100	$\text{ns}$
Switch Turn-OFF	$t_{PSF}$		-	50	100	$\text{ns}$
DATA-IN to Output						
Turn-ON to High Level	$t_{PZH}$		-	60	100	$\text{ns}$
Turn-ON to Low Level	$t_{PZL}$		-	70	100	$\text{ns}$
ADDRESS to Output						
Turn-ON to High Level	$t_{PAN}$		-	70	-	$\text{ns}$
Turn-OFF to Low Level	$t_{PAF}$		-	70	-	$\text{ns}$

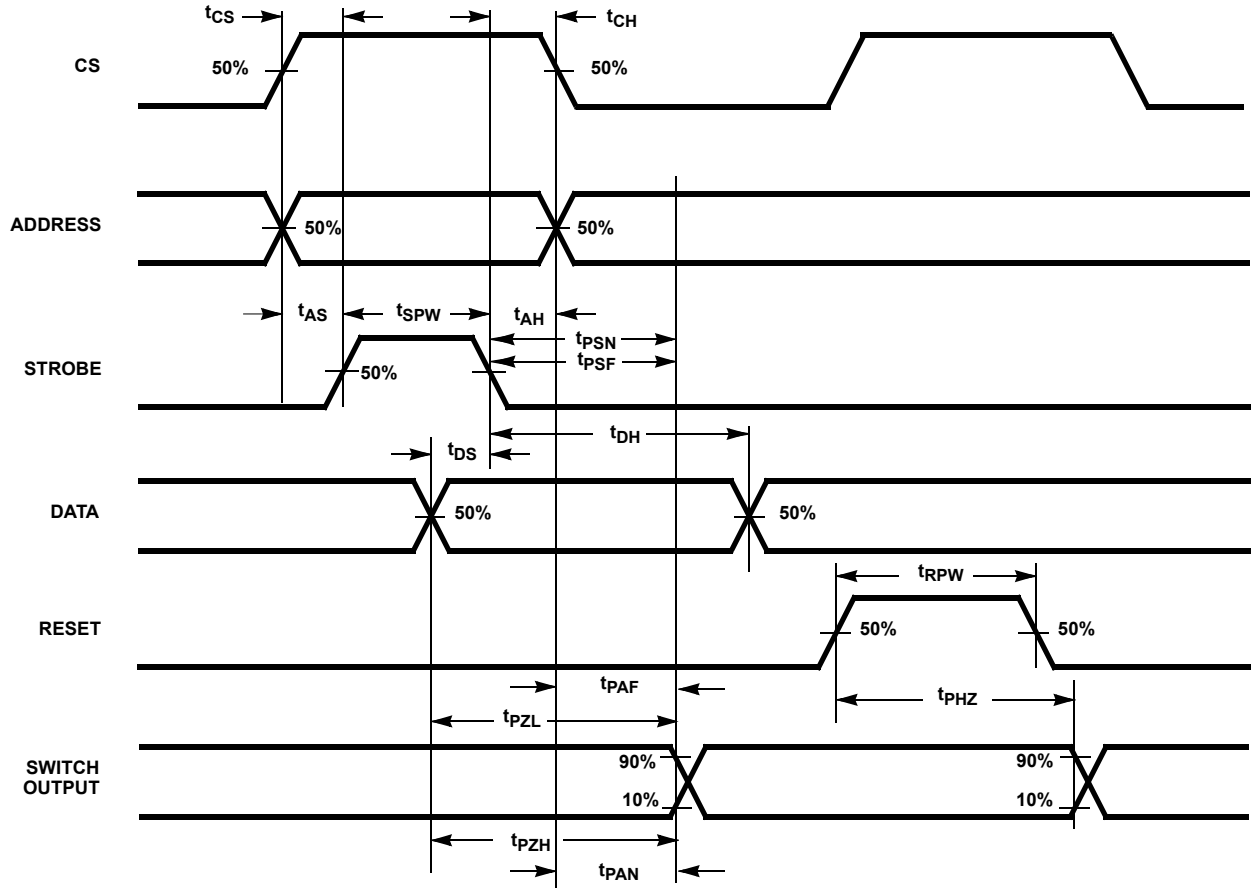
**Electrical Specifications**  $T_A = +25^\circ\text{C}$ ,  $V_{SS} = 0\text{V}$ ,  $V_{EE} = 0\text{V}$ ,  $V_{DD} = 14\text{V}$ ,  $R_L = 1\text{k}\Omega \parallel 50\text{pF}$ , Unless Otherwise Specified. (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Setup Time						
CS to STROBE	$t_{CS}$		10	-	-	ns
DATA-IN to STROBE	$t_{DS}$		10	-	-	ns
ADDRESS to STROBE	$t_{AS}$		10	-	-	ns
Hold Time						
STROBE to CS	$t_{CH}$		10	-	-	ns
ADDRESS to CS			10	-	-	ns
STROBE to DATA-IN	$t_{DH}$		20	-	-	ns
STROBE to ADDRESS	$t_{AH}$		10	-	-	ns
DATA-IN to CS			20	-	-	ns
Pulse Width						
STROBE	$t_{SPW}$		20	-	-	ns
RESET	$t_{RPW}$		20	-	-	ns
RESET Turn-OFF to Output Delay	$t_{PHZ}$		-	70	100	ns

## NOTES:

5. Operation of  $V_{IH}$  at 2.4V or  $V_{IL}$  at 0.8V will result in much higher supply current ( $I_{DD}$ ) than for logic inputs equal to  $V_{DD}$  or  $V_{SS}$  respectively.
6. Reset  $I_{IH} < 20\mu\text{A}$ , Reset =  $V_{IH}$ .
7. At  $+25^\circ\text{C}$  Limit is  $\pm 100\text{nA}$ .

**Timing Diagram**



**TRUTH TABLE X AXIS**

X ADDRESS				
AX3	AX2	AX1	AX0	X SWITCH
0	0	0	0	X0
0	0	0	1	X1
0	0	1	0	X2
0	0	1	1	X3
0	1	0	0	X4
0	1	0	1	X5
0	1	1	0	X12
0	1	1	1	X13
1	0	0	0	X6
1	0	0	1	X7
1	0	1	0	X8
1	0	1	1	X9
1	1	0	0	X10
1	1	0	1	X11
1	1	1	0	X14
1	1	1	1	X15

**TRUTH TABLE Y AXIS**

Y ADDRESS			
AY2	AY1	AY0	Y SWITCH
0	0	0	Y0
0	0	1	Y1
0	1	0	Y2
0	1	1	Y3
1	0	0	Y4
1	0	1	Y5
1	1	0	Y6
1	1	1	Y7

To make a connection (close switch) between any two points, specify an "X" address, a "Y" address, set "DATA" high, and switch "STROBE" from low to high. To break a connection, follow this same procedure with "DATA" low.

Example:

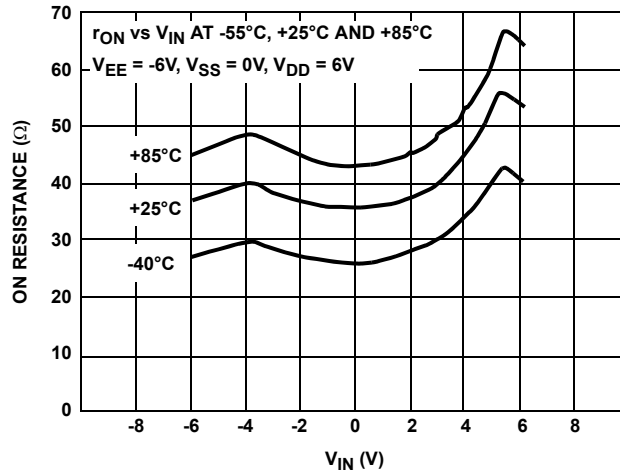
To connect switch X3 to switch Y4:

To connect switch X6 to switch Y7:

To break connection from X3 to Y4:

DATA	X ADDRESS				Y ADDRESS		
	AX3	AX2	AX1	AX0	AY2	AY1	AY0
1	0	0	1	1	1	0	0
1	1	0	0	0	1	1	1
0	0	0	1	1	1	0	0

### Typical Performance Curve



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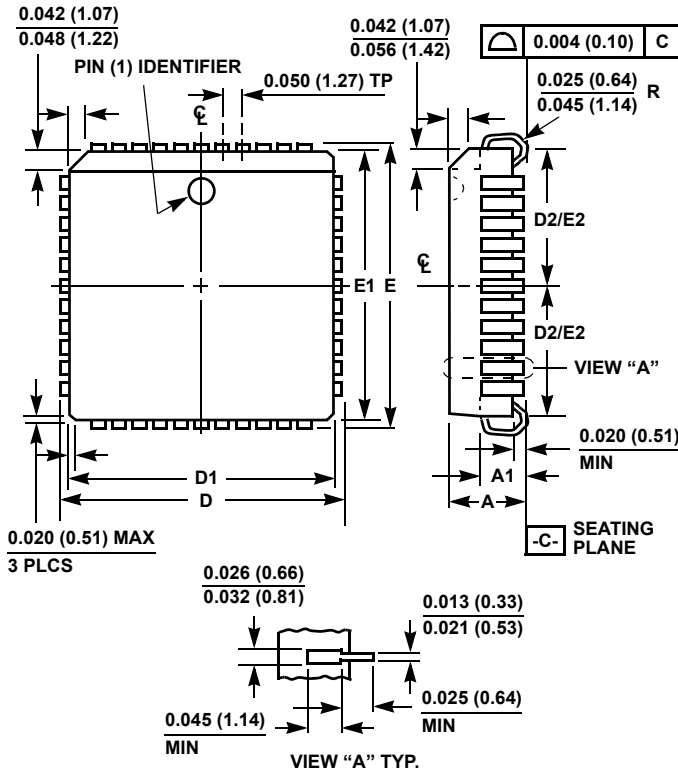
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**Plastic Leaded Chip Carrier Packages (PLCC)**



**N44.65 (JEDEC MS-018AC ISSUE A)  
44 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	0.685	0.695	17.40	17.65	-
D1	0.650	0.656	16.51	16.66	3
D2	0.291	0.319	7.40	8.10	4, 5
E	0.685	0.695	17.40	17.65	-
E1	0.650	0.656	16.51	16.66	3
E2	0.291	0.319	7.40	8.10	4, 5
N	44		44		6

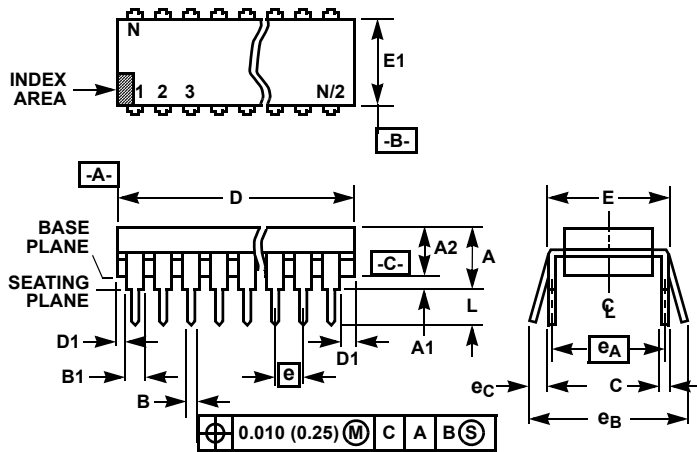
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**NOTES:**

- Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
- Dimensions and tolerancing per ANSI Y14.5M-1982.
- Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side. Dimensions D1 and E1 include mold mismatch and are measured at the extreme material condition at the body parting line.
- To be measured at seating plane -C- contact point.
- Centerline to be determined where center leads exit plastic body.
- "N" is the number of terminal positions.



### Dual-In-Line Plastic Packages (PDIP)



**NOTES:**

- Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
- Dimensioning and tolerancing per ANSI Y14.5M-1982.
- Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
- Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
- D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
- E and e<sub>A</sub> are measured with the leads constrained to be perpendicular to datum -C-.
- e<sub>B</sub> and e<sub>C</sub> are measured at the lead tips with the leads unconstrained. e<sub>C</sub> must be zero or greater.
- B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
- N is the maximum number of terminal positions.
- Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

**E40.6 (JEDEC MS-011-AC ISSUE B)  
40 LEAD DUAL-IN-LINE PLASTIC PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
C	0.008	0.015	0.204	0.381	-
D	1.980	2.095	50.3	53.2	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e <sub>A</sub>	0.600 BSC		15.24 BSC		6
e <sub>B</sub>	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	40		40		9

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