

SA572

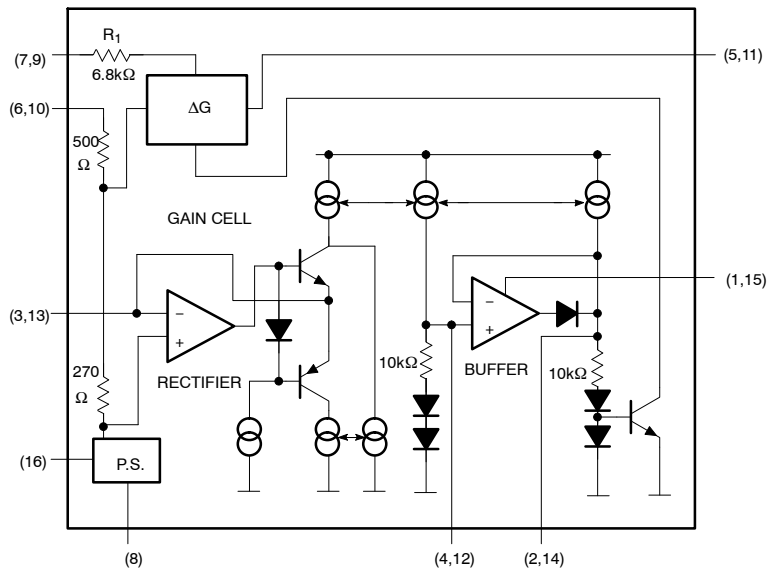


Figure 1. Block Diagram

PIN FUNCTION DESCRIPTION

| Pin | Symbol | Description |
|-----|------------------|----------------------------------|
| 1 | TRACK TRIM A | Tracking Trim A |
| 2 | RECOV. CAP A | Recovery Capacitor A |
| 3 | RECT. IN A | Rectifier A Input |
| 4 | ATTACK CAP A | Attack Capacitor A |
| 5 | ΔG OUT A | Variable Gain Cell A Output |
| 6 | THD TRIM A | Total Harmonic Distortion Trim A |
| 7 | ΔG IN A | Variable Gain Cell A Input |
| 8 | GND | Ground |
| 9 | ΔG IN B | Variable Gain Cell B Input |
| 10 | THD TRIM B | Total Harmonic Distortion Trim B |
| 11 | ΔG OUT B | Variable Gain Cell B Output |
| 12 | ATTACK CAP B | Attack Capacitor B |
| 13 | RECT. IN B | Rectifier B Input |
| 14 | RECOV. CAP B | Recovery Capacitor B |
| 15 | TRACK TRIM B | Tracking Trim B |
| 16 | V_{CC} | Positive Power Supply |

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|-----------------|------------|---------------|
| Supply Voltage | V_{CC} | 22 | V_{DC} |
| Operating Temperature Range | T_A | -40 to +85 | $^{\circ}C$ |
| Operating Junction Temperature | T_J | 150 | $^{\circ}C$ |
| Power Dissipation | P_D | 500 | mW |
| Thermal Resistance, Junction-to-Ambient | $R_{\theta JA}$ | 105 | $^{\circ}C/W$ |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

DC ELECTRICAL CHARACTERISTICS Standard test conditions, $V_{CC} = 15\text{ V}$, $T_A = 25^{\circ}C$; Expander mode (see Test Circuit). Input signals at unity gain level (0 dB) = 100 mV_{RMS} at 1.0 kHz; $V_1 = V_2$; $R_2 = 3.3\text{ k}\Omega$; $R_3 = 17.3\text{ k}\Omega$, unless otherwise noted.

| Characteristic | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|----------|--|------|-----------|------------|---------------|
| Supply Voltage | V_{CC} | - | 6.0 | - | 22 | V_{DC} |
| Supply Current | I_{CC} | No Signal | - | - | 6.3 | mA |
| Internal Voltage Reference | V_R | - | 2.3 | 2.5 | 2.7 | V_{DC} |
| Total Harmonic Distortion (Untrimmed) | THD | 1.0 kHz, $C_A = 1.0\text{ }\mu\text{F}$ | - | 0.2 | 1.0 | % |
| Total Harmonic Distortion (Trimmed) | THD | 1.0 kHz, $C_R = 10\text{ }\mu\text{F}$ | - | 0.05 | - | % |
| Total Harmonic Distortion (Trimmed) | THD | 100 Hz | - | 0.25 | - | % |
| No Signal Output Noise | | Input to V_1 and V_2 grounded (20–20 kHz) | - | 6.0 | 25 | μV |
| DC Level Shift (Untrimmed) | | Input change from no signal to 100 mV_{RMS} | - | ± 20 | ± 50 | mV |
| Unity Gain Level | | - | -1.5 | 0 | +1.5 | dB |
| Large-Signal Distortion | | $V_1 = V_2 = 400\text{ mV}$ | - | 0.7 | 3.0 | % |
| Tracking Error (Measured relative to value at unity gain) = [$V_O - V_O$ (unity gain)] dB - V_2 dB | | Rectifier Input $V_2 = +6.0\text{ dB}$, $V_1 = 0\text{ dB}$ | - | ± 0.2 | - | dB |
| | | $V_2 = -30\text{ dB}$, $V_1 = 0\text{ dB}$ | - | ± 0.5 | -2.5, +1.6 | dB |
| Channel Crosstalk | | 200 mV_{RMS} into channel A, measured output on channel B | 60 | - | - | dB |
| Power Supply Rejection Ratio | PSRR | 120 Hz | - | 70 | - | dB |

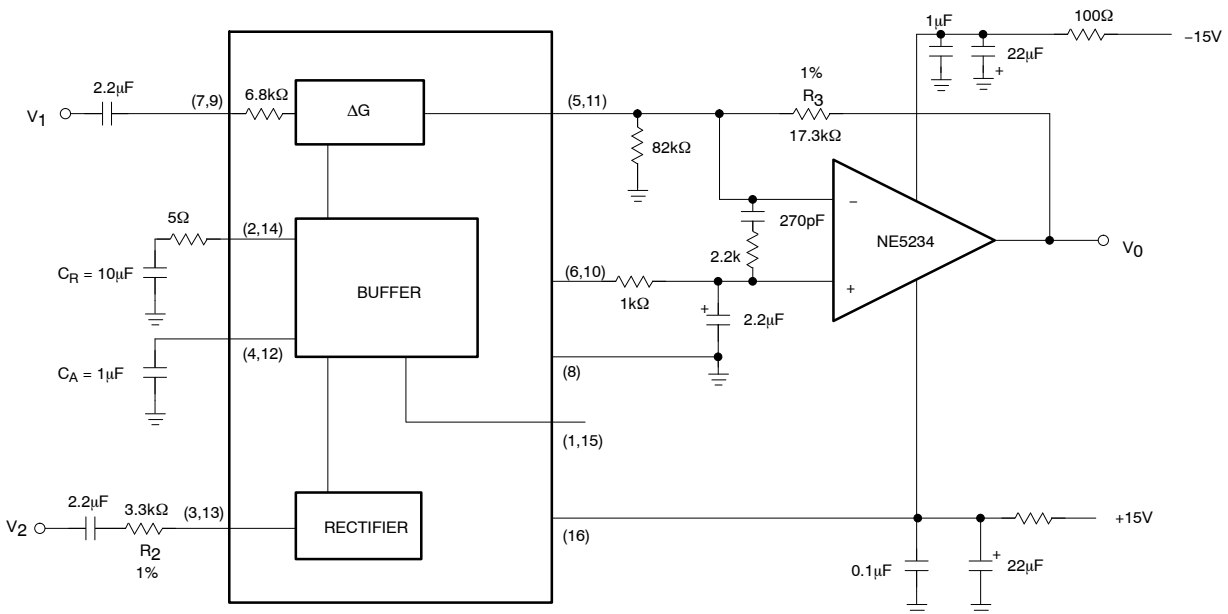


Figure 2. Test Circuit

Audio Signal Processing IC Combines VCA and Fast Attack/Slow Recovery Level Sensor

In high-performance audio gain control applications, it is desirable to independently control the attack and recovery time of the gain control signal. This is true, for example, in compandor applications for noise reduction. In high end systems the input signal is usually split into two or more frequency bands to optimize the dynamic behavior for each band. This reduces low frequency distortion due to control signal ripple, phase distortion, high frequency channel overload and noise modulation. Because of the expense in hardware, multiple band signal processing up to now was limited to professional audio applications.

With the introduction of the SA572 this high-performance noise reduction concept becomes feasible for consumer hi fi applications. The SA572 is a dual channel gain control IC. Each channel has a linearized, temperature-compensated gain cell and an improved level sensor. In conjunction with an external low noise op amp for current-to-voltage conversion, the VCA features low distortion, low noise and wide dynamic range.

The novel level sensor which provides gain control current for the VCA gives lower gain control ripple and independent control of fast attack, slow recovery dynamic response. An attack capacitor C_A with an internal 10 k Ω resistor R_A defines the attack time τ_A . The recovery time τ_R of a tone burst is defined by a recovery capacitor C_R and an internal 10 k Ω resistor R_R . Typical attack time of 4.0 ms for the high-frequency spectrum and 40 ms for the low frequency band can be obtained with 0.1 μ F and 1.0 μ F attack capacitors, respectively. Recovery time of 200 ms can be obtained with a 4.7 μ F recovery capacitor for a 100 Hz signal, the third harmonic distortion is improved by more than 10 dB over the simple RC ripple filter with a single 1.0 μ F attack and recovery capacitor, while the attack time remains the same.

The SA572 is assembled in a standard 16-pin dual in-line plastic package and in oversized SOL package. It operates over a wide supply range from 6.0 V to 22 V. Supply current is less than 6.0 mA. The SA572 is designed for applications from -40°C to $+85^\circ\text{C}$.

BASIC APPLICATIONS

Description

The SA572 consists of two linearized, temperature-compensated gain cells (ΔG), each with a full-wave rectifier and a buffer amplifier as shown in the block diagram. The two channels share a 2.5 V common bias reference derived from the power supply but otherwise operate independently. Because of inherent low distortion, low noise and the capability to linearize large signals, a wide dynamic range can be obtained. The buffer amplifiers are provided to permit control of attack time and recovery time independent of each other. Partitioned as shown in the block diagram, the IC allows flexibility in the design of system levels that optimize DC shift, ripple distortion, tracking accuracy and noise floor for a wide range of application requirements.

Gain Cell

Figure 3 shows the circuit configuration of the gain cell. Bases of the differential pairs Q_1 - Q_2 and Q_3 - Q_4 are both tied to the output and inputs of OPA A_1 . The negative feedback through Q_1 holds the V_{BE} of Q_1 - Q_2 and the V_{BE} of Q_3 - Q_4 equal. The following relationship can be derived from the transistor model equation in the forward active region.

$$\Delta V_{BE_{Q3Q4}} = \Delta V_{BE_{Q1Q2}}$$

$$(V_{BE} = V_T \ln IC/IS)$$

$$V_{Tn} \ln \left(\frac{\frac{1}{2} I_G + \frac{1}{2} I_O}{I_S} \right) - V_{Tn} \ln \left(\frac{\frac{1}{2} I_G - \frac{1}{2} I_O}{I_S} \right) \quad (\text{eq. 1})$$

$$= V_{Tn} \ln \left(\frac{I_1 + I_{IN}}{I_S} \right) - V_{Tn} \ln \left(\frac{I_2 - I_1 - I_{IN}}{I_S} \right)$$

$$\text{where } I_{IN} = \frac{V_{IN}}{R_1}$$

$$R_1 = 6.8 \text{ k}\Omega$$

$$I_1 = 140 \mu\text{A}$$

$$I_2 = 280 \mu\text{A}$$

I_O is the differential output current of the gain cell and I_G is the gain control current of the gain cell.

If all transistors Q_1 through Q_4 are of the same size, equation 1 can be simplified to:

$$I_O = \frac{2}{I_2} \cdot I_{IN} \cdot I_G - \frac{1}{I_2} (I_2 - 2I_1) \cdot I_G \quad (\text{eq. 2})$$

The first term of equation 2 shows the multiplier relationship of a linearized two quadrant transconductance amplifier. The second term is the gain control feedthrough due to the mismatch of devices. In the design, this has been minimized by large matched devices and careful layout. Offset voltage is caused by the device mismatch and it leads to even harmonic distortion. The offset voltage can be trimmed out by feeding a current source within $\pm 25 \mu\text{A}$ into the THD trim pin.

The residual distortion is third harmonic distortion and is caused by gain control ripple. In a compandor system, available control of fast attack and slow recovery improve ripple distortion significantly. At the unity gain level of 100 mV, the gain cell gives THD (total harmonic distortion) of 0.17% typ. Output noise with no input signals

is only 6.0 μV in the audio spectrum (10 Hz-20 kHz). The output current I_O must feed the virtual ground input of an operational amplifier with a resistor from output to inverting input. The non-inverting input of the operational amplifier has to be biased at V_{REF} if the output current I_O is DC coupled.

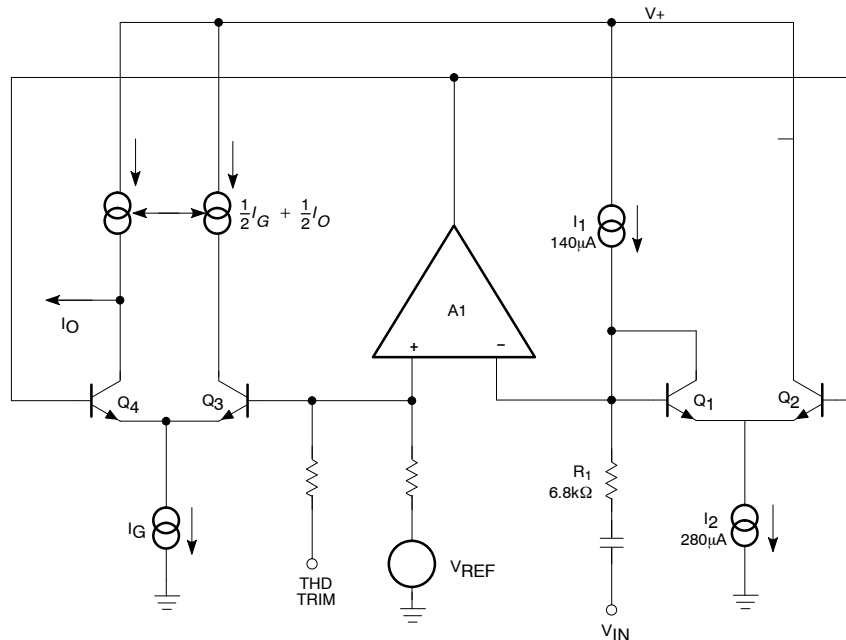


Figure 3. Basic Gain Cell Schematic

Rectifier

The rectifier is a full-wave design as shown in Figure 4. The input voltage is converted to current through the input resistor R_2 and turns on either Q_5 or Q_6 depending on the signal polarity. Deadband of the voltage to current converter is reduced by the loop gain of the gain block A_2 . If AC coupling is used, the rectifier error comes only from input bias current of gain block A_2 . The input bias current is typically about 70 nA. Frequency response of the gain block A_2 also causes second-order error at high frequency. The collector current of Q_6 is mirrored and summed at the collector of Q_5 to form the full wave rectified output current I_R . The rectifier transfer function is:

$$I_R = \frac{V_{IN} - V_{REF}}{R_2} \quad (\text{eq. 3})$$

If V_{IN} is AC-coupled, then the equation will be reduced to:

$$I_{RAC} = \frac{V_{IN(AVG)}}{R_2}$$

The internal bias scheme limits the maximum output current I_R to be around 300 μA. Within a ± 1.0 dB error band the input range of the rectifier is about 52 dB.

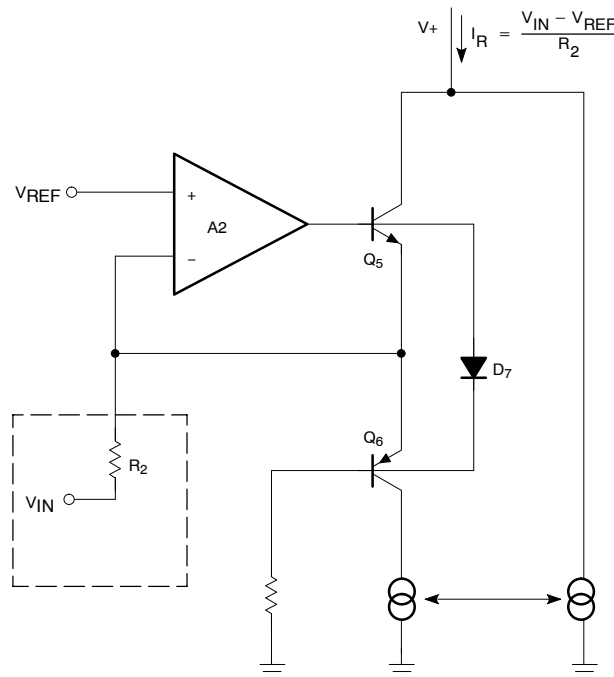


Figure 4. Simplified Rectifier Schematic

Buffer Amplifier

In audio systems, it is desirable to have fast attack time and slow recovery time for a tone burst input. The fast attack time reduces transient channel overload but also causes low-frequency ripple distortion. The low-frequency ripple distortion can be improved with the slow recovery time. If different attack times are implemented in corresponding frequency spectrums in a split band audio system, high quality performance can be achieved. The buffer amplifier is designed to make this feature available with minimum external components. Referring to Figure 5, the rectifier output current is mirrored into the input and output of the unipolar buffer amplifier A3 through Q8, Q9 and Q10. Diodes D11 and D12 improve tracking accuracy and provide common-mode bias for A3. For a positive-going input signal, the buffer amplifier acts like a voltage-follower. Therefore, the output impedance of A3 makes the contribution of capacitor CR to attack time insignificant. Neglecting diode impedance, the gain Ga(t) for ΔG can be expressed as follows:

$$G_a(t) = (G_{a_{INT}} - G_{a_{FNL}}) e^{-\frac{t}{\tau_A}} + G_{a_{FNL}}$$

Ga_{INT} = Initial Gain

Ga_{FNL} = Final Gain

$$\tau_A = R_A \cdot C_A = 10 \text{ k}\Omega \cdot C_A$$

where τ_A is the attack time constant and R_A is a 10 kΩ internal resistor. Diode D15 opens the feedback loop of A3 for a negative-going signal if the value of capacitor CR is larger than capacitor CA. The recovery time depends only on CR • RR. If the diode impedance is assumed negligible, the dynamic gain GR (t) for ΔG is expressed as follows:

$$G_R(t) = (G_{R_{INT}} - G_{R_{FNL}}) e^{-\frac{t}{\tau_R}} + G_{R_{FNL}}$$

$$G_R(t) = (G_{R_{INT}} - G_{R_{FNL}}) e^{-\frac{t}{\tau_R}} + G_{R_{FNL}}$$

$$\tau_R = R_R \cdot C_R = 10 \text{ k}\Omega \cdot C_R$$

where τ_R is the recovery time constant and R_R is a 10 kΩ internal resistor. The gain control current is mirrored to the gain cell through Q14. The low level gain errors due to input bias current of A2 and A3 can be trimmed through the tracking trim pin into A3 with a current source of ± 3.0 μA.

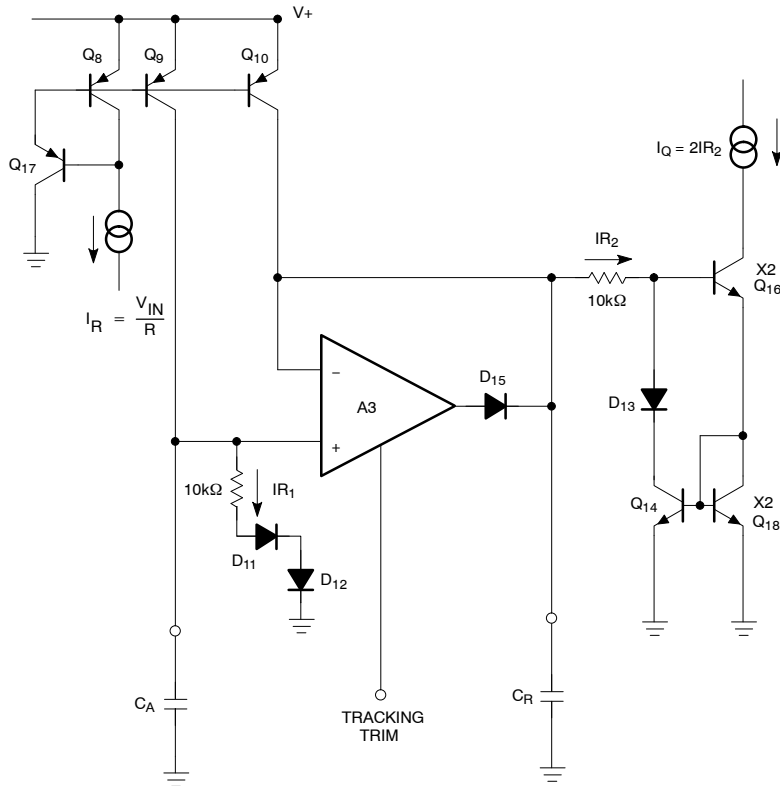


Figure 5. Buffer Amplifier Schematic

Basic Expander

Figure 6 shows an application of the circuit as a simple expander. The gain expression of the system is given by:

$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{2}{I_1} \cdot \frac{R_3 \cdot V_{IN(AVG)}}{R_2 \cdot R_1} \right)^2 \quad (\text{eq. 4})$$

(I₁ = 140 μA)

Both the resistors R₁ and R₂ are tied to internal summing nodes. R₁ is a 6.8 kΩ internal resistor. The maximum input current into the gain cell can be as large as 140 μA. This corresponds to a voltage level of 140 μA • 6.8 kΩ = 952 mV peak. The input peak current into the rectifier is limited to 300 μA by the internal bias system. Note that the value of R₁ can be increased to accommodate higher input level. R₂ and R₃ are external resistors. It is easy to adjust the ratio of R₃/R₂ for desirable system voltage and current levels. A small R₂ results in higher gain control current and smaller static and dynamic tracking error. However, an impedance

buffer A₁ may be necessary if the input is voltage driven with large source impedance.

The gain cell output current feeds the summing node of the external OPA A₂. R₃ and A₂ convert the gain cell output current to the output voltage. In high-performance applications, A₂ has to be low-noise, high-speed and wide band so that the high-performance output of the gain cell will not be degraded. The non-inverting input of A₂ can be biased at the low noise internal reference Pin 6 or 10. Resistor R₄ is used to bias up the output DC level of A₂ for maximum swing. The output DC level of A₂ is given by:

$$V_{OUT DC} = V_{REF} \left(1 + \frac{R_3}{R_4} \right) - V_B \frac{R_3}{R_4} \quad (\text{eq. 5})$$

V_B can be tied to a regulated power supply for a dual supply system and be grounded for a single supply system. C_A sets the attack time constant and C_R sets the recovery time constant.

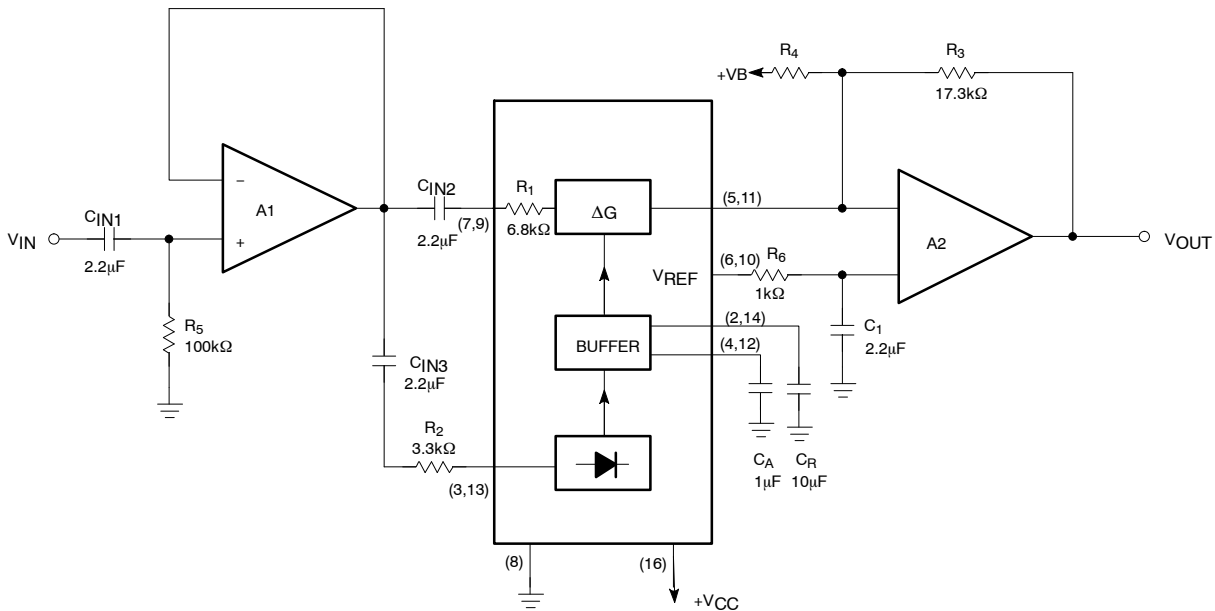


Figure 6. Basic Expander Schematic

Basic Compressor

Figure 7 shows the hook-up of the circuit as a compressor. The IC is put in the feedback loop of the OPA A₁. The system gain expression is as follows:

$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{I_1}{2} \cdot \frac{R_2 \cdot R_1}{R_3 \cdot V_{IN(AVG)}} \right)^{\frac{1}{2}} \quad (\text{eq. 6})$$

(I₁ = 140 μA)

R_{DC1}, R_{DC2}, and CDC form a DC feedback for A₁. The output DC level of A₁ is given by:

$$V_{OUT DC} = V_{REF} \left(1 + \frac{R_{DC1} + R_{DC2}}{R_4} \right) - V_B \cdot \left(\frac{R_{DC1} + R_{DC2}}{R_4} \right) \quad (\text{eq. 7})$$

The zener diodes D₁ and D₂ are used for channel overload protection.

SA572

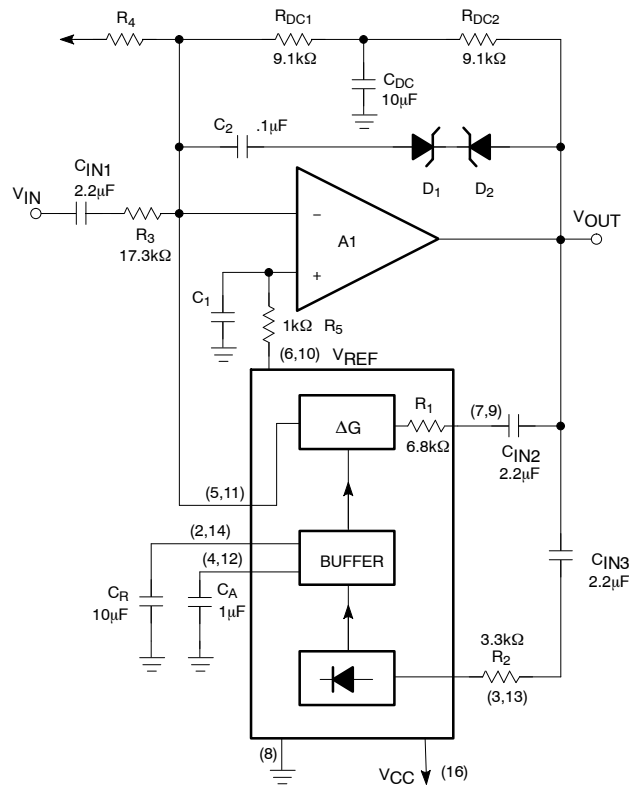


Figure 7. Basic Compressor Schematic

Basic Compressor System

The above basic compressor and expander can be applied to systems such as tape/disc noise reduction, digital audio, bucket brigade delay lines. Additional system design techniques such as bandlimiting, band splitting,

pre-emphasis, de-emphasis and equalization are easy to incorporate. The IC is a versatile functional block to achieve a high performance audio system. Figure 8 shows the system level diagram for reference.

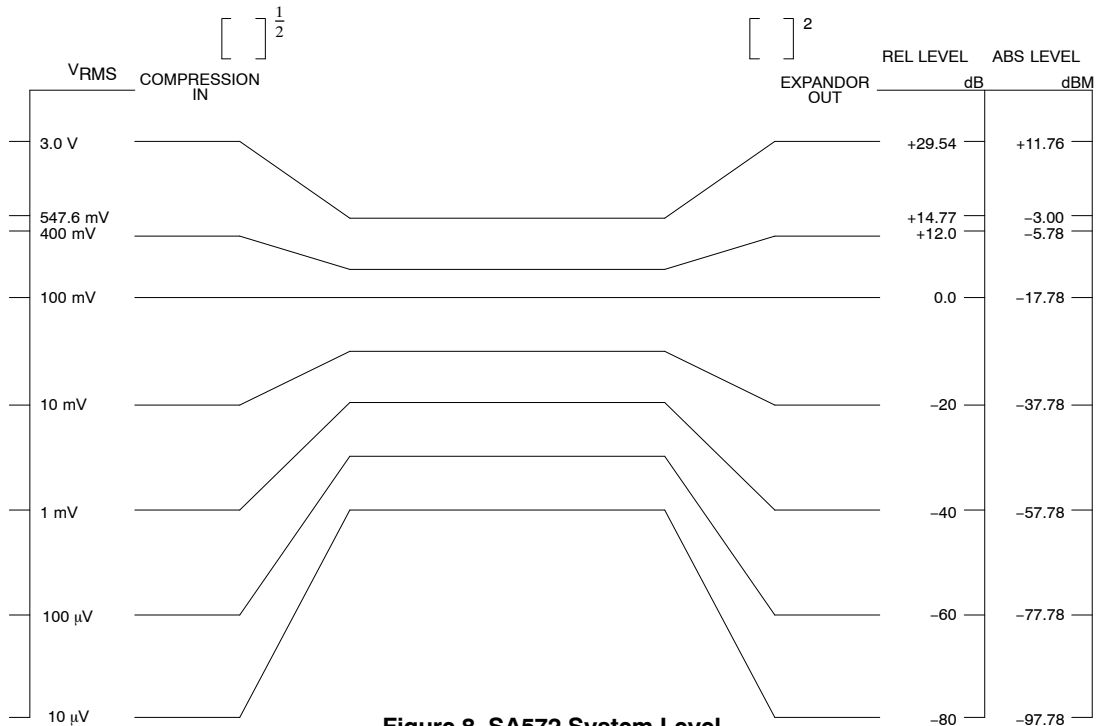


Figure 8. SA572 System Level

SA572

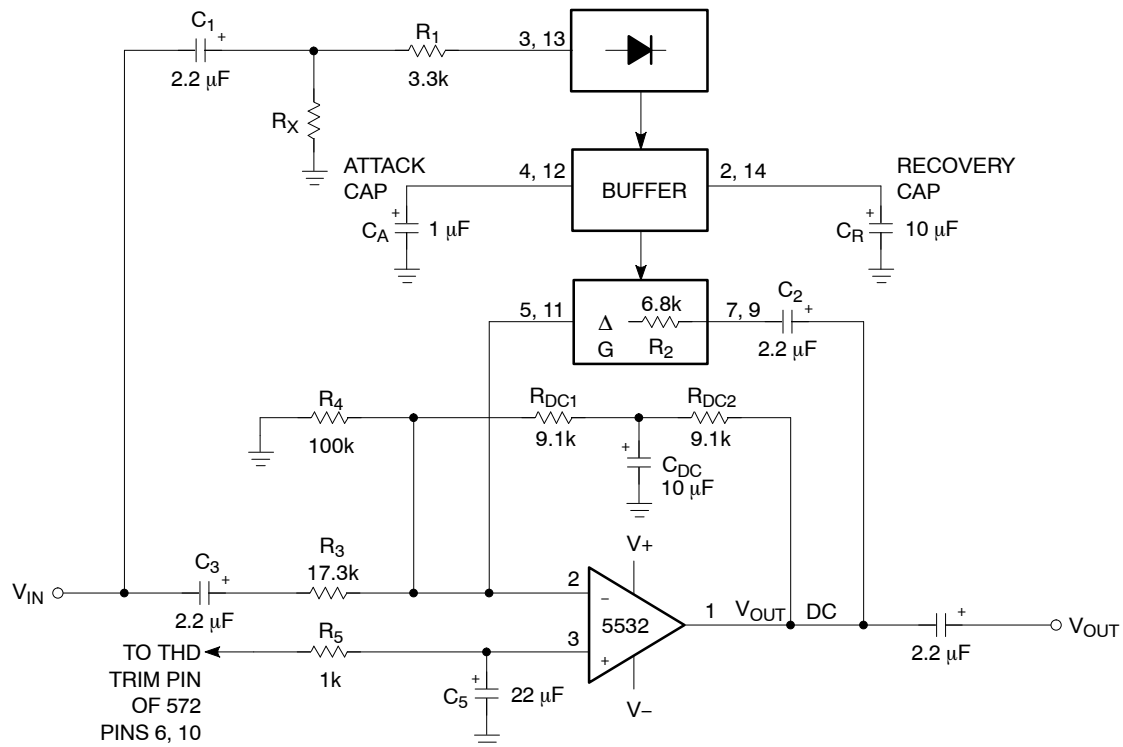


Figure 9. Automatic Level Control

Automatic Level Control (ALC)

In the ALC configuration, the variable gain cell is placed in the feedback loop of the operational amplifier and the rectifier is connected to the input. As the input amplitude increases above the crossover point, the overall system gain decreases proportionally, holding the output amplitude constant. As the input amplitude decreases below the crossover point, the overall system gain increases proportionally, holding the output amplitude at the same constant level.

$$\text{Gain} = \frac{R_1 R_2 I_1}{2 R_3 V_{IN}(\text{avg})}$$

where: $R_1 = 6.8 \text{ k}\Omega$ (Internal)
 $R_2 = 3.3 \text{ k}\Omega$
 $R_3 = 17.3 \text{ k}\Omega$
 $I_1 = 140 \text{ }\mu\text{A}$

The output DC level can be set using the following equation:

$$V_{\text{OUT DC}} = \left(1 + \frac{R_{\text{DC1}} + R_{\text{DC2}}}{R_4} \right) V_{\text{REF}}$$

where: $R_4 = 100 \text{ k}\Omega$
 $R_{\text{DC1}} = R_{\text{DC2}} = 9.1 \text{ k}\Omega$
 $V_{\text{REF}} = 2.5 \text{ V}$

The output level is calculated using the following equation:

$$V_{\text{OUT_LEVEL}} = \frac{R_1 R_2 I_1}{2 R_3} \left(\frac{V_{\text{IN}}}{V_{\text{IN}}(\text{avg})} \right)$$

where: $R_1 = 6.8 \text{ k}\Omega$ (Internal)
 $R_2 = 3.3 \text{ k}\Omega$
 $R_3 = 17.3 \text{ k}\Omega$
 $I_1 = 140 \text{ }\mu\text{A}$

$$\frac{V_{\text{IN}}}{V_{\text{IN}}(\text{avg})} = \frac{\pi}{2\sqrt{2}} = 1.11 \text{ (for sine waves)}$$

Note that for very low input levels, ALC may not be desired and to limit the maximum gain, resistor R_X has been added.

$$\text{Gain max.} = \frac{\left(\frac{R_1 + R_X}{V_{\text{REF}}} \right) \cdot R_2 \cdot I_B}{2 R_3}$$

$$R_X \cong ((\text{desired max gain}) \times 26 \text{ k}\Omega) - 10 \text{ k}\Omega$$

SA572

ORDERING INFORMATION

| Device | Description | Package | Temperature Range | Shipping† |
|-----------|---|----------|-------------------|--------------------|
| SA572DR2G | 16-Pin Plastic Small Outline Package (Pb-Free) | SO-16 WB | -40 to +85°C | 1000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



1
SCALE 1:1

SOIC-16 WB
CASE 751G
ISSUE E

DATE 08 OCT 2021



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION OR FLASH TO BE 0.15 PER SIDE.

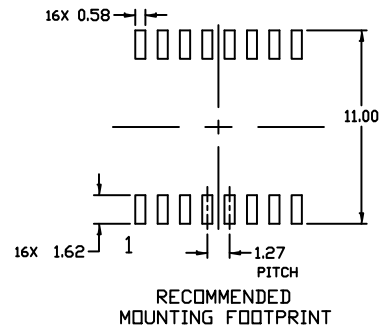
| DIM | MILLIMETERS | |
|-----|-------------|-------|
| | MIN. | MAX. |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| B | 0.35 | 0.49 |
| C | 0.23 | 0.32 |
| D | 10.15 | 10.45 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.53 REF | |
| L | 0.50 | 0.90 |
| M | 0° | 7° |

GENERIC MARKING DIAGRAM*



- XXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



| | | |
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[SA572NG](#)