ABSOLUTE MAXIMUM RATINGS

$V_{CC}1$, $V_{CC}2$, RSTIN, $\overline{MR}$, WDI to GND .....-0.3V to +6V
$\overline{RST}$, $\overline{WDO}$ to GND (open drain).....-0.3V to +6V
$\overline{RST}$, $\overline{WDO}$ to GND (push-pull).....-0.3V to ($V_{CC}1$ + 0.3V)
Input Current/Output Current (all pins) 20mA
Continuous Power Dissipation (T_A = +70°C)
6-Pin SOT23-6 (derate 4.3mW/°C above +70°C) 347.8mW
8-Pin SOT23-8 (derate 5.6mW/°C above +70°C) 444.4mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow)
Lead (Pb)-free packages.....+260°C
Package containing lead (Pb) .....+240°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

6 SOT23
Junction-to-Ambient Thermal Resistance (θ_{JA}).....230°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....76°C/W

8 SOT23
Junction-to-Ambient Thermal Resistance (θ_{JA}).....180°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....60°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

($V_{CC}1$ = $V_{CC}2$ = +0.8V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	$V_{CC}1$, $V_{CC}2$		0.8		5.5	V
Supply Current	$I_{CC}1$	$V_{CC}1$ < +5.5V, all I/O connections open, outputs not asserted		15	39	µA
		$V_{CC}1$ < +3.6V, all I/O connections open, outputs not asserted		10	28	
	$I_{CC}2$	$V_{CC}2$ < +3.6V, all I/O connections open, outputs not asserted		4	11	
		$V_{CC}2$ < +2.75V, all I/O connections open, outputs not asserted		3	9	
$V_{CC}1$ Reset Threshold	$V_{TH}1$	L (falling)	4.500	4.625	4.750	V
		M (falling)	4.250	4.375	4.500	
		T (falling)	3.000	3.075	3.150	
		S (falling)	2.850	2.925	3.000	
		R (falling)	2.550	2.625	2.700	
		Z (falling)	2.250	2.313	2.375	
		Y (falling)	2.125	2.188	2.250	
		W (falling)	1.620	1.665	1.710	
		V (falling)	1.530	1.575	1.620	

ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}1$ = $V_{CC}2$ = +0.8V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{CC}2$ Reset Threshold	$V_{TH}2$	T (falling)	3.000	3.075	3.150	V
		S (falling)	2.850	2.925	3.000	
		R (falling)	2.550	2.625	2.700	
		Z (falling)	2.250	2.313	2.375	
		Y (falling)	2.125	2.188	2.250	
		W (falling)	1.620	1.665	1.710	
		V (falling)	1.530	1.575	1.620	
		I (falling)	1.350	1.388	1.425	
		H (falling)	1.275	1.313	1.350	
		G (falling)	1.080	1.110	1.140	
		F (falling)	1.020	1.050	1.080	
		E (falling)	0.810	0.833	0.855	
		D (falling)	0.765	0.788	0.810	
Reset Threshold Tempco				20		ppm/°C
Reset Threshold Hysteresis	V_{HYST}	Referenced to V_{TH} typical		0.5		%
$V_{CC\_}$ to $\overline{RST}$ Output Delay	t_{RD}	$V_{CC}1$ = ($V_{TH}1$ + 100mV) to ($V_{TH}1$ - 100mV) or $V_{CC}2$ = ($V_{TH}2$ + 75mV) to ($V_{TH}2$ - 75mV)		45		µs
Reset Timeout Period	t_{RP}	D1	1.1	1.65	2.2	ms
		D2	8.8	13.2	17.6	
		D3	140	210	280	
		D5	280	420	560	
		D6	560	840	1120	
		D4	1120	1680	2240	
ADJUSTABLE RESET COMPARATOR INPUT (MAX6734/MAX6735)						
RSTIN Input Threshold	V_{RSTIN}		611	626.5	642	mV
RSTIN Input Current	I_{RSTIN}		-25		+25	nA
RSTIN Hysteresis				3		mV
RSTIN to Reset Output Delay	t_{RSTIND}	V_{RSTIN} to (V_{RSTIN} - 30mV)		22		µs
MANUAL RESET INPUT (MAX6730/MAX6731/MAX6734/MAX6735)						
$\overline{MR}$ Input Threshold	V_{IL}				0.3 × $V_{CC}1$	V
	V_{IH}		0.7 × $V_{CC}1$			
$\overline{MR}$ Minimum Pulse Width			1			µs
$\overline{MR}$ Glitch Rejection				100		ns
$\overline{MR}$ to Reset Output Delay	t_{MR}			200		ns
$\overline{MR}$ Pullup Resistance			25	50	80	kΩ

ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}1 = V_{CC}2$ = +0.8V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

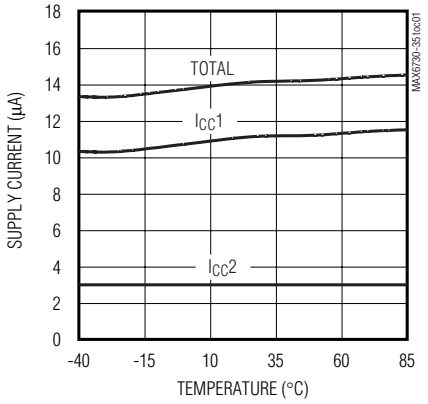
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
WATCHDOG INPUT						
Watchdog Timeout Period	t_{WD-L}	First watchdog period after reset timeout period	35	54	72	s
	t_{WD-S}	Normal mode	1.12	1.68	2.24	
WDI Pulse Width	t_{WDI}	(Note 3)	50			ns
WDI Input Voltage	V_{IL}				$0.3 \times V_{CC}1$	V
	V_{IH}		$0.7 \times V_{CC}1$			
WDI Input Current	I_{WDI}	WDI = 0 or $V_{CC}1$	-1		+1	µA
RESET/WATCHDOG OUTPUT						
$\overline{RST}$/$\overline{WDO}$ Output Low Voltage (Push-Pull or Open Drain)	V_{OL}	$V_{CC}1$ or $V_{CC}2$ +0.8V, I_{SINK} = 1µA, output asserted			0.3	V
		$V_{CC}1$ or $V_{CC}2$ +1.0V, I_{SINK} = 50µA, output asserted			0.3	
		$V_{CC}1$ or $V_{CC}2$ +1.2V, I_{SINK} = 100µA, output asserted			0.3	
		$V_{CC}1$ or $V_{CC}2$ +2.7V, I_{SINK} = 1.2mA, output asserted			0.3	
		$V_{CC}1$ or $V_{CC}2$ +4.5V, I_{SINK} = 3.2mA, output asserted			0.4	
$\overline{RST}$/$\overline{WDO}$ Output High Voltage (Push-Pull Only)	V_{OH}	$V_{CC}1$ +1.8V, I_{SOURCE} = 200µA, output not asserted	$0.8 \times V_{CC}1$			V
		$V_{CC}1$ +2.7V, I_{SOURCE} = 500µA, output not asserted	$0.8 \times V_{CC}1$			
		$V_{CC}1$ +4.5V, I_{SOURCE} = 800µA, output not asserted	$0.8 \times V_{CC}1$			
$\overline{RST}$/$\overline{WDO}$ Output Open-Drain Leakage Current		Output not asserted			0.5	µA

Note 2: Devices tested at T_A = +25°C. Overtemperature limits are guaranteed by design and not production tested.
Note 3: Parameter guaranteed by design.

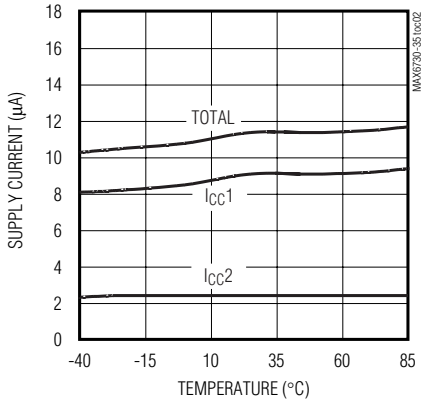
Typical Operating Characteristics

($V_{CC}1$ = +5V, $V_{CC}2$ = +3.3V, T_A = +25°C, unless otherwise noted.)

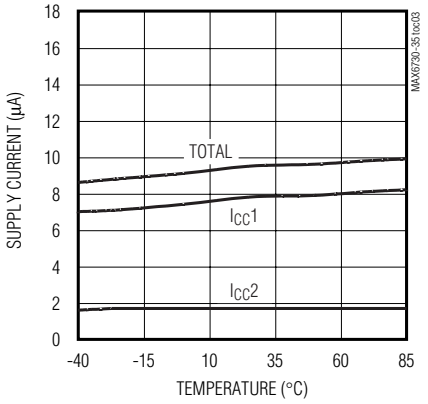
SUPPLY CURRENT vs. TEMPERATURE ($V_{CC}1$ = +5V, $V_{CC}2$ = +3.3V)



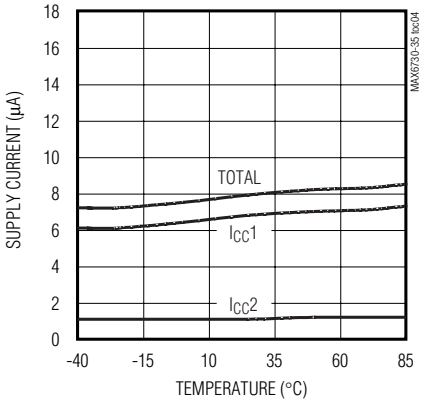
SUPPLY CURRENT vs. TEMPERATURE ($V_{CC}1$ = +3.3V, $V_{CC}2$ = +2.5V)



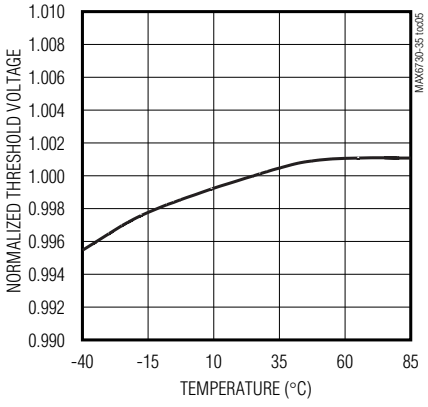
SUPPLY CURRENT vs. TEMPERATURE ($V_{CC}1$ = +2.5V, $V_{CC}2$ = +1.8V)



SUPPLY CURRENT vs. TEMPERATURE ($V_{CC}1$ = +1.8V, $V_{CC}2$ = +1.2V)



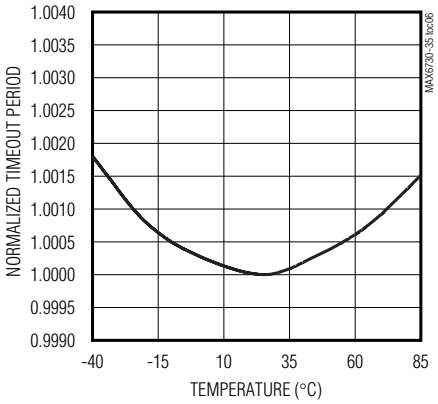
NORMALIZED THRESHOLD VOLTAGE vs. TEMPERATURE



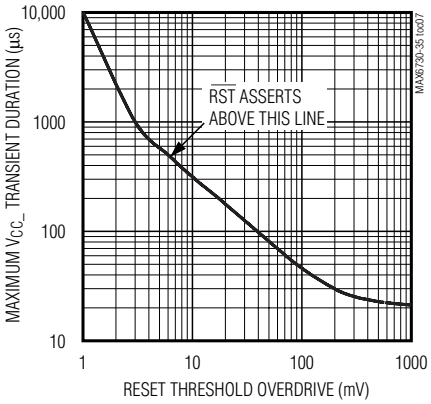
Typical Operating Characteristics (continued)

($V_{CC}1$ = +5V, $V_{CC}2$ = +3.3V, T_A = +25°C, unless otherwise noted.)

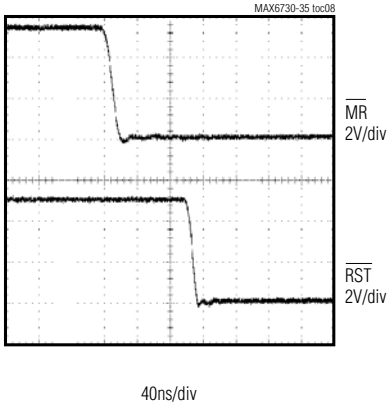
NORMALIZED TIMEOUT PERIOD vs. TEMPERATURE



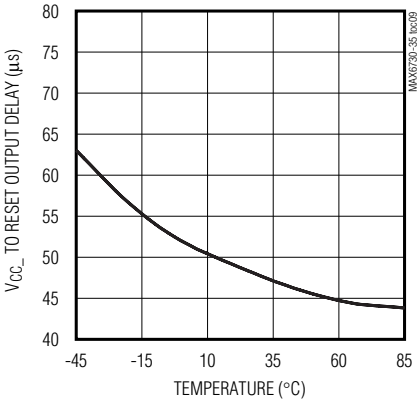
MAXIMUM V_{CC}_ TRANSIENT DURATION vs. RESET THRESHOLD OVERDRIVE



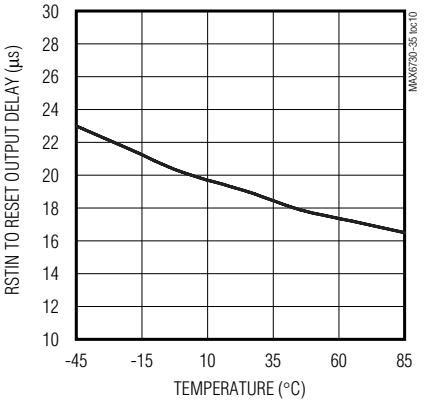
$\overline{MR}$ TO RESET OUTPUT DELAY



V_{CC}_ TO RESET OUTPUT DELAY vs. TEMPERATURE (100mV OVERDRIVE)



RSTIN TO RESET OUTPUT DELAY vs. TEMPERATURE



Pin Description

PIN			NAME	FUNCTION
MAX6730 MAX6731	MAX6732 MAX6733	MAX6734 MAX6735		
1	1	1	$\overline{RST}$	Active-Low Reset Output. The MAX6730/MAX6732/MAX6734 provide an open-drain output. The MAX6731/MAX6733/MAX6735 provide a push-pull output. $\overline{RST}$ asserts low when any of the following conditions occur: $V_{CC}1$ or $V_{CC}2$ drops below its preset threshold, RSTIN drops below its reset threshold, or $\overline{MR}$ is driven low. Open-drain versions require an external pullup resistor.
2	2	2	GND	Ground
3	3	4	$\overline{WDO}$	Active-Low Watchdog Output. The MAX6730/MAX6732/MAX6734 provide an open-drain $\overline{WDO}$ output. The MAX6731/MAX6733/MAX6735 provide a push-pull $\overline{WDO}$ output. $\overline{WDO}$ asserts low when no low-to-high or high-to-low transition occurs on WDI within the watchdog timeout period (t_{WD}) or if an undervoltage lockout condition exists for $V_{CC}1$, $V_{CC}2$, or RSTIN. $\overline{WDO}$ deasserts without a timeout period when $V_{CC}1$, $V_{CC}2$, and RSTIN exceed their reset thresholds, or when the manual reset input is asserted. Open-drain versions require an external pullup resistor.
4	—	5	$\overline{MR}$	Active-Low Manual Reset Input. Drive $\overline{MR}$ low to force a reset. $\overline{RST}$ remains asserted as long as $\overline{MR}$ is low and for the reset timeout period after $\overline{MR}$ releases high. $\overline{MR}$ has a 50kΩ pullup resistor to $V_{CC}1$; leave $\overline{MR}$ open or connect to $V_{CC}1$ if unused.
5	5	3	WDI	Watchdog Input. If WDI remains high or low for longer than the watchdog timeout period, the internal watchdog timer expires and the watchdog output asserts low. The internal watchdog timer clears whenever $\overline{RST}$ asserts or a rising or falling edge on WDI is detected. The watchdog has an initial watchdog timeout period (35s min) after each reset event and a short timeout period (1.12s min) after the first valid WDI transition. Leaving WDI unconnected does not disable the watchdog timer function.
6	6	8	$V_{CC}1$	Primary Supply-Voltage Input. $V_{CC}1$ provides power to the device when it is greater than $V_{CC}2$. $V_{CC}1$ is the input to the primary reset threshold monitor.
—	4	6	$V_{CC}2$	Secondary Supply-Voltage Input. $V_{CC}2$ provides power to the device when it is greater than $V_{CC}1$. $V_{CC}2$ is the input to the secondary reset threshold monitor.
—	—	7	RSTIN	Undervoltage Reset Comparator Input. RSTIN provides a high-impedance comparator input for the adjustable reset monitor. $\overline{RST}$ asserts low if the voltage at RSTIN drops below the 626mV internal reference voltage. Connect a resistive voltage-divider to RSTIN to monitor voltages higher than 626mV. Connect RSTIN to $V_{CC}1$ or $V_{CC}2$ if unused.

Single-/Dual-/Triple-Voltage µP Supervisory Circuits with Independent Watchdog Output

Table 1. Reset Voltage Threshold Suffix Guide**

PART NO. SUFFIX	$V_{CC}1$ NOMINAL VOLTAGE THRESHOLD(V)	$V_{CC}2$ NOMINAL VOLTAGE THRESHOLD (V)
LT	**4.625**	**3.075**
MS	4.375	2.925
MR	4.375	2.625
TZ	3.075	2.313
SY	**2.925**	**2.188**
RY	2.625	2.188
TW	3.075	1.665
SV	**2.925**	**1.575**
RV	**2.625**	**1.575**
TI	3.075	1.388
SH	**2.925**	**1.313**
RH	2.625	1.313
TG	**3.075**	**1.110**
SF	2.925	1.050
RF	2.625	1.050
TE	3.075	0.833
SD	**2.925**	**0.788**
RD	2.625	0.788
ZW	**2.313**	**1.665**
YV	2.188	1.575
ZI	2.313	1.388
YH	**2.188**	**1.313**
ZG	**2.313**	**1.110**
YF	2.188	1.050
ZE	2.313	0.833
YD	**2.188**	**0.788**
WI	1.665	1.388
VH	**1.575**	**1.313**
WG	**1.665**	**1.110**
VF	1.575	1.050
WE	1.665	0.833
VD	**1.575**	**0.788**

***Standard versions are shown in bold and are available in a D3 timeout option only. Standard versions require 2500-piece order increments and are typically held in sample stock. There is a 10,000-piece order increment on nonstandard versions.*
Other threshold voltages may be available; contact factory for availability.

Table 2. Reset Timeout Period Suffix Guide

TIMEOUT PERIOD SUFFIX	ACTIVE TIMEOUT PERIOD	
	MIN (ms)	MAX (ms)
D1	1.1	2.2
D2	8.8	17.6
D3	140	280
D5	280	560
D6	560	1120
D4	1120	2240

Detailed Description

Supply Voltages

The MAX6730–MAX6735 microprocessor (µP) supervisors maintain system integrity by alerting the µP to fault conditions. The MAX6730–MAX6735 monitor one to three supply voltages in µP-based systems and assert an active-low reset output when any monitored supply voltage drops below its preset threshold. The output state remains valid for $V_{CC}1$ or $V_{CC}2$ greater than +0.8V.

Threshold Levels

The two-letter code in the Reset Voltage Threshold Suffix Guide (Table 1) indicates the threshold level combinations for $V_{CC}1$ and $V_{CC}2$.

Reset Output

The MAX6730–MAX6735 feature an active-low reset output ($\overline{RST}$). $\overline{RST}$ asserts when the voltage at either $V_{CC}1$ or $V_{CC}2$ falls below the voltage threshold level, V_{RSTIN} drops below its threshold, or $\overline{MR}$ is driven low (Figure 1). $\overline{RST}$ remains low for the reset timeout period (Table 2) after $V_{CC}1$, $V_{CC}2$, and RSTIN increase above their respective thresholds and after $\overline{MR}$ releases high. Whenever $V_{CC}1$, $V_{CC}2$, or RSTIN go below the reset threshold before the end of the reset timeout period, the internal timer restarts. The MAX6730/MAX6732/ MAX6734 provide an open-drain $\overline{RST}$ output, and the MAX6731/ MAX6733/MAX6735 provide a push-pull $\overline{RST}$ output.

Manual Reset Input

Many µP-based products require manual reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. A logic low on $\overline{MR}$ asserts the reset output, clears the watchdog timer, and deasserts the watchdog output. Reset remains asserted while $\overline{MR}$ is low and for the reset timeout period (t_{RP}) after $\overline{MR}$ returns high. An internal 50kΩ pullup resistor allows $\overline{MR}$ to be left open if unused. Drive $\overline{MR}$ with TTL or CMOS-logic levels or with open-drain/collector outputs. Connect a normally open momentary switch from $\overline{MR}$ to GND to create a manual reset function; external debounce circuitry is not required. Connect a 0.1µF capacitor from $\overline{MR}$ to GND to provide additional noise immunity when driving $\overline{MR}$ over long cables or if the device is used in a noisy environment.

Adjustable Input Voltage (RSTIN)

The MAX6734/MAX6735 provide an additional high-impedance comparator input with a 626mV threshold to monitor a third supply voltage. To monitor a voltage higher than 626mV, connect a resistive-divider to the circuit as shown in Figure 2 to establish an externally controlled threshold voltage, V_{EXT_TH}.

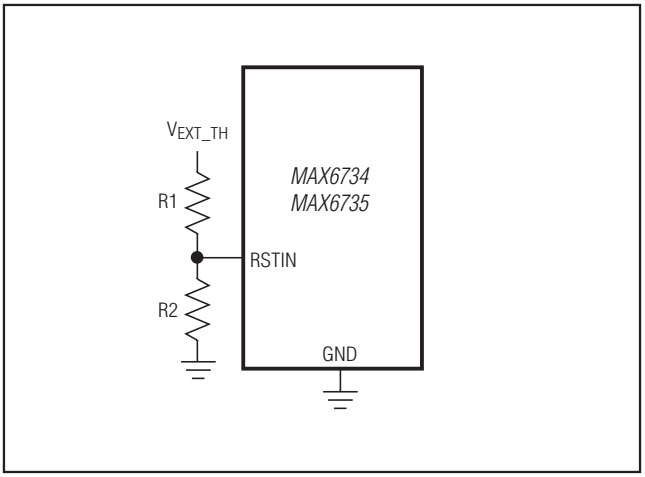


Figure 2. Monitoring a Third Voltage

$$V_{EXT\_TH} = 626mV \times \frac{(R1 + R2)}{R2}$$

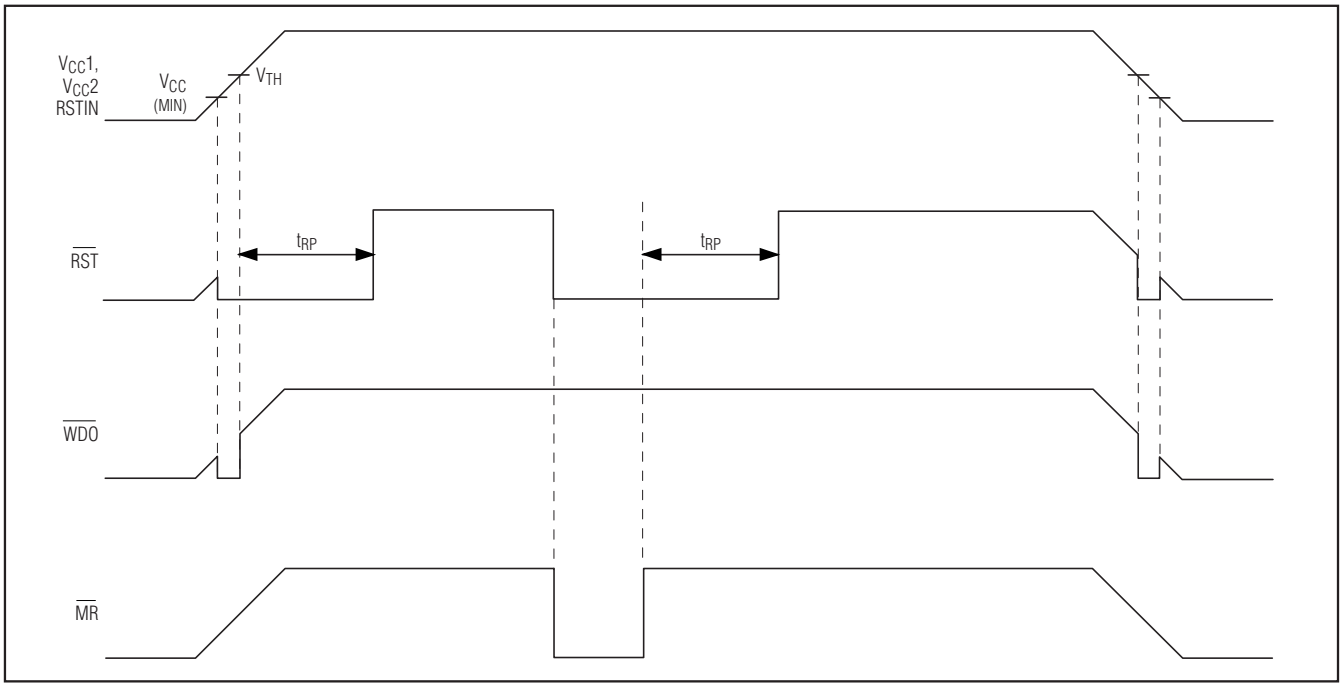


Figure 1. $\overline{RST}$, $\overline{WDO}$, and $\overline{MR}$ Timing Diagram

The RSTIN comparator derives power from $V_{CC}1$, and the input voltage must remain less than or equal to $V_{CC}1$. Low leakage current at RSTIN allows the use of large-valued resistors, resulting in reduced power consumption of the system.

Watchdog

The watchdog feature monitors µP activity through the watchdog input (WDI). A rising or falling edge on WDI within the watchdog timeout period (t_{WD}) indicates normal µP operation. $\overline{WDO}$ asserts low if WDI remains high or low for longer than the watchdog timeout period. Leaving WDI unconnected does not disable the watchdog timer.

The MAX6730–MAX6735 include a dual-mode watchdog timer to monitor µP activity. The flexible timeout architecture provides a long-period initial watchdog mode, allowing complicated systems to complete lengthy boots, and a short-period normal watchdog mode, allowing the supervisor to provide quick alerts when processor activity fails. After each reset event (V_{CC} power-up, brownout, or manual reset), there is a long initial watchdog period of 35s (min). The long watchdog period mode provides an extended time for the system to power up and fully initialize all µP and system components before assuming responsibility for routine watchdog updates.

The usual watchdog timeout period (1.12s min) begins after the initial watchdog timeout period (t_{WD-L}) expires or after the first transition on WDI (Figure 3). During normal operating mode, the supervisor asserts the $\overline{WDO}$ output if the µP does not update the WDI with a valid transition (high to low or low to high) within the standard timeout period (t_{WD-S}) (1.12s min).

Connect $\overline{MR}$ to $\overline{WDO}$ to force a system reset in the event that no rising or falling edge is detected at WDI within the watchdog timeout period. $\overline{WDO}$ asserts low when no edge is detected by WDI, the $\overline{RST}$ output asserts low, the watchdog counter immediately clears, and $\overline{WDO}$ returns high. The watchdog counter restarts, using the long watchdog period, when the reset timeout period ends (Figure 4).

Ensuring a Valid RESET Output Down to V_{CC} = 0V

The MAX6730–MAX6735 guarantee proper operation down to V_{CC} = +0.8V. In applications that require valid reset levels down to V_{CC} = 0V, use a 100kΩ pulldown resistor from $\overline{RST}$ to GND. The resistor value used is not critical, but it must be large enough not to load the reset output when V_{CC} is above the reset threshold. For most applications, 100kΩ is adequate. Note that this configuration does not work for the open-drain outputs of MAX6730/MAX6732/MAX6734.

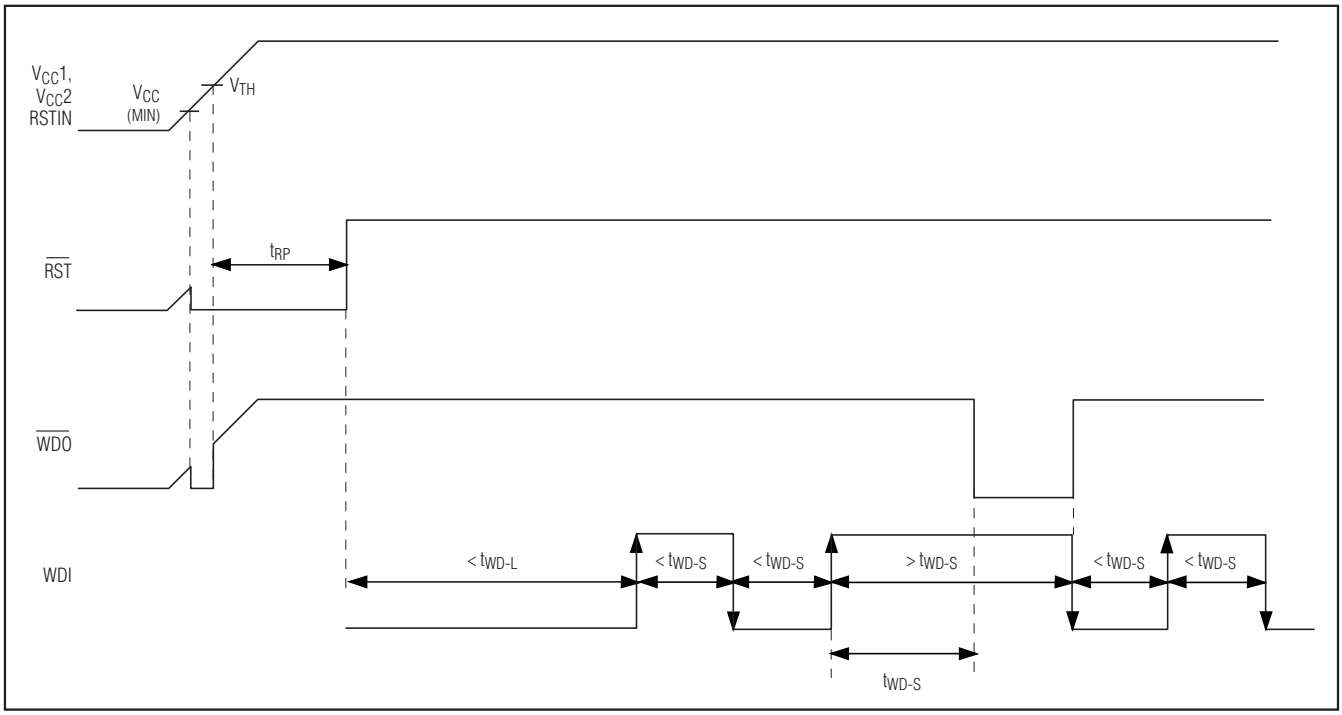


Figure 3. Watchdog Input/Output Timing Diagram ($\overline{MR}$ and $\overline{WDO}$ Not Connected)

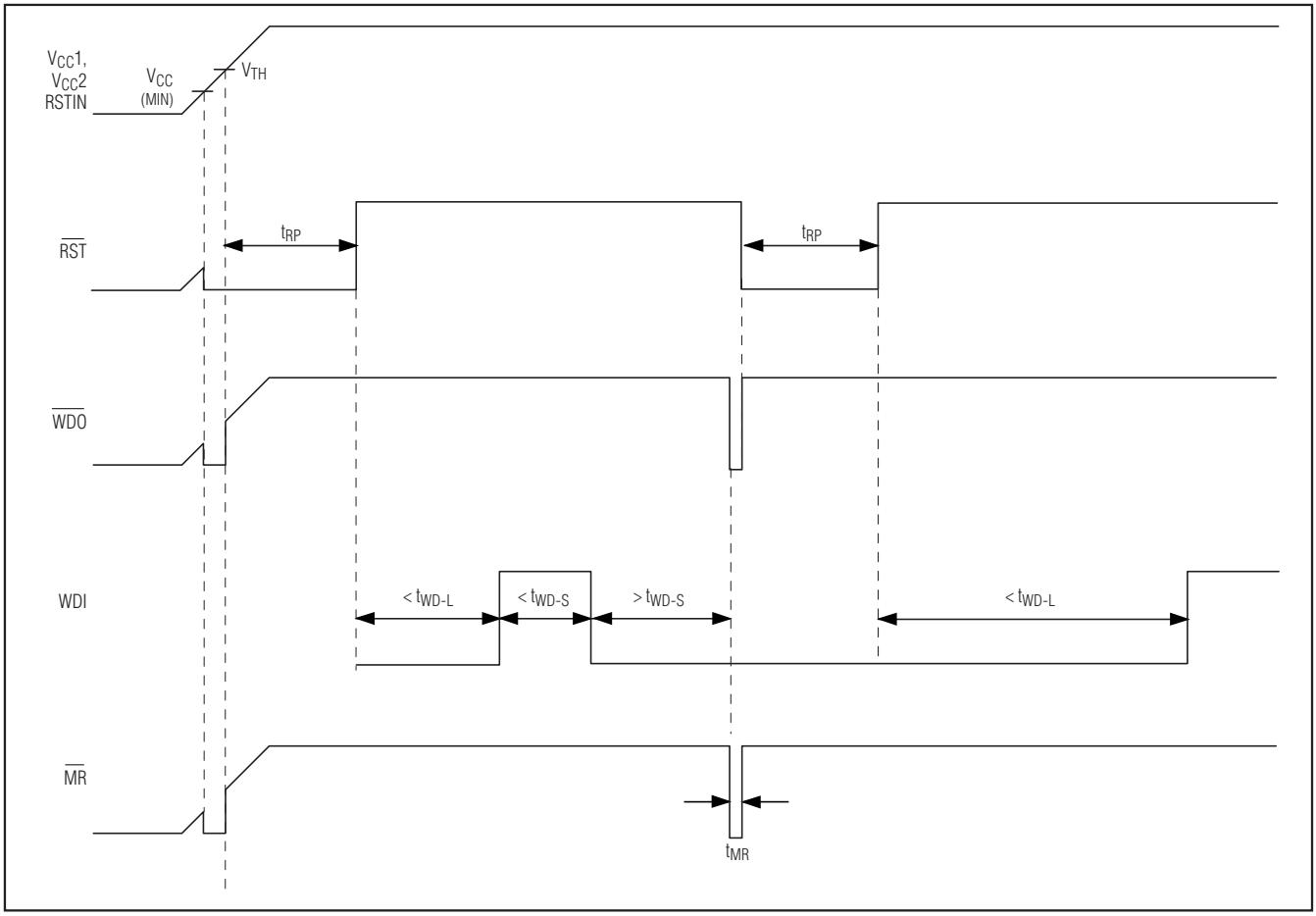


Figure 4. Watchdog Input/Output Timing Diagram (MR and WDO Connected)

Applications Information

Interfacing to µPs with Bidirectional Reset Pins

Microprocessors with bidirectional reset pins can interface directly with the open-drain RST output options. However, conditions might occur in which the push-pull output versions experience logic contention with the bidirectional reset pin of the µP. Connect a 10kΩ resistor between RST and the µP's reset I/O port to prevent logic contention (Figure 5).

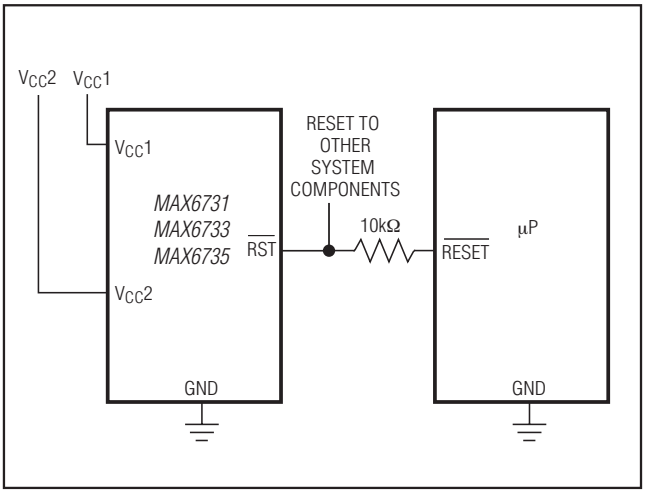


Figure 5. Interfacing to µPs with Bidirectional Reset I/O

Falling VCC Transients

The MAX6730–MAX6735 µP supervisors are relatively immune to short-duration falling VCC_ transients (glitches). Small glitches on VCC_ are ignored by the MAX6730–MAX6735, preventing undesirable reset pulses to the µP. The *Typical Operating Characteristics* show Maximum Transient Duration vs. Reset Threshold

Overdrive, for which reset pulses are not generated. The graph was produced using falling $V_{CC\_}$ pulses, starting above V_{TH} and ending below the reset threshold by the magnitude indicated (reset threshold overdrive). The graph shows the maximum pulse width that a falling V_{CC} transient typically might have without causing a reset pulse to be issued. As the amplitude of the transient increases (i.e., goes further below the reset threshold), the maximum allowable pulse width decreases. A 0.1µF bypass capacitor mounted close to $V_{CC\_}$ provides additional transient immunity.

Watchdog Software Considerations

Setting and resetting the watchdog input at different points in the program rather than "pulsing" the watchdog input high-low-high or low-high-low helps the watchdog timer closely monitor software execution. This technique avoids a "stuck" loop, in which the watchdog timer continues to be reset within the loop, preventing the watchdog from timing out. Figure 6 shows an example flow diagram in which the I/O driving the watchdog input is set high at the beginning of the program, set low at the beginning of every subroutine or loop, and then set high again when the program returns to the beginning. If the program "hangs" in any subroutine, the I/O continually asserts low (or high), and the watchdog timer expires, issuing a reset or interrupt.

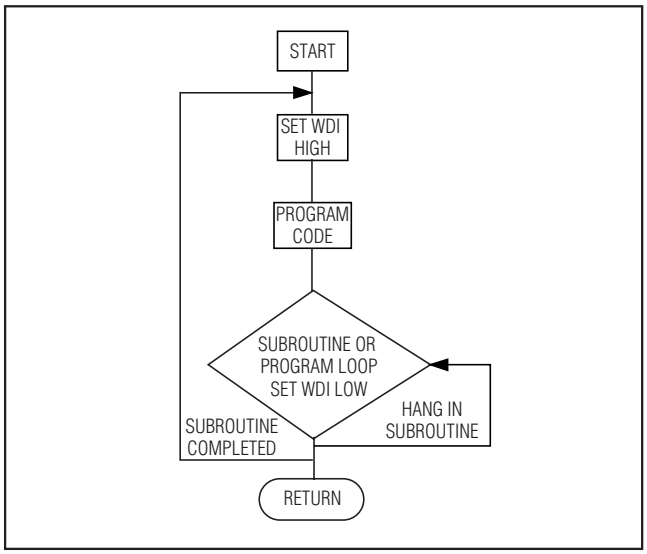
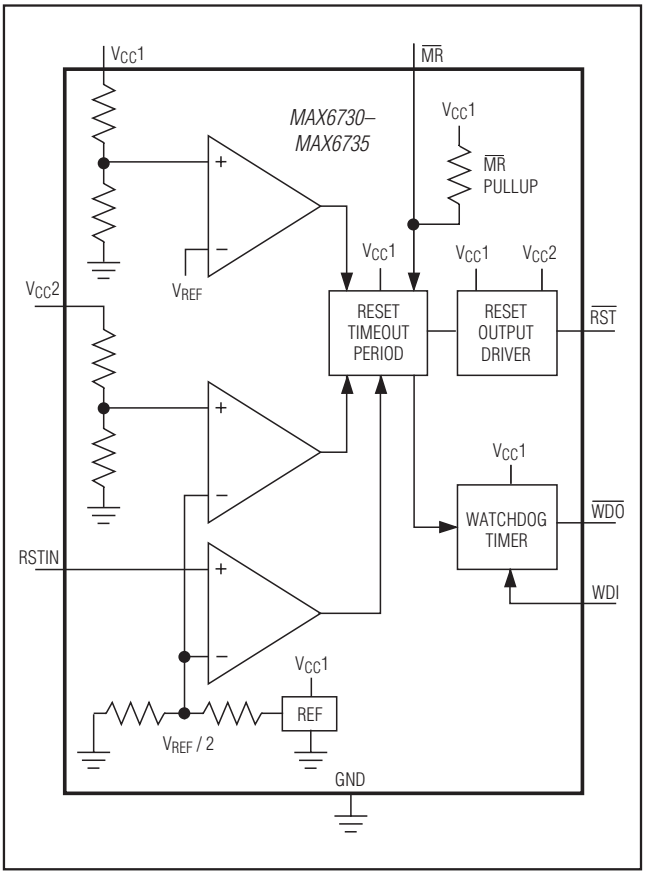


Figure 6. Watchdog Flow Diagram

Functional Diagram



Standard Versions

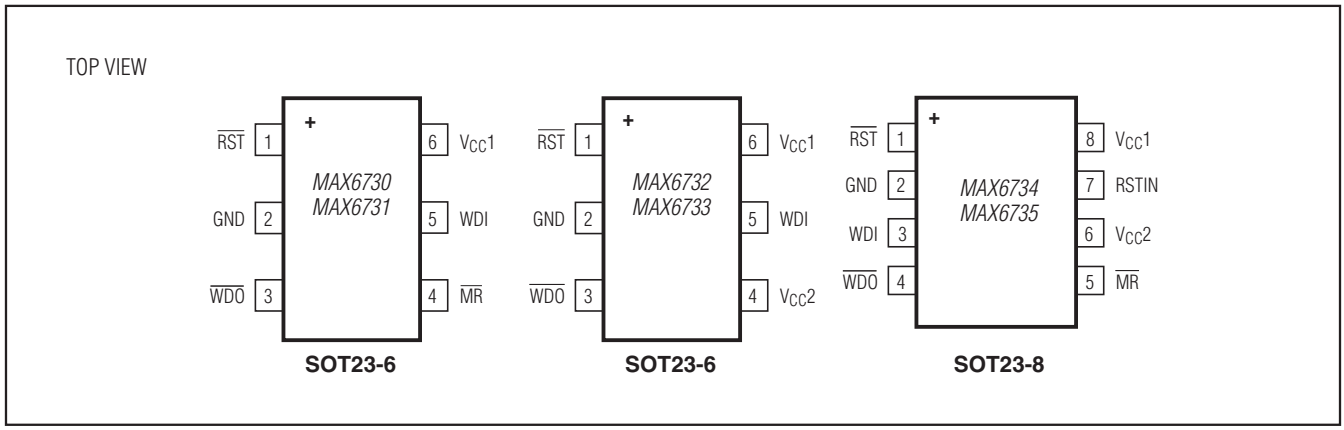
PART	TOP MARK
MAX6730UTLD3-T	ABCC
MAX6730UTSD3-T	ABPB
MAX6730UTRD3-T	ABPA
MAX6730UTZD3-T	ABPD
MAX6730UTVD3-T	ABPC
MAX6731UTLD3-T	ABPE
MAX6731UTTD3-T	ABCD
MAX6731UTSD3-T	ABPG
MAX6731UTRD3-T	ABPF
MAX6731UTZD3-T	ABPI
MAX6731UTVD3-T	ABPH
MAX6732UTLTD3-T	ABCE
MAX6732UTSYD3-T	ABPN
MAX6732UTSVD3-T	ABPM
MAX6732UTRVD3-T	ABPJ
MAX6732UTSHD3-T	ABPL
MAX6732UTTGD3-T	ABPO
MAX6732UTSDD3-T	ABPK
MAX6732UTZWD3-T	ABPV
MAX6732UTYHD3-T	ABPT
MAX6732UTZGD3-T	ABPU
MAX6732UTYDD3-T	ABPS
MAX6732UTVHD3-T	ABPQ
MAX6732UTWGD3-T	ABPR
MAX6732UTVDD3-T	ABPP
MAX6733UTLTD3-T	ABPW
MAX6733UTSYD3-T	ABQB
MAX6733UTSVD3-T	ABQA
MAX6733UTRVD3-T	ABPX
MAX6733UTSHD3-T	ABPZ
MAX6733UTTGD3-T	ABQC
MAX6733UTSDD3-T	ABPY
MAX6733UTZWD3-T	ABQJ
MAX6733UTYHD3-T	ABQH

PART	TOP MARK
MAX6733UTZGD3-T	ABQI
MAX6733UTYDD3-T	ABQG
MAX6733UTVHD3-T	ABQE
MAX6733UTWGD3-T	ABQF
MAX6733UTVDD3-T	ABQD
MAX6734KALTD3-T	AEHN
MAX6734KASYD3-T	AEHS
MAX6734KASVD3-T	AEHR
MAX6734KARVD3-T	AEHO
MAX6734KASHD3-T	AEHQ
MAX6734KATGD3-T	AEHT
MAX6734KASDD3-T	AEHP
MAX6734KAZWD3-T	AEIA
MAX6734KAYHD3-T	AEHY
MAX6734KAZGD3-T	AEHZ
MAX6734KAYDD3-T	AEHX
MAX6734KAVHD3-T	AEHV
MAX6734KAWGD3-T	AEHW
MAX6734KAVDD3-T	AEHU
MAX6735KALTD3-T	AEIB
MAX6735KASYD3-T	AEIG
MAX6735KASVD3-T	AEIF
MAX6735KARVD3-T	AEIC
MAX6735KASHD3-T	AEIE
MAX6735KATGD3-T	AEIH
MAX6735KASDD3-T	AEID
MAX6735KAZWD3-T	AEIO
MAX6735KAZID3-T	AAJZ
MAX6735KAYHD3-T	AEIM
MAX6735KAZGD3-T	AEIN
MAX6735KAYDD3-T	AEIL
MAX6735KAVHD3-T	AEIJ
MAX6735KAWGD3-T	AEIK
MAX6735KAVDD3-T	AEII

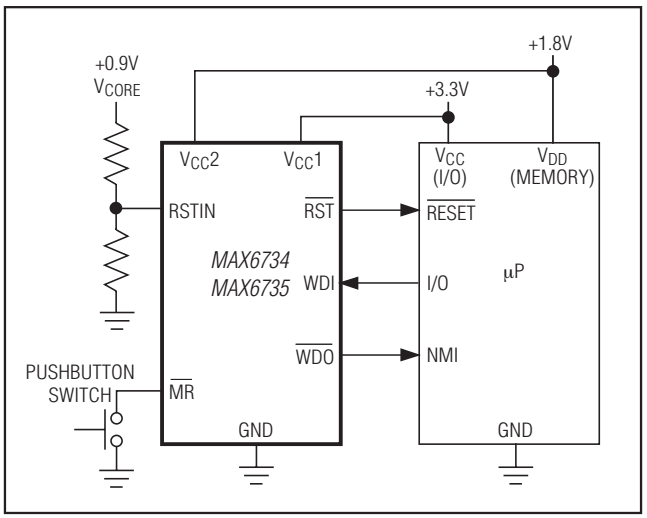
Note: *Sample stock is generally held on standard versions only. Standard versions have an order increment requirement of 2500 pieces. Nonstandard versions have an order increment requirement of 10,000 pieces. Contact factory for availability of nonstandard versions.*

Single-/Dual-/Triple-Voltage µP Supervisory Circuits with Independent Watchdog Output

Pin Configurations



Typical Operating Circuit



Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
6 SOT23	U6-1	21-0058	90-0175
8 SOT23	K8SN-1	21-0078	90-0176

Selector Guide

PART NUMBER	VOLTAGE MONITORS	$\overline{RST}$ OUTPUT	MANUAL RESET	WATCHDOG INPUT	WATCHDOG OUTPUT
MAX6730	1	Open Drain	√	√	Open Drain
MAX6731	1	Push-Pull	√	√	Push-Pull
MAX6732	2	Open Drain	—	√	Open Drain
MAX6733	2	Push-Pull	—	√	Push-Pull
MAX6734	3	Open Drain	√	√	Open Drain
MAX6735	3	Push-Pull	√	√	Push-Pull

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/02	Initial release.	—
1	12/02	Released MAX6730/MAX6731.	1
2	1/03	Released MAX6733.	1
3	3/04	Updated *Typical Operating Circuit*.	14
4	12/05	Added lead-free notation *to Ordering Information*.	1
5	3/09	Updated *Pin Description* and added *Package Table*.	7, 14
6	11/11	Added automotive-qualified part information	1
7	4/13	Added *Package Thermal Characteristics* and corrected power dissipation errors and package code for 8 SOT23	2–4, 14

Mouser Electronics

Authorized Distributor

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Maxim Integrated:

MAX6730UTLD3+T MAX6730UTSD2+T MAX6730UTSD3+T MAX6730UTTD3+T MAX6731UTTD3+T MAX6735KALTD3+T MAX6735KARVD3+T MAX6735KASHD3+T MAX6735KASVD3+T MAX6735KASYD3+T MAX6735KATGD3+T MAX6730UTRD3+T MAX6731UTLD3+T