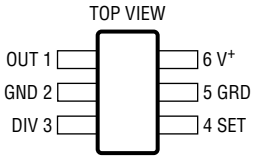
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V^+ ..... –0.3V to 6V
DIV to GND ..... –0.3V to (V^+ + 0.3V)
SET to GND ..... –0.3V to (V^+ + 0.3V)
GRD to GND ..... –0.3V to (V^+ + 0.3V)
Operating Temperature Range (Note 7)
  LTC6906C ..... –40°C to 85°C
  LTC6906I ..... –40°C to 85°C
  LTC6906H ..... –40°C to 125°C
Specified Temperature Range (Note 7)
  LTC6906C ..... 0°C to 70°C
  LTC6906I ..... –40°C to 85°C
  LTC6906H ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



S6 PACKAGE
6-LEAD PLASTIC TSOT-23
T_{JMAX} = 150°C, θ_{JA} = 230°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC6906CS6#PBF	LTC6906CS6#TRPBF	LTBJN	6-Lead Plastic TSOT-23	0°C to 70°C
LTC6906IS6#PBF	LTC6906IS6#TRPBF	LTBJN	6-Lead Plastic TSOT-23	–40°C to 85°C
LTC6906HS6#PBF	LTC6906HS6#TRPBF	LTBJN	6-Lead Plastic TSOT-23	–40°C to 125°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING***	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LTC6906CS6	LTC6906CS6#TR	LTBJN	6-Lead Plastic TSOT-23	0°C to 70°C
LTC6906IS6	LTC6906IS6#TR	LTBJN	6-Lead Plastic TSOT-23	–40°C to 85°C
LTC6906HS6	LTC6906HS6#TR	LTBJN	6-Lead Plastic TSOT-23	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Δf	Frequency Accuracy (Notes 2, 3, 9)	V^+ = 2.7V to 3.6V	100kHz ≤ f ≤ 1MHz			±0.25	±0.5	%
			100kHz ≤ f ≤ 1MHz, LTC6906C	●			±0.65	%
			100kHz ≤ f ≤ 1MHz, LTC6906I	●			±1.3	%
			f = 1MHz, LTC6906H	●			±1.3	%
			f = 100kHz, LTC6906H	●			±2.2	%
		V^+ = 2.25V	100kHz ≤ f ≤ 1MHz			±0.25	±0.7	%
			100kHz ≤ f ≤ 1MHz, LTC6906C	●			±0.85	%
			100kHz ≤ f ≤ 1MHz, LTC6906I	●			±1.3	%
			f = 1MHz, LTC6906H	●			±1.3	%
			f = 100kHz, LTC6906H	●			±2.2	%

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
R_{SET}	Frequency-Setting Resistor Range			●	100		1000	kΩ
Δf/ΔT	Frequency Drift Over Temp (Note 3)	R_{SET} = 316k		●		±0.005		%/°C
Δf/ΔV	Frequency Drift Over Supply (Note 3)	V^+ = 2.25V to 3.6V, 100k ≤ R_{SET} ≤ 1000k				0.06		%/V
	Timing Jitter (Note 4)	Pin 3 = V^+, 100k ≤ R_{SET} ≤ 1000k Pin 3 = Open, 100k ≤ R_{SET} ≤ 1000k Pin 3 = 0V, 100k ≤ R_{SET} ≤ 1000k				0.03 0.07 0.15		% % %
S_f	Long-Term Stability of Output Frequency	Pin 3 = V^+				300		ppm/√kHr
DC	Duty Cycle			●	45	50	55	%
V^+	Operating Supply Range (Note 8)			●	2.25		3.6	V
I_S	Power Supply Current	R_{SET} = 1000k, Pin 3 = 0V, R_L = 10M (DIV = 1, f_{OUT} = 100kHz)	V^+ = 3.6V V^+ = 2.25V	● ●		12.5 10.0	18 15	µA µA
		R_{SET} = 100k, Pin 3 = 0V, R_L = 10M (DIV = 1, f_{OUT} = 1MHz)	V^+ = 3.6V V^+ = 2.25V	● ●		78 60	100 80	µA µA
V_{IH}	High Level DIV Input Voltage		V^+ = 3.6V V^+ = 2.25V	● ●	3.1 2.05			V V
V_{IL}	Low Level DIV Input Voltage		V^+ = 3.6V V^+ = 2.25V	● ●			0.5 0.2	V V
I_{DIV}	DIV Input Current (Note 5)	Pin 3 = V^+ Pin 3 = 0V		● ●	 –2	1 –1	2	µA µA
V_{OH}	High Level Output Voltage (Note 5)	V^+ = 3.6V	I_{OH} = –100µA I_{OH} = –1mA	● ●	3.40 2.80	3.59 3.30		V V
		V^+ = 2.25V	I_{OH} = –100µA I_{OH} = –1mA	● ●	2.15 1.75	2.2 2.0		V V
V_{OL}	Low Level Output Voltage (Note 5)	V^+ = 3.6V	I_{OL} = 100µA I_{OL} = 1mA	● ●		0.02 0.15	0.2 0.8	V V
		V^+ = 2.25V	I_{OL} = 100µA I_{OL} = 1mA	● ●		0.03 0.30	0.1 0.5	V V
t_r	OUT Rise Time (Note 6)	V^+ = 3.6V V^+ = 2.25V				10 25		ns ns
t_f	OUT Fall Time (Note 6)	V^+ = 3.6V V^+ = 2.25V				10 25		ns ns
VGS	GRD Pin Voltage Relative to SET Pin Voltage	–10µA ≤ I_{GRD} ≤ 0.3µA		●	–10		10	mV

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Some frequencies may be generated using two different values of R_{SET}. For these frequencies, the error is specified assuming that the larger value of R_{SET} is used.

Note 3: Frequency accuracy is defined as the deviation from the f_{OUT} equation.

Note 4: Jitter is the ratio of the peak-to-peak deviation of the period to the mean of the period. This specification is based on characterization and is not 100% tested.

Note 5: Current into a pin is given as a positive value. Current out of a pin is given as a negative value.

Note 6: Output rise and fall times are measured between the 10% and 90% power supply levels.

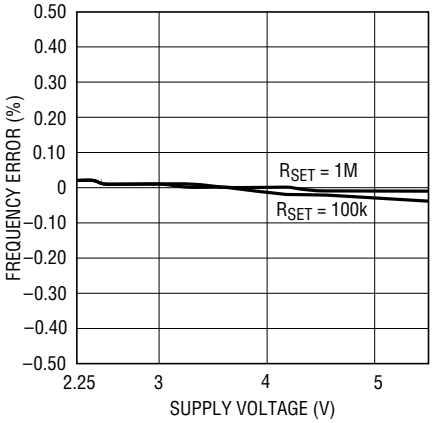
Note 7: The LTC6906C is guaranteed to meet specified performance from 0°C to 70°C. The LTC6906C is designed, characterized and expected to meet specified performance from –40°C to 85°C but is not tested or QA sampled at these temperatures. The LTC6906I is guaranteed to meet specified performance from –40°C to 85°C.

Note 8: Consult the Applications Information section for operation with supplies higher than 3.6V.

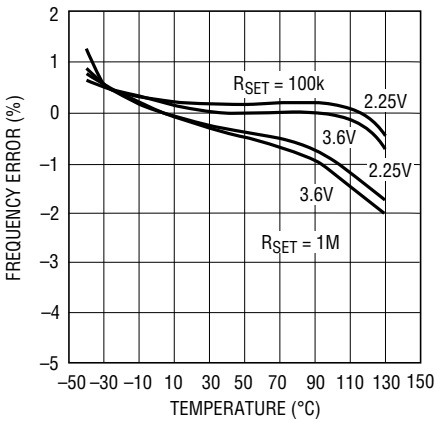
Note 9: Test conditions reflect the master oscillator frequency. The output divider is functionally tested and divided frequency accuracy is guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

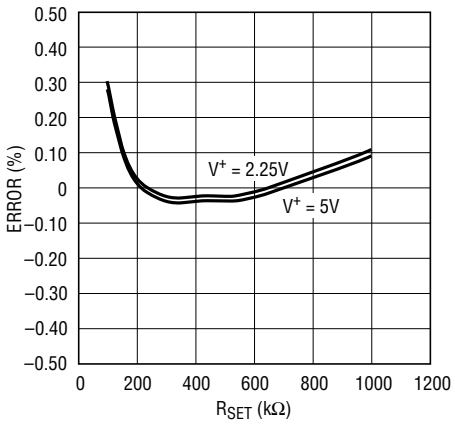
Typical Frequency Error vs Power Supply



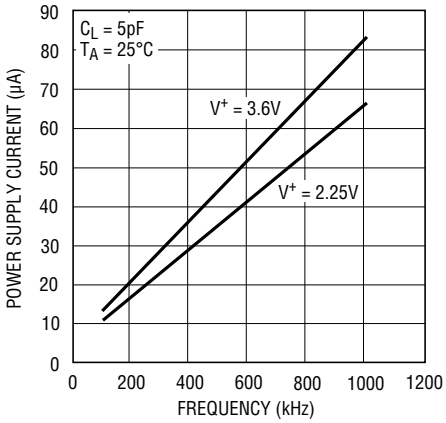
Typical Frequency Error vs Temperature



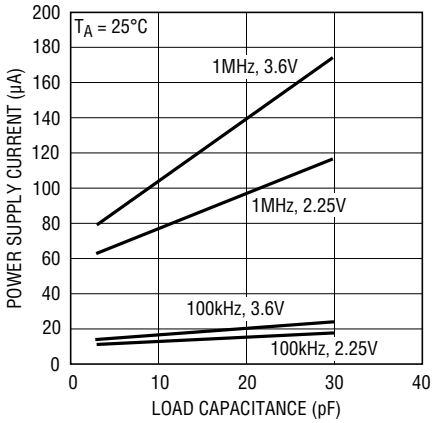
Typical Frequency Error vs R_{SET}



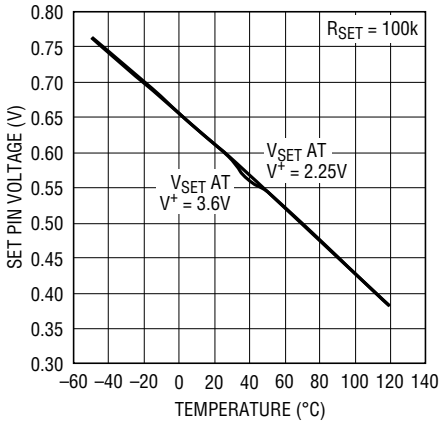
Typical Supply Current vs Frequency



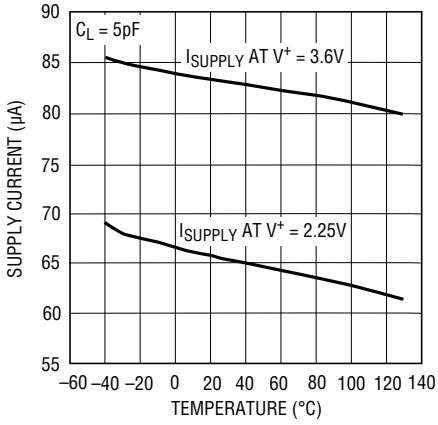
Typical Supply Current vs Load Capacitance



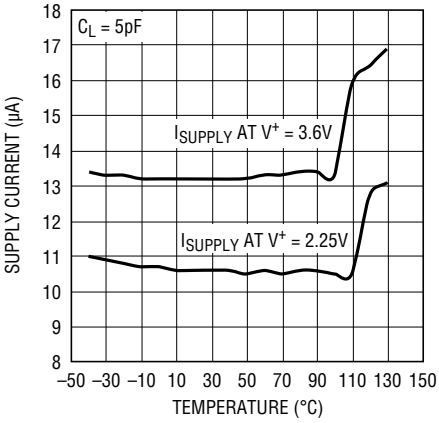
V_{SET} vs Temperature (V_{SET} is the Voltage Measured at the R_{SET} Pin)



Typical Supply Current vs Temperature, 1MHz



Typical Supply Current vs Temperature, 100kHz



PIN FUNCTIONS

OUT (Pin 1): Oscillator Output. The OUT pin swings from GND to V^+ with an output resistance of approximately 150Ω. For micropower operation, the load resistance must be kept as high as possible and the load capacitance as low as possible.

GND (Pin 2): Ground.

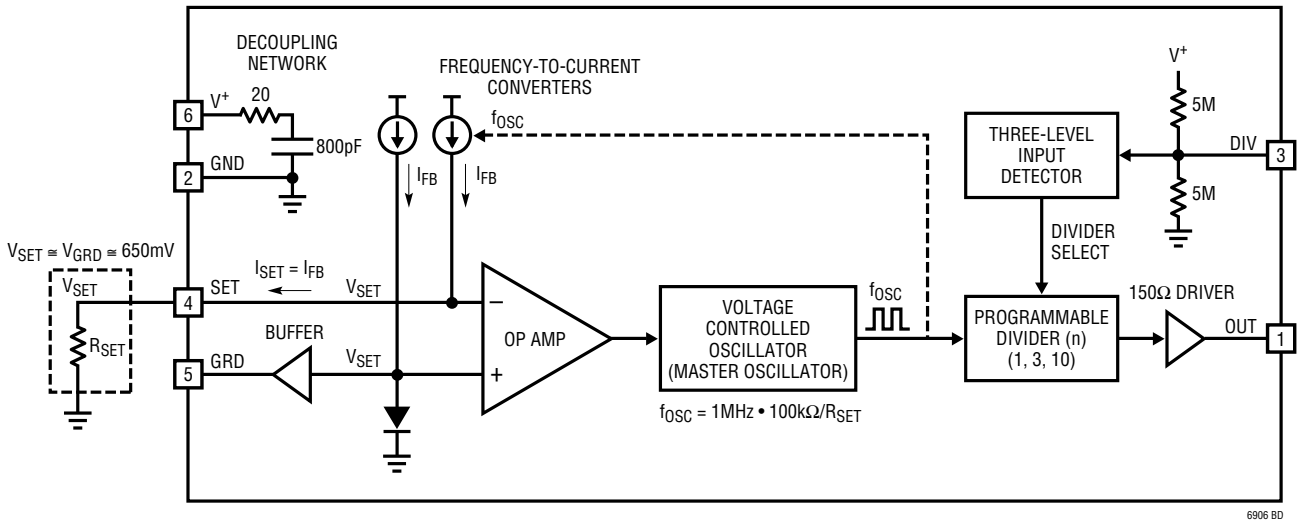
DIV (Pin 3): Divider Setting Input. This three-level input selects one of three internal digital divider settings, determining the value of N in the frequency equation. Tie to GND for ÷1, leave floating for ÷3 and tie to V^+ for ÷10. When left floating, the LTC6906 pulls Pin 3 to mid-supply with a 2.5M resistor. When Pin 3 is floating, care should be taken to reduce coupling from the OUT pin and its trace to Pin 3. Coupling can be reduced by increasing the physical space between traces or by shielding the DIV pin with grounded metal.

SET (Pin 4): Frequency Setting Resistor Input. Connect a resistor, R_{SET}, from this pin to GND to set the oscillator frequency. For best performance use a precision metal- or thin-film resistor of 0.5% or better tolerance and 50ppm/°C or better temperature coefficient. For lower accuracy applications, an inexpensive 1% thick-film resistor may be used. Limit the capacitance in parallel with R_{SET} to less than 10pF to reduce jitter and to ensure stability. Capacitance greater than 10pF could cause the LTC6906 internal feedback circuits to oscillate. The voltage on the SET pin is approximately 650mV and decreases with temperature by about –2.2mV/°C.

GRD (Pin 5): Guard Signal. This pin can be used to reduce PC board leakage across the frequency setting resistor, R_{SET}. The GRD pin is held within a few millivolts of the SET pin and shunts leakage current away from the SET pin. To control leakage, connect a bare copper trace (a trace with no solder mask) to GRD and loop it around the SET pin and all PC board metal connected to SET.

V^+ (Pin 6): Voltage Supply (2.25V to 3.6V). This supply is internally decoupled with a 20Ω resistor in series with an 800pF capacitor. No external decoupling capacitor is required for OUT pin loads less than 50pF. V^+ should be kept reasonably free of noise and ripple.

BLOCK DIAGRAM



TEST CIRCUIT

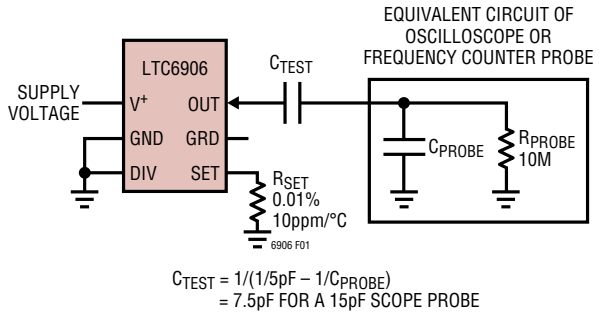


Figure 1. Test Circuit with 5pF Effective Load

EQUIVALENT INPUT AND OUTPUT CIRCUITS

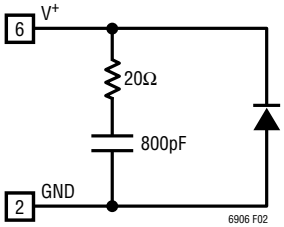


Figure 2. V+ Pin

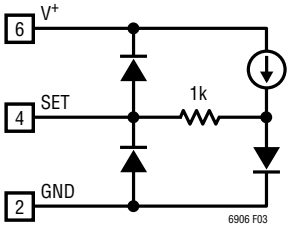


Figure 3. SET Pin

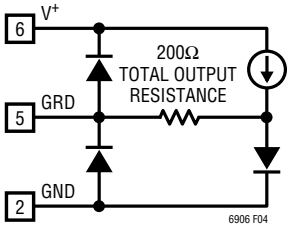


Figure 4. GRD Pin

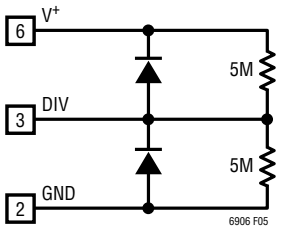


Figure 5. DIV Pin

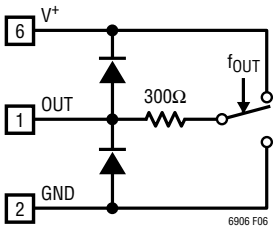


Figure 6. OUT Pin

THEORY OF OPERATION

The LTC6906 is a precision, resistor programmable oscillator (see the Block Diagram). It generates a square wave at the OUT pin with a period directly proportional to the value of an external resistor, R_{SET}. A feedback circuit measures and controls the oscillator frequency to achieve the highest possible accuracy. In equilibrium, this circuit ensures that the current in the SET pin, I_{SET}, is balanced by I_{FB}. I_{FB} is proportional to the master oscillator frequency, so we have the relationship:

$$I_{SET} = I_{FB} = V_{SET} \bullet f_{OSC} \bullet C_{OSC} \quad (1)$$

where C_{OSC} is a precision internal capacitor:

C_{OSC} = 10pF for the LTC6906

Solving for the oscillator period:

$$t_{OSC} = \frac{1}{f_{OSC}} = \frac{V_{SET}}{I_{SET}} \bullet C_{OSC} \quad (2)$$

This is the fundamental equation for the LTC6906. It holds regardless of how the SET pin is driven. When a resistor, R_{SET}, is connected from the SET pin to ground, we have the relationship:

$$\frac{V_{SET}}{I_{SET}} = R_{SET} \quad (3)$$

so

$$t_{OSC} = \frac{1}{f_{OSC}} = R_{SET} \bullet C_{OSC} \quad (4)$$

The period and frequency are determined exclusively by R_{SET} and the precision internal capacitor. Importantly, the value of V_{SET} is immaterial, and the LTC6906 maintains its accuracy even though V_{SET} is not a precision reference voltage.

The digital dividers shown in the Block Diagram further divide the master oscillator frequency by 1, 3 or 10 producing:

$$f_{OUT} = \frac{f_{OSC}}{N} \quad (5)$$

and

$$t_{OUT} = N \bullet t_{OSC} \quad (6)$$

Table 1 gives specific frequency and period equations for the LTC6906. The Applications Information section gives further detail and discusses alternative ways of setting the LTC6906 output frequency.

Table 1. Output Frequency Equations

PART NUMBER	FREQUENCY	PERIOD	DIVIDER RATIOS
LTC6906	$f_{OUT} = \frac{1MHz}{N} \bullet \left(\frac{100k}{R_{SET}}\right)$	$t_{OUT} = N \bullet 1\mu s \bullet \left(\frac{R_{SET}}{100k}\right)$	$N = \begin{cases} 10, & DIV\ Pin = V^+ \\ 3, & DIV\ Pin = Open \\ 1, & DIV\ Pin = GND \end{cases}$

APPLICATIONS INFORMATION

Selecting R_{SET} and the Divider Ratio

The LTC6906 contains a master oscillator followed by a digital divider (see the Block Diagram). R_{SET} determines the master oscillator frequency and the DIV pin sets the divider ratio, N. The range of frequencies accessible in each divider ratio overlap, as shown in Figure 7. This figure is derived from the equations in Table 1. ***For any given frequency, power can be minimized by minimizing the master oscillator frequency. This implies maximizing R_{SET} and using the lowest possible divider ratio, N***. The relationship between R_{SET}, N and the unloaded power consumption is shown in Figure 8, where we can clearly see that supply current decreases for large values of R_{SET}. For a discussion of jitter and divide ratio, refer to page 11.

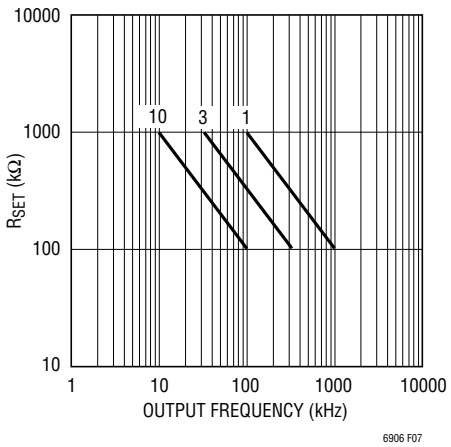


Figure 7. R_{SET} vs Desired Output Frequency (LTC6906)

Minimizing Power Consumption

The supply current of the LTC6906 has four current components:

- Constant (Independent V^+, f_{OUT} and C_{LOAD})
- Proportional to I_{SET} (which is the current in R_{SET})
- Proportional to V^+, f_{OUT} and C_{LOAD}
- Proportional to V^+ and R_{LOAD}

An approximate expression for the total supply current is:

$$I^+ \cong 5\mu A + 6 \bullet I_{SET} + V^+ \bullet f_{OUT} \bullet (C_{LOAD} + 5pF) + \frac{V^+}{2 \bullet R_{LOAD}}$$

$$\cong 5\mu A + 6 \bullet \frac{V_{SET}}{R_{SET}} + V^+ \bullet f_{OUT} \bullet (C_{LOAD} + 5pF) + \frac{V^+}{2 \bullet R_{LOAD}}$$

V_{SET} is approximately 650mV at 25°C, but varies with temperature. This behavior is shown in the Typical Performance Characteristics section.

Power can be minimized by maximizing R_{SET}, minimizing the load on the OUT pin and operating at lower frequencies. Figure 9 shows total supply current vs frequency under typical conditions. Below 100kHz the load current is negligible for the 5pF load shown.

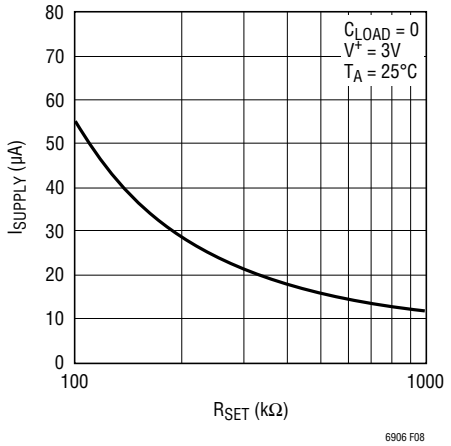


Figure 8. Unloaded Supply Current vs R_{SET}

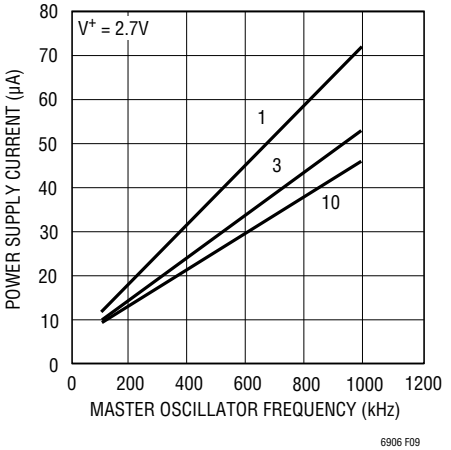


Figure 9. Supply Current vs Frequency

APPLICATIONS INFORMATION

Guarding Against PC Board Leakage

The LTC6906 uses relatively large resistance values for R_{SET} to minimize power consumption. For R_{SET} = 1M, the SET pin current is typically only 0.65µA. Thus, only 0.65nA leaking into the SET pin causes a 0.1% frequency error. Similarly, 1G of leakage resistance across R_{SET} (1000 • R_{SET}) causes the same 0.1% error.

Achieving the highest accuracy requires controlling potential leakage paths. PC board leakage is aggravated by both dirt and moisture. Effective cleaning is a good first step to minimizing leakage, and some PC board manufacturers offer high impedance or low leakage processing options.

Another effective method for controlling leakage is to shunt the leakage current away from the sensitive node through a low impedance path. The LTC6906 provides a signal on the GRD pin for this purpose. Figure 10 shows a PC board layout that uses the GRD pin and a "guard ring" to absorb leakage currents. The guard ring surrounds the SET pin and the end of R_{SET} to which it is connected. The guard ring must have no solder mask covering it to be effective. The GRD pin voltage is held within a few millivolts of the SET pin voltage, so any leakage path between the SET pin and the guard ring generates no leakage current.

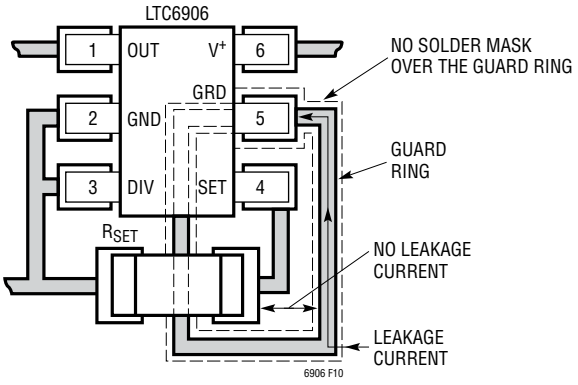


Figure 10. PC Board Layout with Guard Ring

Bypassing the Power Supply

The LTC6906 has on-chip power supply decoupling that eliminates the need for an external decoupling capacitor in most cases. Figure 11 shows a simplified equivalent circuit of the output driver and on-chip decoupling network. When the output driver switches from low to high, the 800pF capacitor delivers the current needed to charge the off-chip capacitive load. Within nanoseconds the system power supply recharges the 800pF capacitor.

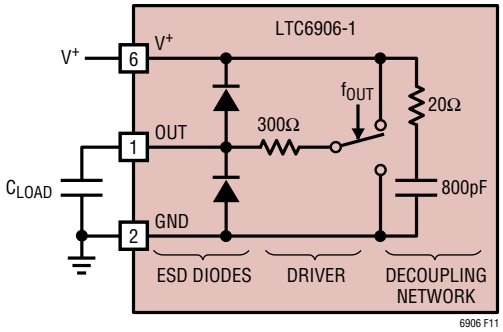


Figure 11. Simplified Equivalent of the Output Driver and On-Chip Decoupling Circuit

Figure 12 shows a test circuit for evaluating performance of the LTC6906 with a highly inductive, 330nH power supply. Figure 13 shows the effectiveness of the on-chip decoupling network. For C_{LOAD} = 5pF to 50pF, the output waveforms remain well formed.

The extremely low supply current of the LTC6906 allows operation with substantial resistance in the power supply. Figure 14 shows a test circuit for evaluating performance of the LTC6906 with a highly resistive, 100Ω power supply. Figure 15 shows the effectiveness of the on-chip decoupling network. For C_{LOAD} = 5pF to 50pF, the output waveforms remain well formed. With a 50pF load, a very small (2.5%) slow tail can be seen on the rising edge. The output waveform is still well formed even in this case. The ability of the LTC6906 to operate with a resistive supply permits supplying power via a CMOS logic gate or microcontroller pin. Since the LTC6906 has a turn-on time of less than 200µs, this technique can be used to enable the device only when needed and further reduce power consumption.

APPLICATIONS INFORMATION

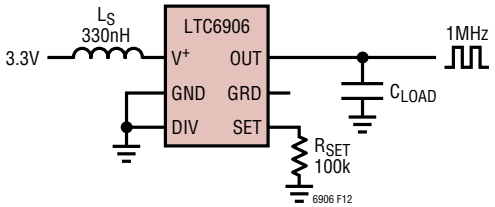


Figure 12. Test Circuit with an Inductive Power Supply

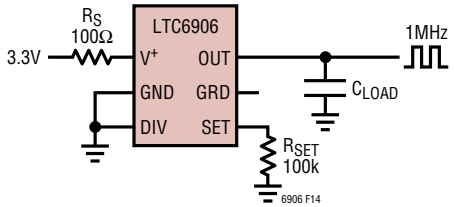


Figure 14. Test Circuit with a Resistive Power Supply

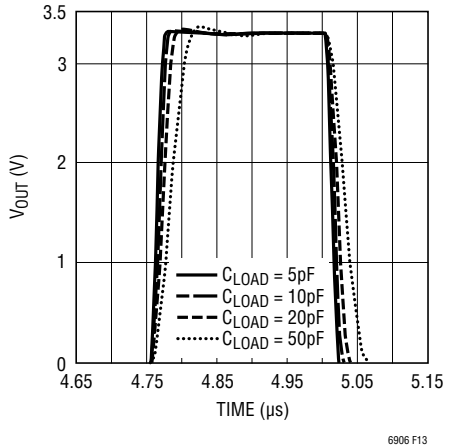


Figure 13. Output Waveforms with an Inductive Supply (See Figure 12)

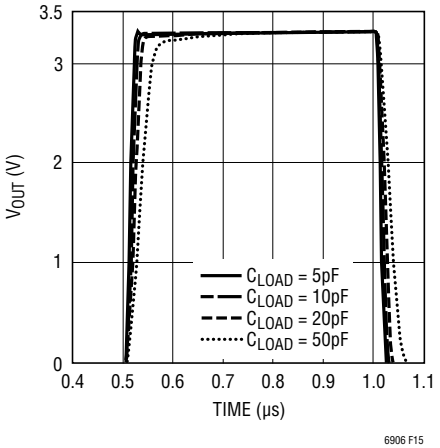


Figure 15. Output Waveforms with a Resistive Supply (See Figure 14)

Start-Up Time

When the LTC6906 is powered up, it holds the OUT pin low. After the master oscillator has settled, the OUT pin is enabled and the first output cycle is guaranteed to be within specification. The time from power-up to the first output transition is given approximately by:

$$t_{START} \cong 64 \bullet t_{OSC} + 100\mu s$$

The digital divider ratio, N, does not affect the start-up time.

Power Supply Rejection

The LTC6906 has a very low supply voltage coefficient, meaning that the output frequency is nearly insensitive to the DC power supply voltage. In most cases, this error term can be neglected.

High frequency noise on the power supply (V^+) pin has the potential to interfere with the LTC6906's master oscillator. Periodic noise, such as that generated by a switching power supply, can shift the output frequency or increase jitter. The risk increases when the fundamental frequency or harmonics of the noise fall near the master oscillator frequency. It is relatively easy to filter the LTC6906 power supply because of the very low supply current. For example, an RC filter with R = 160Ω and C = 10µF provides a 100Hz lowpass filter while dropping the supply voltage only about 10mV.

Operating the LTC6906 with Supplies Higher Than 3.6V

The LTC6906 may also be used with supply voltages between 3.6V and 5.5V under very specific conditions. To ensure proper functioning above 3.6V, a filter circuit must be attached to the power supply and located within 1cm of the device. A simple RC filter consisting of a 100Ω resistor and 1µF capacitor (Figure 16) will ensure that supply resonance at higher supply voltages does not induce unpredictable oscillator behavior. Accuracy under higher supplies may be estimated from the typical Frequency vs Supply Voltage curves in the Typical Performance Characteristics section of this data sheet.

APPLICATIONS INFORMATION

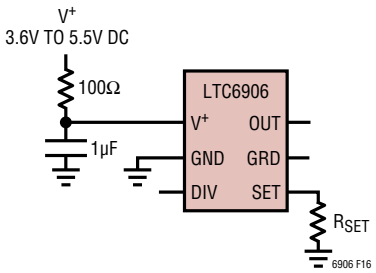


Figure 16. Using the LTC6906 at Higher Supply Voltages

Alternative Methods for Setting the Output Frequency

Any means of sinking current from the SET pin will control the output frequency of the LTC6906. Equation 2 (repeated below) gives the fundamental relationship between frequency and the SET pin voltage and current:

$$t_{OSC} = \frac{1}{f_{OSC}} = \frac{V_{SET}}{I_{SET}} \bullet 10pF \qquad (2)$$

This equation shows that the LTC6906 converts conductance (I_{SET}/V_{SET}) to frequency or, equivalently, converts resistance ($R_{SET} = V_{SET}/I_{SET}$) to period.

V_{SET} is the voltage across an internal diode, and as such it is given approximately by:

$$V_{SET} \cong V_T \bullet Log_e \frac{I_{SET}}{I_S}$$

$$\cong 25.9mV \bullet Log_e \left(\frac{I_{SET}}{82 \bullet 10^{-18} A} \right) - 2.3mV/°C$$

where

$V_T = kT/q = 25.9mV$ at $T = 300°K$ (27°C)

$I_S \cong 82 \bullet 10^{-18}$ Amps

(I_S is also temperature dependent)

V_{SET} varies with temperature and the SET pin current. The response of V_{SET} to temperature is shown in the Typical Performance graphs. V_{SET} changes approximately –2.3mV/°C. At room temperature V_{SET} increases 18mV/octave or 60mV/decade of increase in I_{SET}.

If the SET pin is driven with a current source generating I_{SET}, the oscillator output frequency will be:

$$f_{OSC} \cong \frac{\frac{I_{SET}}{10pF}}{25.9mV \bullet \ell n\left(\frac{I_{SET}}{82 \bullet 10^{-18} A} \right) - 2.3mV/°C}$$

Figure 17 and Figure 18 show a current controlled oscillator and a voltage controlled oscillator. These circuits are not highly accurate if used alone, but can be very useful if they are enclosed in an overall feedback circuit such as a phase-locked loop.

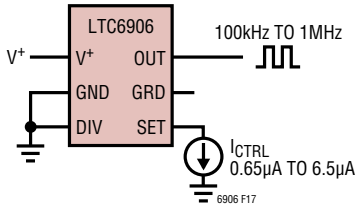


Figure 17. Current Controlled Oscillator

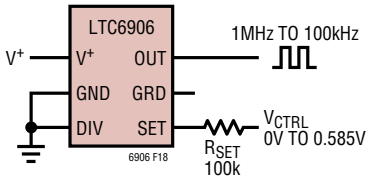


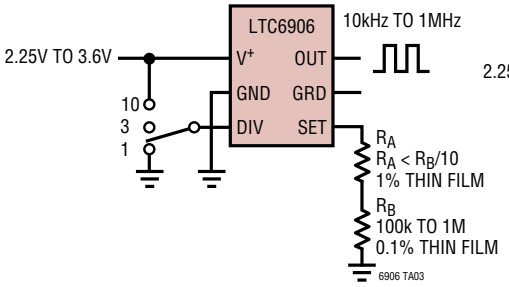
Figure 18. Voltage Controlled Oscillator

Jitter and Divide Ratio

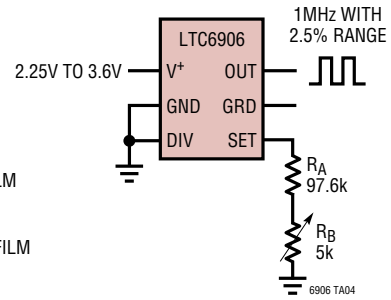
At a given output frequency, a higher master oscillator frequency and a higher divide ratio will result in lower jitter and higher power supply dissipation. Indeterminate jitter percentage will decrease by a factor of slightly less than the square root of the divider ratio, while determinate jitter will not be similarly attenuated. Please consult the specification tables for typical jitter at various divider ratios.

TYPICAL APPLICATIONS

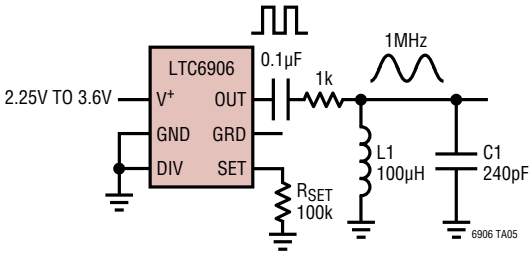
Setting Frequency to 0.1% Resolution with Standard Resistors



Trimming the Frequency

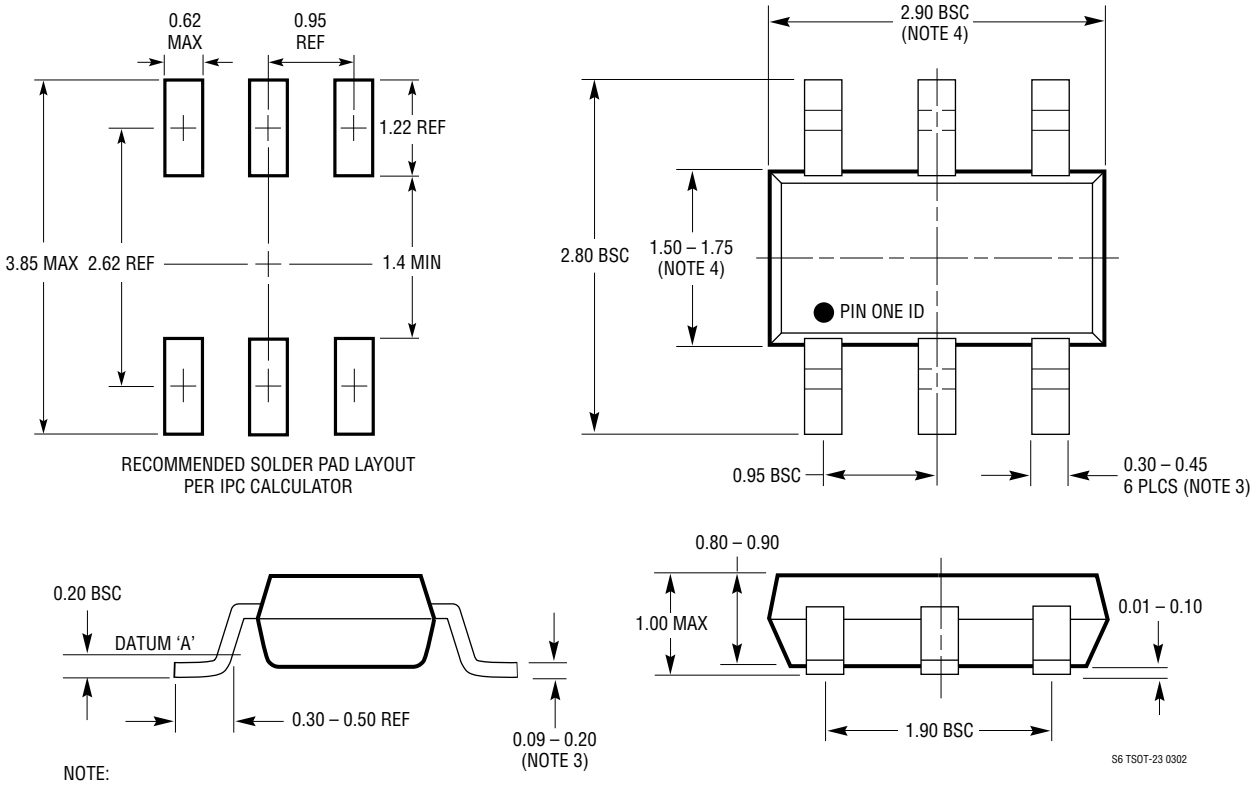


Sine Wave Oscillator



PACKAGE DESCRIPTION

S6 Package
6-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1636)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	12/10	Added Note 9.	2-3
		Revised values in the Guarding Against PC Board Leakage section.	9
C	11/11	Reinsert symbols missing from Rev B.	1, 4, 5, 6, 8, 9, 10, 11, 12
D	02/21	Reinsert missing symbols in plots.	1, 4, 5, 10

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1799	1kHz to 33MHz ThinSOT Oscillator	Single Output, Greater Frequency Range
LTC6900	1kHz to 20MHz ThinSOT Oscillator	Single Output, Greater Frequency Range
LTC6902	Multiphase Oscillator with Spread Spectrum Frequency Modulation	2-, 3- or 4-Phase Outputs
LTC6903/LTC6904	1kHz to 68MHz Serial Port Programmable Oscillator	Very Wide Frequency Range with Digital Programmability
LTC6905	17MHz to 170MHz ThinSOT Oscillator	Single Output, Higher Frequency

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LTC6906HS6#TRPBF LTC6906IS6#TRMPBF LTC6906IS6#TRPBF LTC6906CS6#TRMPBF LTC6906HS6#TRMPBF LTC6906CS6#TRPBF DC2073B-H