ABSOLUTE MAXIMUM RATINGS

Voltage on All Pins Except V_{PROG} Relative to V_{SS}...-0.3V to +6V
Voltage on V_{PROG} Relative to V_{SS}.....-0.3V to +18V
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-55°C to +125°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING PROCEDURE

(2.5V ≤ V_{DD} ≤ 4.5V, T_A = -20°C to +70°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}	(Note 1)	+2.5		+4.5	V
Data I/O Pins	SCL, SDA	(Note 1)	-0.3		+4.5	V
Programming Pin	V_{PROG}	(Note 1)	-0.3		+15.5	V
V_{IN}, AIN0, AIN1 Pin	V_{IN}, AIN0, AIN1	(Note 1)	-0.3		V_{DD} + 0.3	V

DC ELECTRICAL CHARACTERISTICS

(2.5V ≤ V_{DD} ≤ 4.5V, T_A = -20°C to +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Active Current	I_{ACTIVE}			50	75	µA
Sleep-Mode Current	I_{SLEEP}	V_{DD} = 2.0V, SCL, SDA = V_{SS}		0.3	1.0	µA
		SCL, SDA = V_{SS}		1	3	
Current-Measurement Resolution	I_{LSB}			25		µV
Current-Measurement Full-Scale Magnitude	I_{FS}	(Note 1)		±51.2		mV
Current-Measurement Offset Error	I_{OERR}	(Note 2)	-50		+50	µV
Current-Measurement Gain Error	I_{GERR}		-1.5		+1.5	% of reading
Timebase Accuracy	t_{ERR}	V_{DD} = 3.6V at +25°C	-1		+1	%
		T_A = 0°C to +70°C	-2		+2	
		T_A = -20°C to +70°C	-3		+3	
Voltage Error	V_{GERR}	V_{DD} = V_{IN} = 3.6V, T_A = 0°C to +50°C	-10		+10	mV
		T_A = -20°C to +70°C	-20		+20	
Input Resistance V_{IN}, AIN0, AIN1	R_{IN}		15			MΩ
AIN0, AIN1 Error			-8		+8	LSB
V_{OUT} Output Drive		I_O = 1mA		V_{DD} - 0.5		V
V_{OUT} Precharge Time	t_{PRE}		13.2	13.7	14.2	ms
Temperature Error	T_{ERR}		-3		+3	°C

DC ELECTRICAL CHARACTERISTICS (continued)

(2.5V ≤ V_{DD} ≤ 4.5V, T_A = -20°C to +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Logic-High: SCL, SDA	V_{IH}	(Note 1)	1.4			V
Input Logic-Low: SCL, SDA	V_{IL}	(Note 1)			0.6	V
Output Logic-Low: SDA	V_{OL}	I_{OL} = 4mA (Note 1)			0.4	V
Pulldown Current: SCL, SDA	I_{PD}	V_{DD} = 4.2V, V_{PIN} = 0.4V		0.2	1.0	µA
V_{PROG} Pulldown	R_{VPROG}			20		kΩ
Input Capacitance: SCL, SDA	C_{BUS}				50	pF
Bus Low Timeout	t_{SLEEP}	(Note 3)	1.5		2.2	s
EEPROM Programming Voltage	V_{PROG}		14		15	V
EEPROM Programming Current	I_{PROG}				2	mA
EEPROM Programming Time	t_{PROG}		3.1		14	ms
EEPROM Copy Endurance			100			Writes

ELECTRICAL CHARACTERISTICS: 2-WIRE INTERFACE

(2.5V ≤ V_{DD} ≤ 4.5V, T_A = -20°C to +70°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	(Note 4)	0		400	kHz
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$	(Note 5)	0.6			µs
Low Period of SCL Clock	t_{LOW}		1.3			µs
High Period of SCL Clock	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU:STA}$		0.6			µs
Data Hold Time	$t_{HD:DAT}$	(Notes 6, 7)	0		0.9	µs
Data Setup Time	$t_{SU:DAT}$	(Note 6)	100			ns
Rise Time of Both SDA and SCL Signals	t_R		20 + 0.1C_B		300	ns
Fall Time of Both SDA and SCL Signals	t_F		20 + 0.1C_B		300	ns
Setup Time for STOP Condition	$t_{SU:STO}$		0.6			µs
Spike Pulse Widths Suppressed by Input Filter	t_{SP}	(Note 8)	0		50	ns
Capacitive Load for Each Bus Line	C_B	(Note 9)			400	pF
SCL, SDA Input Capacitance	C_{BIN}				60	pF

Note 1: All voltages are referenced to V_{SS}.
Note 2: Offset specified after autocalibration cycle and Current Offset Bias Register = 00h.
Note 3: The DS2786B enters the sleep mode 1.5s to 2.2s after (SCL < V_{IL}) **and** (SDA < V_{IL}).
Note 4: Timing must be fast enough to prevent the DS2786B from entering sleep mode due to bus low for period > t_{SLEEP}.
Note 5: f_{SCL} must meet the minimum clock low time plus the rise/fall times.

ELECTRICAL CHARACTERISTICS: 2-WIRE INTERFACE (continued)

(2.5V ≤ V_{DD} ≤ 4.5V, T_A = -20°C to +70°C.)

Note 6: The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the low period (t_{LOW}) of the SCL signal.

Note 7: This device internally provides a hold time of at least 100ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Note 8: Filters on SDA and SCL suppress noise spikes at the input buffers and delay the sampling instant.

Note 9: C_B—total capacitance of one bus line in pF.

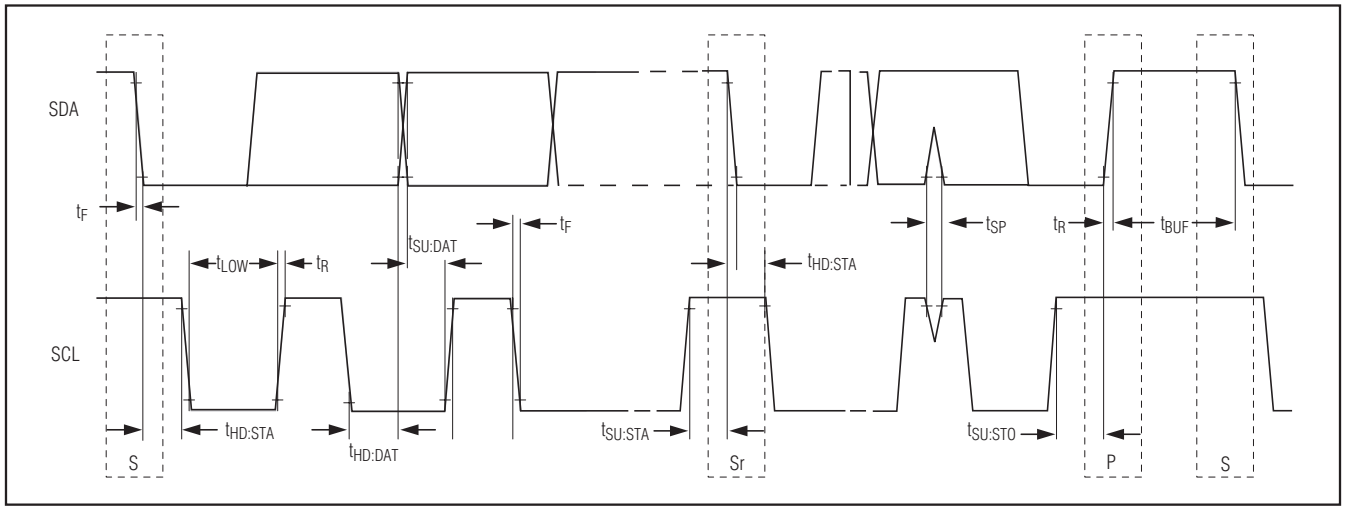
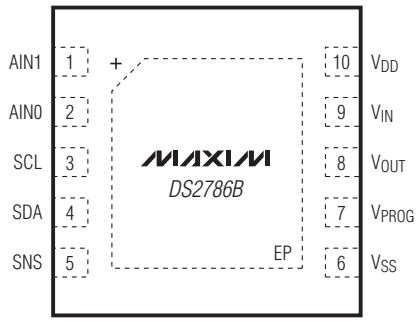


Figure 1. 2-Wire Bus Timing Diagram

Pin Configuration



TDFN
(3mm x 3mm)

Pin Description

PIN	NAME	FUNCTION
1	AIN1	Auxiliary Voltage Input Number 1
2	AIN0	Auxiliary Voltage Input Number 0
3	SCL	Serial Clock Input. Input only 2-wire clock line. Connect this pin to the clock signal of the 2-wire interface. This pin has a 0.2µA typical pulldown to sense disconnection.
4	SDA	Serial Data Input/Output. Open-drain 2-wire data line. Connect this pin to the clock signal of the 2-wire interface. This pin has a 0.2µA typical pulldown to sense disconnection.
5	SNS	Current-Sense Input. Connect to the handset side of the sense resistor.
6	V_{SS}	Device Ground. Connect to the battery side of the sense resistor.
7	V_{PROG}	EEPROM Programming Voltage Input. Connect to external supply for production programming. Connect to V_{SS} during normal operation.
8	V_{OUT}	Voltage Out. Supply for auxiliary input voltage measurement dividers. Connect to high side of resistor-divider circuits.
9	V_{IN}	Battery Voltage Input. The voltage of the cell pack is measured through this pin.
10	V_{DD}	Power-Supply Input. 2.5V to 4.5V Input Range. Connect to system power through a decoupling network.
—	EP	Exposed Pad. Connect to V_{SS}.

Detailed Description

The DS2786B provides current-flow, voltage, and temperature-measurement data to support battery-capacity monitoring in cost-sensitive applications. Current is measured bidirectionally over a dynamic range of ±51.2mV with a resolution of 25µV. Assuming a 15mΩ sense resistor, the current-sense range is ±3.4A, with a 1 least significant bit (LSB) resolution of 1.667mA. Current measurements are performed at regular intervals and each measurement is accumulated internally to coulomb count host power consumption. Each current measurement is reported with sign and magnitude in the 2-byte Current Register. Battery-voltage measurements are reported in the 2-byte Voltage Register with 12-bit (1.22mV) resolution, and auxiliary voltage measurements are reported in the 2-byte Aux Volt Registers with 11-bit resolution. Additionally, the Temperature Register reports temperature with 0.125°C resolution and ±3°C accuracy from the on-chip sensor. The on-chip temperature measurement is optional and replaces auxiliary voltage channel AIN1. Figure 1 is the 2-wire bus timing diagram; Figure 2 is the DS2786B block diagram. Figure 3 is an application example.

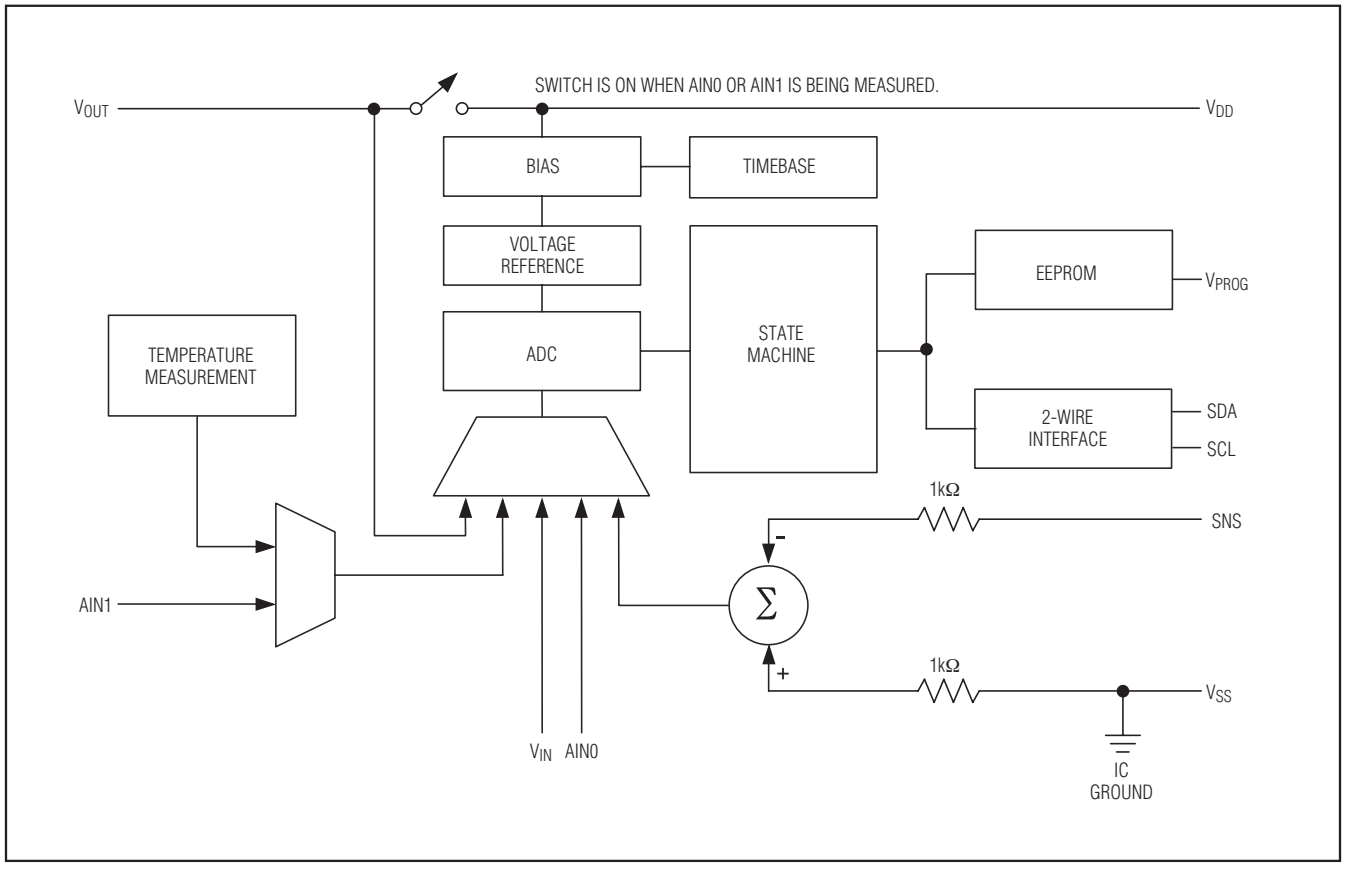


Figure 2. Block Diagram

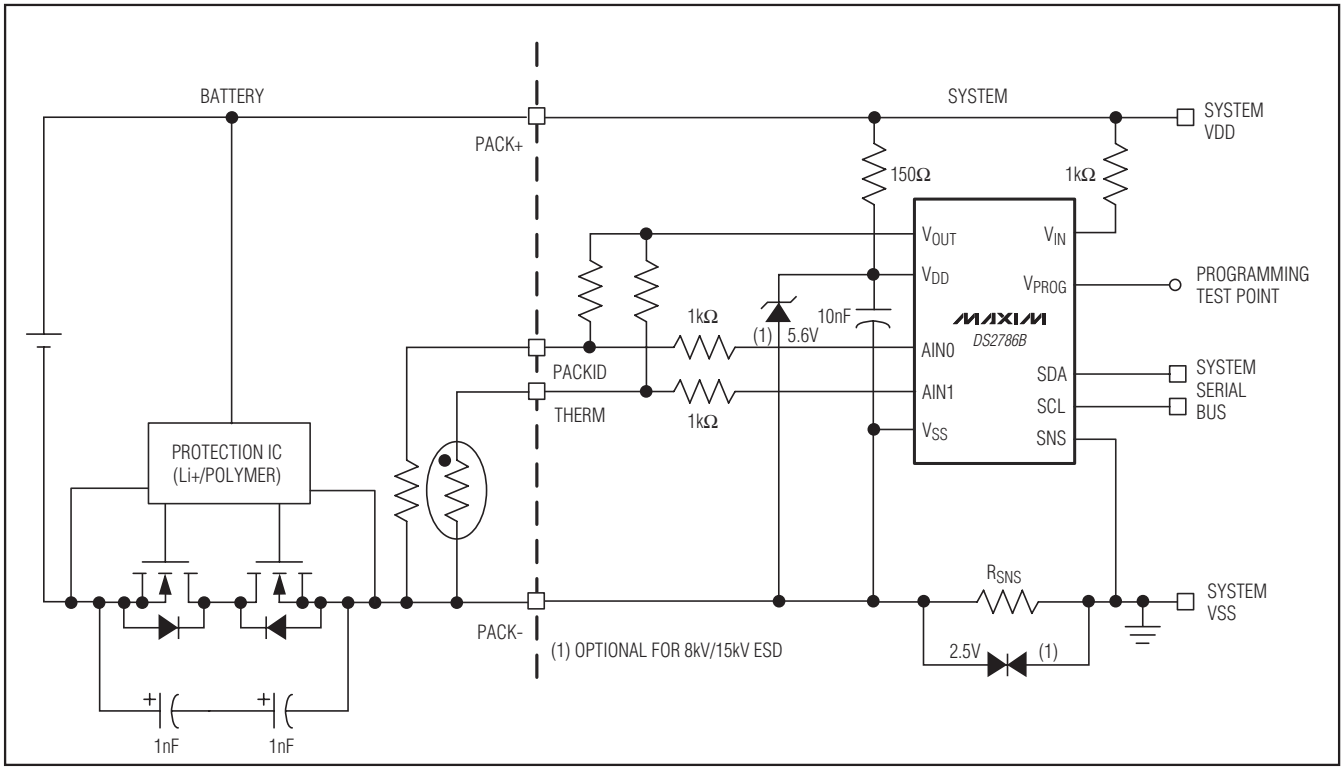


Figure 3. Application Example

The DS2786B provides accurate relative capacity measurements during periods of host system inactivity by looking at cell open-circuit voltage. Cell capacity is calculated using an OCV voltage profile and a 1-byte scale factor to weight-accumulated current. The OCV voltage profile and scale factor are stored in EEPROM memory. The EEPROM memory is constructed with a SRAM shadow so that the OCV voltage profile and scale factor can be overwritten by the host to accommodate a variety of cell types and capacities from multiple-cell vendors. The I^2C interface also allows read/write access to the Status, Configuration, and Measurement Registers.

Power Modes

The DS2786B operates in one of two power modes: Active and Sleep. While in Active Mode, the DS2786B operates as a high-precision battery monitor with temperature, voltage, auxiliary inputs, current, and accumulated current measurements acquired continuously and the resulting values updated in the measurement registers. In Sleep Mode, the DS2786B operates in a low-power mode with no measurement activity. Read-and-write access is allowed to all registers in either mode.

The DS2786B operating mode transitions from sleep to active when:

$$(SCL > V_{IH}) \textbf{ or } (SDA > V_{IH})$$

The DS2786B operating mode transitions from Active to Sleep when:

$$SMOD = 1 \textbf{ and } (SCL < V_{IL}) \textbf{ and } (SDA < V_{IL}) \text{ for } t_{SLEEP}$$

Caution: If SMOD = 1, a pullup resistor is required on SCL and SDA in order to ensure that the DS2786B transitions from Sleep to Active Mode when the battery is charged. If the bus is not pulled up, the DS2786B remains in Sleep and cannot accumulate the charge current. This caution statement applies particularly to a battery that is charged on a standalone charger.

Stand-Alone OCV-Based Fuel Gauge

Parameter Measurement

The DS2786B uses a sigma-delta A/D converter to make measurements. The measurement sequence shown in Figure 4 repeats continuously while the DS2786B is in Active Mode. The V_{OUT} pin is activated t_{PRE} before the AIN0 and AIN1 conversion to allow for the V_{OUT} output voltage to settle. The DS2786B can be configured to measure temperature using its on-chip sensor instead of the AIN1 input. When the internal temperature measurement uses the AIN1 conversion timeslot, V_{OUT} is not activated. A full sequence of voltage measurements nominally takes 1760ms to complete.

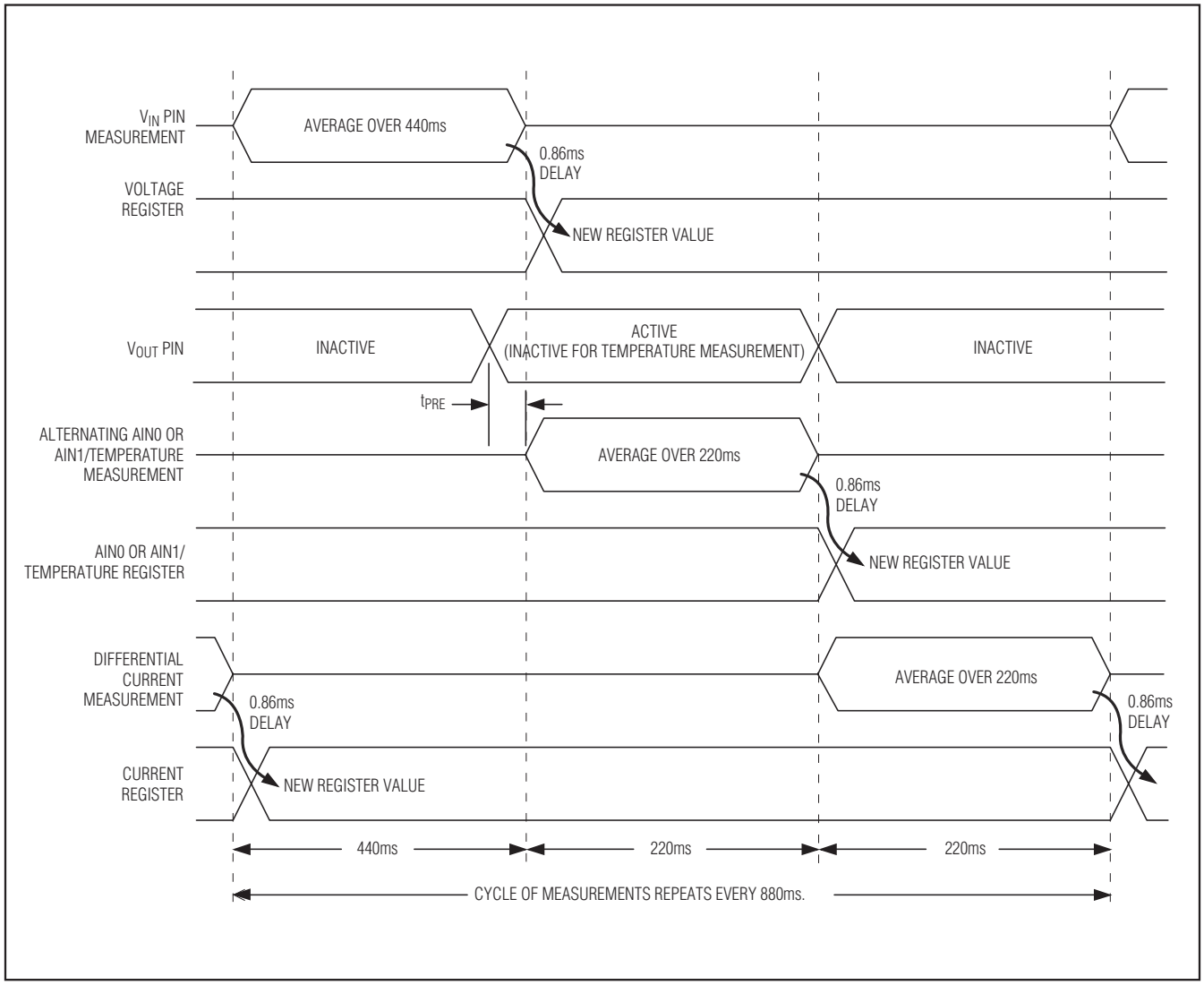


Figure 4. Measurement Sequence

Voltage Measurement

Battery voltage is measured at the V_{IN} input with respect to V_{SS} over a 0 to 4.999V range and with a resolution of 1.22mV. The result is updated every 880ms and placed in the Voltage Register in two's-complement form. Voltages above the maximum register value are reported as 7FFFh. Figure 5 is the Voltage Register format.

The input impedance of V_{IN} is sufficiently large (> 15MΩ) to be connected to a high-impedance voltage-divider in order to support multiple-cell applications. The pack voltage should be divided by the number of series cells to present a single-cell average voltage to the V_{IN} input.

Every 1024th conversion, the ADC measures its input offset to facilitate offset correction to improve voltage accuracy. Offset correction occurs approximately every 15min. The resulting correction factor is applied to the subsequent 1023 measurements. During the offset-correction conversion, the ADC does not measure the V_{IN} signal. The voltage measurement just prior to the offset conversion is displayed in the Voltage Register. The OCV algorithm automatically adjusts for the effects of the offset-correction cycle.

Auxilary Input Measurements

The DS2786B has two auxiliary voltage-measurement inputs, AIN0 and AIN1. Both are measured with respect to V_{SS}. These inputs are designed for measuring resistor ratios, particularly useful for measuring thermistor or pack identification resistors. Prior to the beginning of a measurement cycle on AIN0 or AIN1, the V_{OUT} pin outputs a reference voltage in order to drive a resistive divider formed by a known resistor value, and the unknown resistance to be measured. This technique delivers good accuracy at a reasonable cost, as it removes reference tolerance from the error calculations. Measurements alternate between each input. Each auxiliary measurement is therefore updated every 1760ms and placed in the corresponding AIN0 or AIN1 Register in two's-complement form. Figure 6 shows the Auxiliary Input Registers format.

MSB—ADDRESS 0Ch

S	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5

MSB LSB

"S": SIGN BIT, "X": RESERVED

LSB—ADDRESS 0Dh

2^4	2^3	2^2	2^1	2^0	X	X	X

MSB LSB

UNITS: 1.22mV

Figure 5. Voltage Register Format

AIN0

MSB—ADDRESS 08h

S	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4

MSB LSB

"S": SIGN BIT, "X": RESERVED

LSB—ADDRESS 09h

2^3	2^2	2^1	2^0	X	X	X	X

MSB LSB

UNITS: V_{OUT} × 1/2047

AIN1

MSB—ADDRESS 0Ah

S	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4

MSB LSB

"S": SIGN BIT, "X": RESERVED

LSB—ADDRESS 0Bh

2^3	2^2	2^1	2^0	X	X	X	X

MSB LSB

UNITS: V_{OUT} × 1/2047

Figure 6. Auxiliary Input Registers Format

Temperature Measurement

The DS2786B uses an integrated temperature sensor to measure battery temperature with a resolution of 0.125°C. Temperature measurements are updated every 1760ms and placed in the Temperature Register in two's-complement form. The format of the Temperature Register is shown in Figure 7. The ITEMP bit in the Status/Configuration Register must be set to enable the internal temperature measurement instead of the AIN1 measurement.

Current Measurement

In the Active Mode of operation, the DS2786B continually measures the current flow into and out of the battery by measuring the voltage drop across a low-value current-sense resistor, R_{SNS}, connected between the SNS and V_{SS} pins. The voltage-sense range between SNS and V_{SS} is ±51.2mV. Note that positive current values occur when V_{SNS} is less than V_{SS}, and negative current values occur when V_{SNS} is greater than V_{SS}. Peak signal amplitudes up to 102mV are allowed at the input as long as the continuous or average signal level does not exceed ±51.2mV over the conversion-cycle period. The ADC samples the input differentially and updates the Current Register every 880ms at the completion of each conversion cycle. Figure 8 describes the Current Measurement Register format and resolution for each option. Charge currents above the maximum register value are reported at the maximum value (7FFFh = +51.2mV). Discharge currents below the minimum register value are reported at the minimum value (8000h = -51.2mV).

Every 1024th conversion, the ADC measures its input offset to facilitate offset correction to improve current accuracy. Offset correction occurs approximately every 15min. The resulting correction factor is applied to the subsequent 1023 measurements. During the offset correction conversion, the ADC does not make a measurement. The current measurement just prior to the offset conversion is displayed in the Current Register. See Table 1 for current range and resolution for various R_{SNS} values.

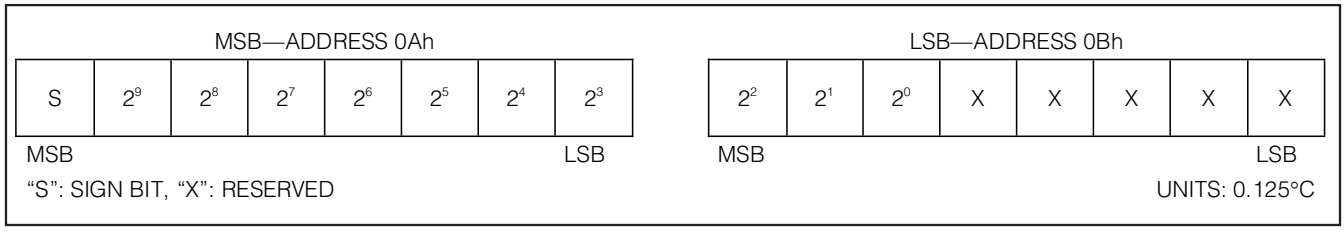


Figure 7. Temperature Register Format

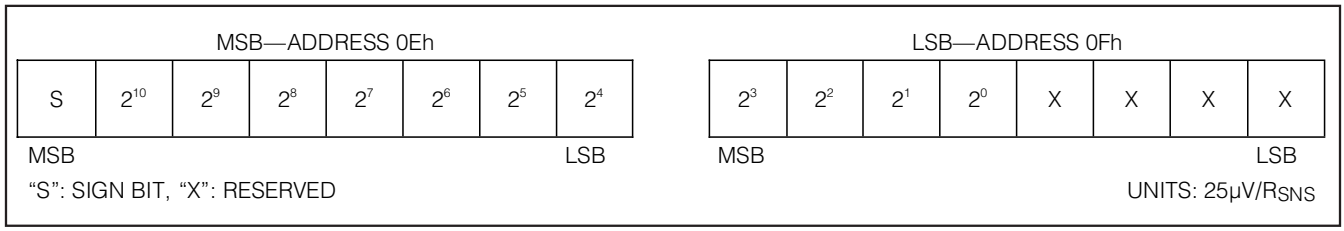


Figure 8. Current Register Formats

Table 1. Current Range and Resolution for Various R_{SNS} Values

CURRENT RESOLUTION (1 LSB)				
$\lvert V_{SS} - V_{SNS} \rvert$	R_{SNS}			
	20mΩ	15mΩ	10mΩ	5mΩ
25µV	1.25mA	1.667mA	2.5mA	5mA

CURRENT INPUT RANGE				
$V_{SS} - V_{SNS}$	R_{SNS}			
	20mΩ	15mΩ	10mΩ	5mΩ
±51.2mV	±2.56A	±3.41A	±5.12A	±10.24A

Current Offset Bias

The Current Offset Bias Register (COBR) allows a programmable offset value to be added to raw current measurements. The result of the raw current measurement plus the COBR value is displayed as the current measurement result in the Current Register, and is used for current accumulation and detection of an OCV condition. The COBR value can be used to correct for a static offset error, or can be used to intentionally skew the current results and therefore the current accumulation.

Read and write access is allowed to COBR. Whenever the COBR is written, the new value is applied to all subsequent current measurements. COBR can be programmed in 25µV steps to any value between +3.175mV and -3.2mV. The COBR value is stored as a two's-complement value in nonvolatile (NV) memory. The COBR factory default value is 00h. Figure 9 shows the Current Offset Bias Register format.

Current Accumulation

An Internal Accumulated Current Register (IACR) serves as an up/down counter holding a running count of charge since the last OCV condition. Current measurement results, plus a programmable bias value are internally summed, or accumulated, at the completion of each current measurement-conversion period. The IACR has a range of ±204.8mVh. The IACR uses the Initial or Learned Cell Capacity Registers to increment or decrement the Relative Capacity Register as current flows into or out of the battery. In this way, the fuel gauge is accurate even when an OCV condition does not occur for an extended time period. See Table 2 for the accumulated current range for various R_{SNS} values.

ADDRESS 60h

S	2^6	2^5	2^4	2^3	2^2	2^1	2^0

MSB LSB

"S": SIGN BIT UNITS: 25µV/R_{SNS}

Figure 9. Current Offset Bias Register Format

Table 2. Accumulated Current Range for Various R_{SNS} Values

IACR RANGE				
V_{SS} - V_{SNS}	R_{SNS}			
	20mΩ	15mΩ	10mΩ	5mΩ
±204.8mVh	±10.24Ah	±13.65Ah	±20.48Ah	±40.96Ah

Cell-Capacity Estimation

The DS2786B uses a hybrid OCV measurement and coulomb-counting algorithm to estimate remaining cell capacity. During periods of charging or discharging the cell, the DS2786B counts charge flow into and out of the cell. When the application becomes inactive, the DS2786B waits for the cell voltage to relax and then adjusts the coulomb count based on an open-circuit voltage cell model stored in device EEPROM. The resulting calculation is reported to the system as a percentage value between 0 and 100%. As the cell ages, a learn feature adjusts for changes in capacity.

The Relative Capacity Register reports remaining cell charge as a percentage of full. Relative capacity is reported with a resolution of 0.5% and is limited to a value between 0% and 100%. The Relative Capacity Register is updated each time the IC performs a current measurement or open-circuit cell-voltage measurement. See Figure 10.

ADDRESS 02h

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

MSB LSB

UNITS: 0.5%

Figure 10. Relative Capacity Register Format

Prior to the first learn operation, the relative capacity value is calculated by adding the IACR multiplied by the initial capacity scaling factor (7Ah) to the last OCV relative capacity (16h). After the first learn operation, the relative capacity value is calculated by adding the IACR multiplied by the learned capacity scaling factor (17h) to the last OCV relative capacity (16h).

Each Capacity Scaling Factor Register has a resolution of 78.125%/Vh and a maximum range of 0 to 19921.875%/Vh. During assembly, the Initial Capacity Register should be programmed to the capacity of the cell. For example, an application using a 1Ah cell and 0.015Ω sense resistor would set the Initial Capacity Register to a value of (100%/(1Ah x 0.015Ω))/ 78.125%/Vh = 55h. The Learned Capacity Scaling Factor Register is controlled by the DS2786B. The power-up value is 00h, and the register is updated with the calculated new cell capacity value after every learn operation. See Figures 11 and 12.

OCV Detection

When the magnitude of the measured current (after COBR is applied) is less than the value defined by the OCV Threshold Register, the DS2786B begins dV/dt measurement evaluation to detect an OCV voltage condition. A threshold value that is below the minimum operational current, but above the maximum idle current of the application should be selected. The OCV Threshold Register has a resolution of 25µV/R_{SNS}, and a range from 0mV/R_{SNS} to 6.375mV/R_{SNS}. The factory default value is 28h. See Figure 13 for the OCV threshold register format.

While the measured current is below the OCV threshold level, the DS2786B actively searches for a relaxed cell by calculating the change in cell voltage as reported in the Voltage Register over 7.5min intervals (dV/dt). If the 7.5min dV/dt change of an average of four Voltage Register readings is less than the value stored in the OCV dV/dt Threshold Register, the DS2786B determines that the cell is now in a relaxed state and the Relative Capacity Register is adjusted based on the OCV cell model stored in parameter EEPROM. This operation occurs repeatedly every 7.5min up to 1hr after the cell enters a relaxed state.

The OCV dV/dt Threshold Register has a resolution of 0.61mV/7.5min and a range from 0mV/7.5min to 9.15mV/7.5min. The factory default value is 2.44mV/7.5min. Note that the upper 4 bits of the OCV dV/dt Threshold Register are used to EEPROM back bits from the Status/Configuration Register. Figure 14 shows the OCV dV/dt threshold register format.

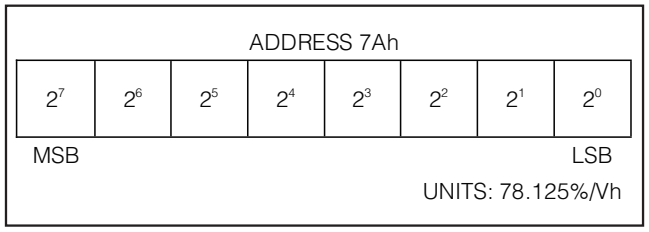


Figure 11. Initial Capacity Scaling Factor Register Format

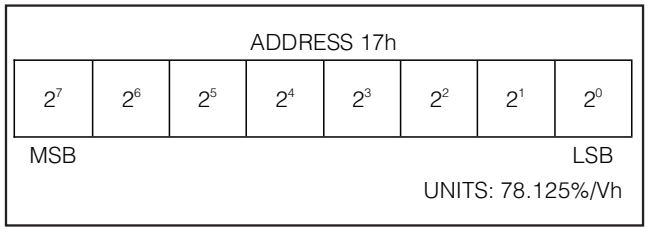


Figure 12. Learned Capacity Scaling Factor Register Format

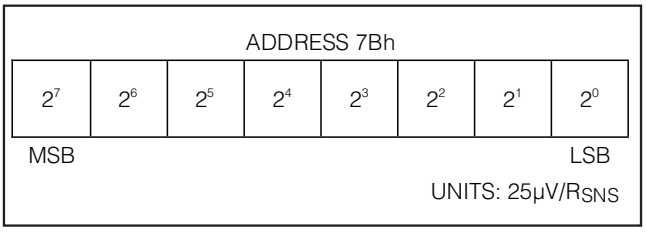


Figure 13. OCV Threshold Register Format

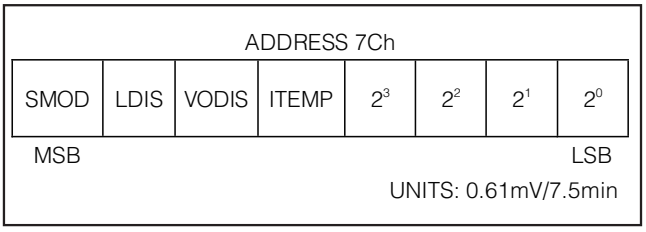


Figure 14. OCV dV/dt Threshold Register Format

OCV Cell Model

The OCV cell model is a 9-point piece-wise linear approximation of open-circuit cell voltage vs. the remaining capacity of the cell. Whenever an OCV update occurs, the Relative Capacity Register is adjusted to a new value based on the OCV voltage reading and a linear approximation of the table values. Figure 15 shows the factory-default cell model stored in EEPROM.

The OCV cell model can be modified by changing the Capacity and Voltage Breakpoint Registers in EEPROM. Capacity 0 is fixed at 0% and cannot be changed. Capacity 1 through Capacity 7 are stored with 0.5% resolution at addresses 61h through 67h, respectively. Capacity values must be monotonic (Capacity 1 > Capacity 0, Capacity 2 > Capacity 1, etc.), but otherwise can be written to any value between 0.5% to 99.5%. Capacity 8 is fixed at a value of 100% and cannot be changed. See Figure 16.

Voltage breakpoints require 2 bytes per breakpoint, but are otherwise stored in a similar manner: voltage breakpoint 0: MSB stored at address 68h, LSB stored at address 69h. Other voltage breakpoints are stored sequentially through address location 79h. Each voltage breakpoint has a resolution of 1.22mV, and a range from 0.0V to 4.996V. Voltage breakpoint values must also be monotonic. Figure 17 is the Voltage Breakpoint Register format.

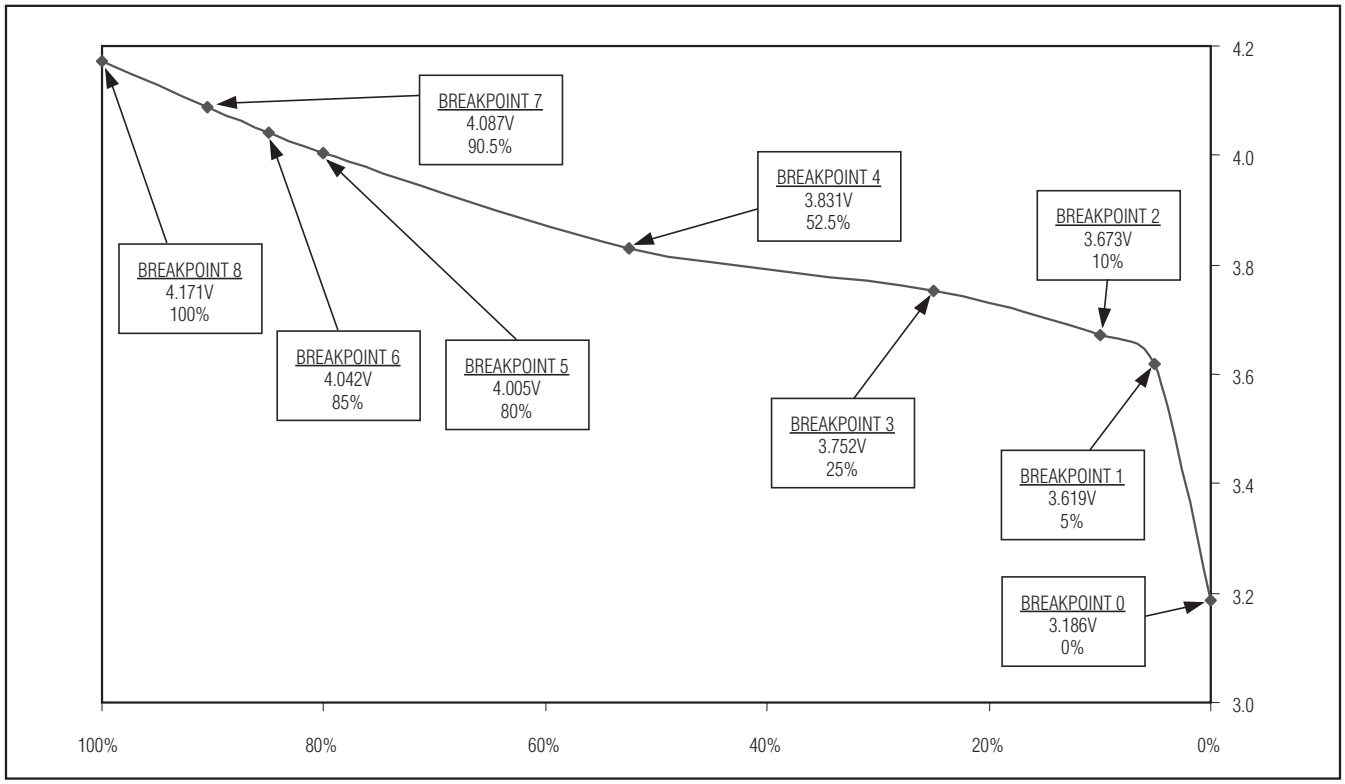


Figure 15. DS2786BG-C3 OCV Cell Model

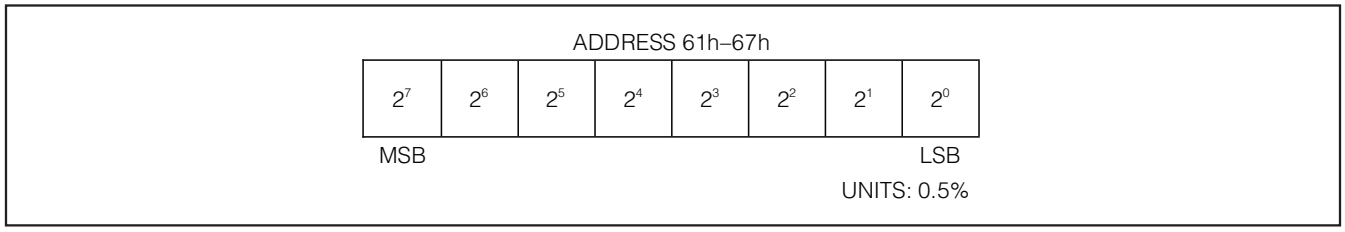


Figure 16. Capacity 1 to Capacity 7 Registers Format

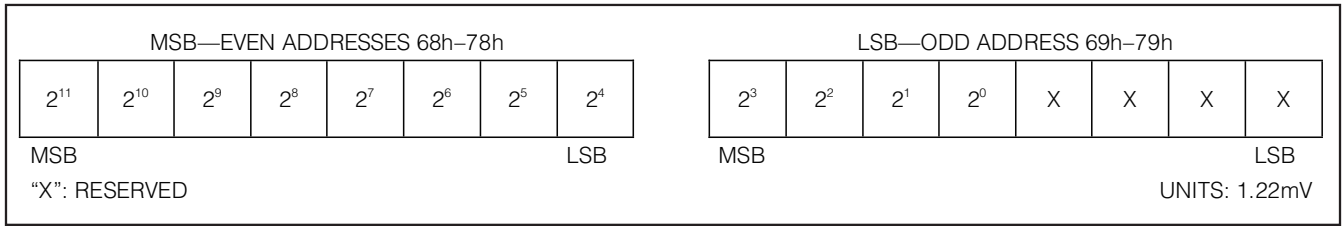


Figure 17. Voltage Breakpoint Register Format

Initial Capacity Estimation

The DS2786B calculates relative capacity immediately upon power-up. During initialization, the DS2786B makes a voltage measurement and uses the OCV cell model data to determine a starting point for the Relative Capacity Register. This estimation occurs regardless of the load on the cell. Any error induced from cell loading is removed at the next OCV adjustment. The initial voltage measurement used in determining the starting point is stored in the Initial Voltage Register until the IC is power cycled. See Figure 18.

New Capacity Learning

As the cell ages, the Initial Capacity Scaling Factor Register value might no longer accurately reflect the true capacity of the cell, causing error in relative capacity calculation while in coulomb-counting mode of operation. The DS2786B has a learn feature that allows the IC to remain accurate as the cell changes. The DS2786B compares the percent relative capacity difference between the last two OCV updates to the change in the coulomb count to learn the new cell capacity. The Last OCV Register maintains the relative capacity percentage at the previous OCV adjustment point used for learning the new cell capacity. The last OCV is updated with a new value at each OCV adjustment. Figure 19 shows the Last OCV Register format.

Example: Assuming a 15mΩ sense resistor, the DS2786B adjusts the relative capacity of a 1000mAh cell to 10% based on an OCV measurement during an idle period of the application. The cell is then charged by 500mAh (to 60% expected) based on the internal coulomb count multiplied by the learned capacity scaling factor value of 55h. The next OCV adjustment determines the relative capacity should actually be at 65%, not 60%. The DS2786B then adjusts the learned capacity scaling factor value upward to (65% - 10%)/(500mAh x 0.015Ω) = 5Eh, lowering the expected cell capacity by approximately 10%.

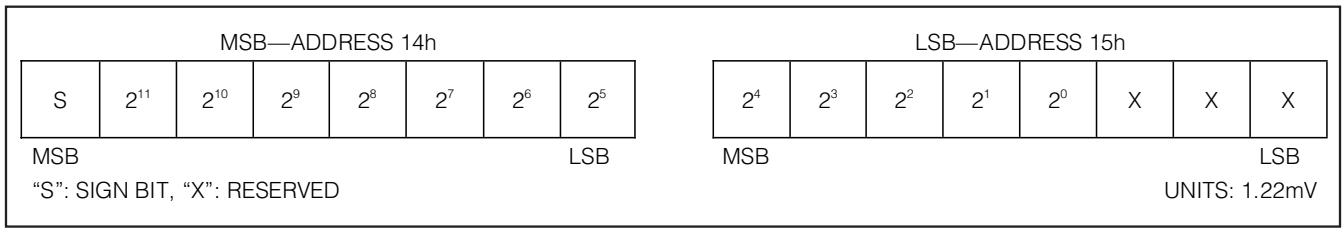


Figure 18. Initial Voltage Register Format

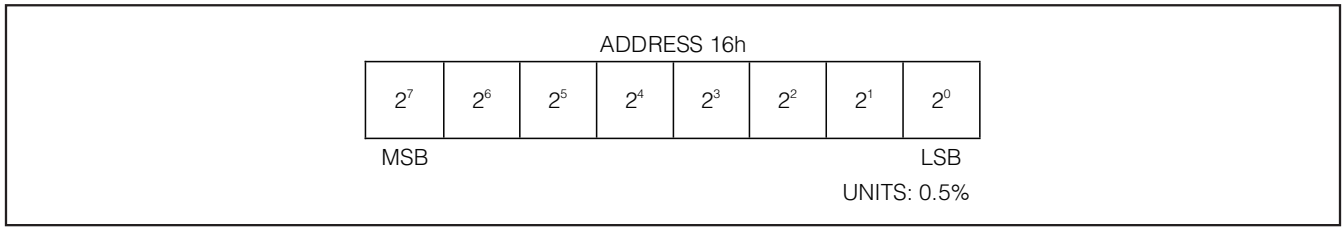


Figure 19. Last OCV Register Format

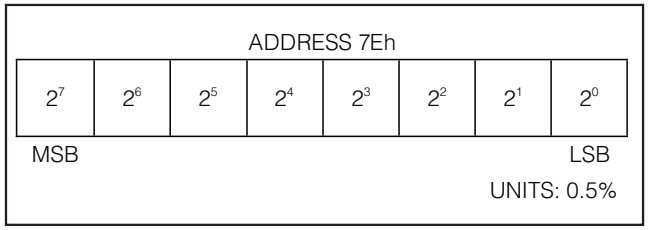


Figure 20. Learn Delta Percent Threshold

The learn delta percent threshold allows the application to select how large a cell capacity change is required before the new cell-capacity value is learned. The difference between the present OCV measurement and the last OCV measurement must be greater than the learn delta percent threshold value for a learn to occur. This prevents IC measurement resolution from adding error to the learned cell-capacity value. It is recommended this register be set to a value of at least 50%. Figure 20 shows the learn delta percent threshold.

Memory Map

The DS2786B has memory space with registers for instrumentation, status, and control. When the MSB of a 2-byte register is read, both the MSB and LSB are latched and held for the duration of the read data command to prevent updates during the read and ensure synchronization between the 2 register bytes. For consistent results, always read the MSB and the LSB of a 2-byte register during the same read data command sequence.

Memory locations 60h through 7Fh are EEPROM storage locations. EEPROM memory is shadowed by RAM to eliminate programming delays between writes and to allow the data to be verified by the host system before being copied to EEPROM. The read data and write data protocols to/from EEPROM memory addresses access the shadow RAM. Setting the RCALL bit in the Command Register (FEh) initiates data transfer from the EEPROM to the shadow RAM. See Figure 21.

Setting the COPY bit in the Command Register initiates data transfer from the shadow RAM to the EEPROM. An external voltage supply must be provided on the V_{PROG} pin prior to writing the COPY bit. The DS2786B requires the COPY bit be reset to zero within the t_{PROG} time window to properly program EEPROM. Resetting COPY too soon might prevent a proper write of the cells. Resetting COPY too late might degrade EEPROM copy endurance.

The DS2786B uses shadow RAM data for fuel-gauge calculations. Fuel-gauge information can be changed in the application by writing the shadow RAM locations. Afterwards, the SOCV bit should be written to reset the fuel gauge. Note that any reset of the IC causes the shadow RAM data to be restored from EEPROM.

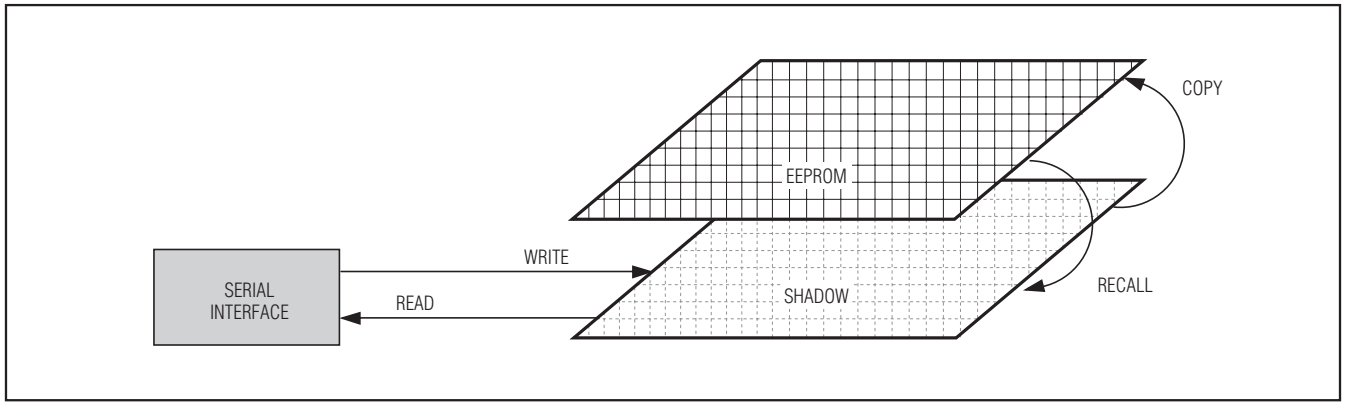


Figure 21. EEPROM Access Through Shadow RAM

Table 3. Memory Map

ADDRESS	DESCRIPTION	READ/WRITE
00h	Reserved	—
01h	Status/Config Register	R/W
02h	Relative Capacity	R
03h to 07h	Reserved	—
08h	Auxiliary Input 0 MSB	R
09h	Auxiliary Input 0 LSB	R
0Ah	Auxiliary Input 1/ Temperature MSB	R
0Bh	Auxiliary Input 1/ Temperature LSB	R
0Ch	Voltage Register MSB	R
0Dh	Voltage Register LSB	R
0Eh	Current Register MSB	R

ADDRESS	DESCRIPTION	READ/WRITE
0Fh	Current Register LSB	R
10h to 13h	Reserved	—
14h	Initial Voltage MSB	R
15h	Initial Voltage LSB	R
16h	Last OCV Relative Capacity	R
17h	Learned Capacity Scaling Factor	R
18h to 5Fh	Reserved	—
60h to 7Fh	Parameter EEPROM	R/W
80h to FDh	Reserved	—
FEh	Command	R/W
FFh	Reserved	—

Table 4. Parameter EEPROM Memory Block

ADDRESSS	DESCRIPTION	FACTORY VALUE
60h	Current Offset Bias Register	00h
61h	Capacity 1	0Ah
62h	Capacity 2	14h
63h	Capacity 3	32h
64h	Capacity 4	69h
65h	Capacity 5	A0h
66h	Capacity 6	AAh
67h	Capacity 7	B5h
68h	Voltage Breakpoint 0 MSB	A3h
69h	Voltage Breakpoint 0 LSB	20h
6Ah	Voltage Breakpoint 1 MSB	B9h
6Bh	Voltage Breakpoint 1 LSB	50h
6Ch	Voltage Breakpoint 2 MSB	BCh
6Dh	Voltage Breakpoint 2 LSB	10h
6Eh	Voltage Breakpoint 3 MSB	C0h
6Fh	Voltage Breakpoint 3 LSB	20h

ADDRESS	DESCRIPTION	FACTORY VALUE
70h	Voltage Breakpoint 4 MSB	C4h
71h	Voltage Breakpoint 4 LSB	20h
72h	Voltage Breakpoint 5 MSB	CDh
73h	Voltage Breakpoint 5 LSB	10h
74h	Voltage Breakpoint 6 MSB	CEh
75h	Voltage Breakpoint 6 LSB	F0h
76h	Voltage Breakpoint 7 MSB	D1h
77h	Voltage Breakpoint 7 LSB	40h
78h	Voltage Breakpoint 8 MSB	D5h
79h	Voltage Breakpoint 8 LSB	90h
7Ah	Initial Capacity Scaling	80h
7Bh	OCV Current Threshold	06h
7Ch	OCV dV/dt Threshold	94h
7Dh	I^2C Address Configuration*	60h*
7Eh	Learn Threshold	78h
7Fh	User EEPROM	00h

**The factory default 7-bit slave address is 0110110. The upper 3 bits are fixed at 011; the lower 4 bits can be changed by writing the I^2C Address Configuration Register as illustrated in Figures 24 and 25.*

Status/Config Register

The Status/Config Register is read/write with individual bits designated as read only. Bit values indicate status as well as program or select device functionality. Bits 3 though 6 are EEPROM backed at memory location 7Ch. Note that their bit positions differ between these locations. See Figure 22:

- **PORF**—The power-on-reset flag is set to indicate initial power-up. PORF is not cleared internally. The user must write this flag value to a zero in order to use it to indicate subsequent power-up events. POR event causes a reset of the fuel gauge. PORF is read/write-to-zero.
- **SMOD**—Sleep Mode enable. A value of 1 allows the IC to enter Sleep Mode when SCL **and** SDA are low for t_{SLEEP}. A value of zero disables the transition to Sleep Mode. This bit is EEPROM backed by bit 7 of memory location 7Ch. The factory-programmed value is 1.

  Caution: SMOD sleep feature must be disabled when a battery is charged on an external charger that does not connect to the SDA or SCL pins. SMOD sleep can be used if the charger pulls SDA or SCL high. The IC remains in sleep on a charger that fails to properly drive SDA or SCL and therefore does not adjust relative capacity when a battery is charged.
- **LDIS**—Learn disable. A value of 1 disables cell-capacity learning by the IC. A value of zero allows cell-capacity learning to occur normally. This bit is EEPROM backed by bit 6 of memory location 7Ch. The factory-programmed value is zero.
- **VODIS**—V_{OUT} disable. A value of 1 disables the V_{OUT} output. When set to zero, this output is driven t_{PRE} before the AIN0 conversion begins, and disabled after the AIN1 conversion ends. This bit is EEPROM backed by bit 5 of memory location 7Ch. The factory-programmed value is zero.
- **ITEMP**—ITEMP. A value of 1 enables measurement of temperature using the internal sensor during the AIN1 conversion timeslot. The AIN1 input is not selected and V_{OUT} is not enabled during the AIN1 timeslot. A value of zero restores the measurement of AIN1 and enables V_{OUT} during the AIN1 timeslot. This bit is EEPROM backed by bit 4 of memory location 7Ch. The factory-programmed value is 1.
- **AIN1**—AIN1 conversion valid. This read-only bit indicates that the V_{OUT} output was enabled and a conversion has occurred on the AIN1 pin. When using the VODIS bit, before reading the AIN1 Registers, read the AIN1 bit. Only once the AIN1 bit is set should the AIN1 Register be read.
- **AIN0**—AIN0 conversion valid. This read-only bit indicates that the V_{OUT} output was enabled and a conversion has occurred on the AIN0 pin. When using the VODIS bit, before reading the AIN0 Registers, read the AIN0 bit. Only once the AIN0 bit is set should the AIN0 Register be read.

Command Register

The Command Register is read/write accessible. Bit values indicate operations requested to be performed by the device. See Figure 23 for the Command Register format.

ADDRESS 01h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
X	PORF	SMOD	LDIS	VODIS	ITEMP	AIN1	AIN0

X—Reserved.

Figure 22. Status/Config Register Format

ADDRESS FEh

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
POR	1	X	X	POCV	SOCV	RCALL	COPY

1—Bit always reads logic 1.

X—Reserved.

Figure 23. Command Register Format

- **COPY**—The Copy bit is set to start a copy command of the scratchpad to EEPROM. A programming voltage must be present on the V_{PROG} pin prior for the copy to be successful. The Copy bit must be cleared by software within the t_{PROG} time window.
- **RCALL**—The Recall bit is set to recall the contents of EEPROM into the scratchpad.
- **SOCV**—Stored OCV calculation. This command can be used to reset the relative capacity calculation after updating OCV cell model data in the scratchpad. When set to 1, the part is performing an OCV calculation based on the voltage stored in the Initial Voltage Register and the OCV lookup table values present in the scratchpad. Writing the bit to 1 forces a calculation. Forcing an OCV calculation creates capacity-estimation error. The bit is cleared when the hardware completes the calculation.
- **POCV**—Present OCV calculation. When set to 1, the part is performing an OCV calculation based on the voltage stored in the Voltage Register and the OCV lookup table values present in the scratchpad. Writing the bit to 1 forces a calculation. This function should be used for test purposes only. Forcing an OCV calculation creates capacity-estimation error. The bit is cleared when the hardware completes the calculation.
- **POR**—Power-on reset. A value of 1 starts a power-on reset event. The bit is cleared on the next start or stop on the 2-wire bus, exiting the reset state.

User EEPROM

Location 7Fh provides 1 byte available for storage of user-defined information. This byte does not affect operation of the fuel gauge. Factory default is 00h.

2-Wire Bus System

The 2-wire bus system supports operation as a slave-only device in a single or multislave, and single or multimaster system. The 2-wire interface consists of a serial data line (SDA) and serial clock line (SCL). SDA and SCL provide bidirectional communication between the DS2786B slave device and a master device at speeds up to 400kHz. The DS2786B's SDA pin operates bidirectionally; that is, when the DS2786B receives data, SDA operates as an input, and when the DS2786B returns data, SDA operates as an open-drain output, with the host system providing a resistive pullup. The DS2786B always operates as a slave device, receiving and transmitting data under the control of a master device. The master initiates all transactions on the bus and generates the SCL signal, as well as the START and STOP bits, which begin and end each transaction.

Bit Transfer

One data bit is transferred during each SCL clock cycle, with the cycle defined by SCL transitioning low to high and then high to low. The SDA logic level must remain stable during the high period of the SCL clock pulse. Any change in SDA when SCL is high is interpreted as a START or STOP control signal.

Bus Idle

The bus is defined to be idle, or not busy, when no master device has control. Both SDA and SCL remain high when the bus is idle. The STOP condition is the proper method to return the bus to the idle state.

START and STOP Conditions

The master initiates transactions with a START condition (S) by forcing a high-to-low transition on SDA while SCL is high. The master terminates a transaction with a STOP condition (P), a low-to-high transition on SDA while SCL is high. A Repeated START condition (Sr) can be used in place of a STOP then START sequence to terminate one transaction and begin another without returning the bus to the idle state. In multimaster systems, a Repeated START allows the master to retain control of the bus. The START and STOP conditions are the only bus activities in which the SDA transitions when SCL is high.

Acknowledge Bits

Each byte of a data transfer is acknowledged with an Acknowledge bit (A) or a No Acknowledge bit (N). Both the master and the DS2786B slave generate Acknowledge bits. To generate an acknowledge, the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low until SCL returns low. To generate a no acknowledge (also called NAK), the receiver releases SDA before the rising edge of the acknowledge-related clock pulse and leaves SDA high until SCL returns low. Monitoring the Acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer can occur if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication.

Data Order

A byte of data consists of 8 bits ordered MSB first. The LSB of each byte is followed by the Acknowledge bit. The DS2786B registers composed of multibyte values are ordered MSB first. The MSB of multibyte registers is stored on even data memory addresses.

Slave Address

A bus master initiates communication with a slave device by issuing a START condition followed by a slave address (SAddr) and the read/write (R/W) bit. When the bus is idle, the DS2786B continuously monitors for a START condition followed by its slave address. When the IC receives an address that matches its slave address, it responds with an Acknowledge bit during the clock period following the R/W bit. The DS2786BG-C3 7-bit slave address is 0110110. The upper 3 bits are fixed at 011; the lower 4 bits can be changed by writing the I²C Address Configuration Register at location 7Dh.

Read/Write Bit

The R/W bit following the slave address determines the data direction of subsequent bytes in the transfer. R/W = 0 selects a write transaction, with the following bytes being written by the master to the slave. R/W = 1 selects a read transaction, with the following bytes being read from the slave by the master. With the ADDR3–ADDR0 bits at their default of 0110, writes occur using address 0x6Ch, while reads occur at 0x6Dh.

Bus Timing

The DS2786B is compatible with any bus timing up to 400kHz. No special configuration is required to operate at any speed.

2-Wire Command Protocols

The command protocols involve several transaction formats. The simplest format consists of the master writing the START bit, slave address, and R/W bit, and then monitoring the Acknowledge bit for presence of the DS2786B. More complex formats such as the write data, read data, and function command protocols write data, read data, and execute device-specific operations. All bytes in each command format require the slave or host to return an Acknowledge bit before continuing with the next byte. Each function command definition outlines the required transaction format. Table 5 applies to the transaction formats.

ADDRESS 7Dh

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ADDR3	ADDR2	ADDR1	ADDR0	X	X	X	X

X—RESERVED.

ADDR3:0—USER-ADJUSTABLE BITS OF THE DS2786BG-C3'S I²C ADDRESS. FACTORY DEFAULT IS 0110.

Figure 24. I²C Address Configuration Register Format

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	1	1	ADDR3	ADDR2	ADDR1	ADDR0	R/W

Figure 25. DS2786B I²C Address Byte Format

Table 5. 2-Wire Protocol Key

KEY	DESCRIPTION
S	START bit
SAddr	Slave address (7 bit)
FCmd	Function command byte
MAddr	Memory address byte
Data	Data byte written by master
A	Acknowledge bit—master
N	No acknowledge—master

KEY	DESCRIPTION
Sr	Repeated START
W	R/W bit = 0
R	R/W bit = 1
P	STOP bit
Data	Data byte returned by slave
A	Acknowledge bit—slave
N	No acknowledge—slave

Basic Transaction Formats

Write: S SAddr W A MAddr A Data0 A P

A write transaction transfers 1 or more data bytes to the DS2786B. The data transfer begins at the memory address supplied in the MAddr byte. Control of the SDA signal is retained by the master throughout the transaction, except for the acknowledge cycles.

Read: SAddr W A MAddr A Sr SAddr R A Data0 N P

Write Portion | Read Portion

A read transaction transfers 1 or more bytes from the DS2786B. Read transactions are composed of two parts—a write portion followed by a read portion—and are therefore inherently longer than a write transaction. The write portion communicates the starting point for the read operation. The read portion follows immediately, beginning with a Repeated START, Slave Address with R/W set to 1. Control of SDA is assumed by the DS2786B beginning with the Slave Address Acknowledge cycle. Control of the SDA signal is retained by the DS2786B throughout the transaction, except for the acknowledge cycles. The master indicates the end of a read transaction by responding to the last byte it requires with a no acknowledge. This signals the DS2786B that control of SDA is to remain with the master following the acknowledge clock.

Write Data Protocol

The write data protocol is used to write to register and shadow RAM data to the DS2786B starting at memory address MAddr. Data0 represents the data written to MAddr, Data1 represents the data written to MAddr + 1, and DataN represents the last data byte, written to MAddr + N. The master indicates the end of a write transaction by sending a STOP or Repeated START after receiving the last acknowledge bit:

S SAddr W A MAddr A Data0 A Data1 A … DataN A P

The MSB of the data to be stored at address MAddr can be written immediately after the MAddr byte is acknowledged. Because the address is automatically incremented after the LSB of each byte is received by the DS2786B, the MSB of the data at address MAddr + 1 can be written immediately after the acknowledgment of the data at address MAddr. If the bus master continues an autoincremented write transaction beyond address 4Fh, the DS2786B ignores the data. Data is also ignored on writes to read-only addresses and reserved addresses, as well as a write that autoincrements to the Function Command Register (address FEh). Incomplete bytes and bytes that are not acknowledged by the DS2786B are not written to memory. As noted in the *Memory Map* section, writes to EEPROM locations modify the shadow RAM only.

Read Data Protocol

The read data protocol is used to read register and shadow RAM data from the DS2786B starting at memory address specified by MAddr. Data0 represents the data byte in memory location MAddr, Data1 represents the data from MAddr + 1, and DataN represents the last byte read by the master:

S SAddr W A MAddr A Sr SAddr R A Data0 A Data1 ...DataN N P

Data is returned beginning with the MSB of the data in MAddr. Because the address is automatically incremented after the LSB of each byte is returned, the MSB of the data at address MAddr + 1 is available to the host immediately after the acknowledgment of the data at address MAddr. If the bus master continues to read beyond address FFh, the DS2786B outputs data values of FFh. Addresses labeled Reserved in the memory map (Table 3) return undefined data. The bus master terminates the read transaction at any byte boundary by issuing a no acknowledge followed by a STOP or Repeated START.

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
10 TDFN	T1033+1	**21-0137**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/08	Initial release	—
1	4/10	Changed the maximum operating voltage on V_{DD} to 4.5V in the *Features*, *Electrical Characteristics*, and *Pin Description* sections	1–5

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Maxim Integrated:

DS2786BG+ DS2786BG+T&R DS2786BK