

Low-Cost 4x4, 8x4, 8x8 Video Crosspoint Switches

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V+ to V-)+12V
 Positive Supply Voltage (V+) Referred to AGND-0.3V to +12V
 Negative Supply Voltage (V-) Referred to AGND-12V to +0.3V
 DGND to AGND±0.3V
 Buffer Short Circuit to Ground when
 Not Exceeding Package Power DissipationIndefinite
 Analog Input Voltage(V+ + 0.3V) to (V- - 0.3V)
 Digital Input Voltage(V+ + 0.3V) to (V- - 0.3V)
 Input Current, Power On or Off
 Digital Inputs.....±20mA
 Analog Inputs±50mA

Continuous Power Dissipation (T_A = +70°C)
 36-Pin SSOP (derate 11.8mW/°C above +70°C).....941mW
 24-Pin SO (derate 11.8mW/°C above +70°C).....941mW
 40-Pin Plastic DIP (derate 11.3mW/°C above +70°C)....889mW
 44-Pin PLCC (derate 13.3mW/°C above +70°C)1066mW
 Operating Temperature Ranges
 MAX4456C _ _0°C to +70°C
 MAX4_ _ _E_ _-40°C to +85°C
 Junction Temperature+150°C
 Storage Temperature Range-65°C to +150°C
 Lead Temperature (soldering, 10s)+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V+ = +5V, V- = -5V, V_{LOAD} = +5V (internal load resistors on), V_{IN} = V_{AGND} = V_{DGND} = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|--|--|---|------|------|------|-------|
| Operating Supply Voltage | Inferred from PSRR test | | ±4.5 | | ±5.5 | V |
| Input Voltage Range | Inferred from swing test | | -1.3 | | 1.3 | V |
| Voltage Gain | Internal load resistors on, no external load, V _{IN} = 0 to 1V | T _A = +25°C | 0.99 | 1.0 | 1.01 | V/V |
| | | T _A = T _{MIN} to T _{MAX} | 0.98 | 1.0 | 1.02 | |
| Buffer Offset Voltage | T _A = +25°C | | | ±1 | ±15 | mV |
| | T _A = T _{MIN} to T _{MAX} | | | | ±20 | |
| Offset Voltage Drift | | | | 20 | | µV/°C |
| Supply Current, All Buffers On (no external load) | MAX4359/MAX4360 | T _A = +25°C | | 20 | 32 | mA |
| | | T _A = T _{MIN} to T _{MAX} | | | 37 | |
| | MAX4456 | T _A = +25°C | | 39 | 50 | |
| | | T _A = T _{MIN} to T _{MAX} | | | 65 | |
| Supply Current, All Buffers Off | | | | 1.6 | 5 | mA |
| Power-Supply Rejection Ratio | ±4.5V to ±5.5V | | 50 | 64 | | dB |
| Analog Input Current | | | | ±0.1 | ±100 | nA |
| Output Leakage Current | Internal load resistors off, all buffers off | | | | ±100 | nA |
| Internal Amplifier Load Resistor | V _{LOAD} = 5V | T _A = +25°C | 250 | 400 | 600 | Ω |
| | | T _A = T _{MIN} to T _{MAX} | 200 | | 765 | |
| Buffer Output Voltage Swing | Internal load resistors on, no external load | | ±1.3 | | | V |
| Digital Input Current | | | | | ±1 | µA |
| Output Impedance at DC | | | 10 | | | Ω |
| Input-Logic Low Threshold | | | 0.8 | | | V |
| Input-Logic High Threshold | | | 2.4 | | | V |
| SER OUT Output-Logic Low/High | Serial mode, V _{SER} /P _{AR} = 5V | I _{OL} = 0.4mA | 0.4 | | | V |
| | | I _{OH} = -0.4mA | 4 | | | |

Low-Cost 4x4, 8x4, 8x8 Video Crosspoint Switches

MAX4359/MAX4360/MAX4456

AC ELECTRICAL CHARACTERISTICS

(V+ = +5V, V- = -5V, V_{LOAD} = +5V (internal load resistors on), V_{AGND} = V_{DGND} = 0V, T_A = +25°C, unless otherwise noted.)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------|--|-----|-----|-----|-------------------|
| DYNAMIC SPECIFICATIONS | | | | | |
| Output-Buffer Slew Rate | Internal load resistors on, 10pF load | | 250 | | V/μs |
| Single-Channel Crosstalk | 5MHz, V _{IN} = 2V _{P-P} (Note 1) | | 70 | | dB |
| All-Hostile Crosstalk | 5MHz, V _{IN} = 2V _{P-P} (Notes 1, 2) | | 57 | | dB |
| All-Channel Off-Isolation | 5MHz, V _{IN} = 2V _{P-P} (Note 1) | | 80 | | dB |
| -3dB Bandwidth | 10pF load, V _{IN} = 2V _{P-P} (Note 1) | | 35 | | MHz |
| Small-Signal -3dB Bandwidth | 10pF load, V _{IN} = 100mV _{P-P} (Note 1) | | 65 | | MHz |
| 0.1dB Bandwidth | 10pF load, V _{IN} = 100mV _{P-P} (Note 1) | | 4 | | MHz |
| Differential Phase Error | (Note 3) | | 1.0 | | degrees |
| Differential Gain Error | (Note 3) | | 0.5 | | % |
| Input Noise | DC to 40MHz | | 0.3 | | mV _{RMS} |
| Input Capacitance | All buffer inputs grounded | | 6 | | pF |
| Buffer Input Capacitance | Additional capacitance for each output buffer connected to channel input | | 2 | | pF |
| Output Capacitance | Output buffer off | | 7 | | pF |

SWITCHING CHARACTERISTICS

(Figure 4, V+ = +5V, V- = -5V, V_{LOAD} = +5V (internal load resistors on), V_{IN-} = V_{AGND} = V_{DGND} = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 4)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------|------------------------------------|---------------|-----|-----|-----|-------|
| Chip-Enable to Write Setup | t _{CE} | | 0 | | | ns |
| Write Pulse Width High | t _{WH} | | 80 | | | ns |
| Write Pulse Width Low | t _{WL} | | 80 | | | ns |
| Data Setup | t _{DS} | Parallel mode | 240 | | | ns |
| | | Serial mode | 160 | | | |
| Data Hold | t _{DH} | | 0 | | | ns |
| Latch Pulse Width | t _L | | 80 | | | ns |
| Latch Delay | t _D | | 80 | | | ns |
| Switch Break-Before-Make Delay | t _{ON} - t _{OFF} | | | 15 | | ns |
| LATCH Edge to Switch Off | t _{OFF} | LATCH on | | 35 | | ns |
| LATCH Edge to Switch On | t _{ON} | | | 50 | | ns |

Note 1: See *Dynamic Test Circuits* section.

Note 2: 3dB typical crosstalk improvement when R_S = 0.

Note 3: Input test signal: 3.58MHz sine wave of amplitude 40IRE superimposed on a linear ramp (0 to 100IRE). IRE is a unit of video-signal amplitude developed by the International Radio Engineers. 140IRE = 1.0V.

Note 4: Guaranteed by design.

Low-Cost 4x4, 8x4, 8x8 Video Crosspoint Switches

MAX4359/MAX4360/MAX4456

Pin Description

| PIN | | | | | NAME | FUNCTION |
|-------------|---------------------|-----------------------------------|-----------------------------------|------------------------------------|------------------------------|--|
| MAX4359 | | MAX4360 | MAX4456 | | | |
| SO | SSOP | SSOP | DIP | PLCC | | |
| 1 | 1 | 1 | 1 | 2 | D1/ SER OUT | Parallel Data Bit D1 when SER/ $\overline{\text{PAR}}$ = GND. Serial output for cascading multiple parts when SER/ $\overline{\text{PAR}}$ = V_{CC} . |
| 2 | 2 | 2 | 2 | 3 | D0/SER IN | Parallel Data Bit D0 when SER/ $\overline{\text{PAR}}$ = GND. Serial input when SER/ $\overline{\text{PAR}}$ = V_{CC} . |
| 3, 5 | 3, 5 | 3, 5 | 3, 4, 6 | 4, 5, 7 | A ₋ | Output Buffer Address Lines |
| 4, 6, 8, 10 | 4, 6, 8, 10 | 4, 6, 8, 10, 12, 14, 16, 18 | 5, 7, 9, 11, 13, 15, 17, 19 | 6, 8, 10, 13, 15, 17, 19, 21 | IN ₋ | Video Input Lines |
| 7 | 7 | 7 | 8 | 9 | LOAD | Asynchronous Control Line. When LOAD = V_{CC} , all the 400 Ω internal active loads are on. When LOAD = GND, external 400 Ω loads must be used. The buffers <i>must</i> have a resistive load to maintain stability. |
| 9 | 9 | 9 | 10, 12 | 11, 14 | DGND | Digital Ground. DGND pins must have the same potential and be bypassed to AGND. DGND should be within $\pm 0.3V$ of AGND. |
| 11 | 11 | 11 | 14 | 16 | EDGE/ LEVEL | When this control line is high, the 2nd-rank registers are loaded with the rising edge of LATCH. If this control line is low, the 2nd-rank registers are transparent when LATCH is low, passing data directly from the 1st-rank registers to the decoders. |
| — | 12–16, 18, 22–26 | 22–26 | — | 1, 12, 23, 34 | N.C. | No connection. Not internally connected. |
| 12 | 17 | 17 | 18 | 20 | SER/ $\overline{\text{PAR}}$ | Connect to V_{CC} for serial mode; connect to GND for parallel mode. |
| 13 | 19, 30 | 19, 30 | 20, 34 | 22, 38 | V- | Negative Supply. All V- pins must be connected to each other and bypassed to GND separately (Figure 2). |
| 14 | 20 | 20 | 21 | 24 | WR | In serial mode, WR (write) shifts data into the input register. In parallel mode, WR loads data into the 1st-rank registers. Data is latched on the rising edge. |
| 15 | 21 | 21 | 22 | 25 | LATCH | If EDGE/ $\overline{\text{LEVEL}}$ = V_{CC} , data is loaded from the 1st-rank registers to the 2nd-rank registers on the rising edge of LATCH. If EDGE/ $\overline{\text{LEVEL}}$ = GND, data is loaded while LATCH = GND. In addition, data is loaded during the execution of parallel-mode functions 1011 through 1110, or if LATCH = V_{CC} during the execution of the parallel-mode “software-latch” command (1111). |

Low-Cost 4x4, 8x4, 8x8 Video Crosspoint Switches

Pin Description (continued)

| PIN | | | | | NAME | FUNCTION |
|----------------|----------------|----------------|--------------------------------|--------------------------------|------------------|---|
| MAX4359 | | MAX4360 | MAX4456 | | | |
| SO | SSOP | SSOP | DIP | PLCC | | |
| — | — | — | 23 | 26 | \overline{CE} | Active-Low Chip Enable. WR is enabled when $\overline{CE} = \text{GND}$ and $\text{CE} = V_{CC}$. WR is disabled when $\overline{CE} = V_{CC}$ and $\text{CE} = \text{GND}$. |
| 16 | 27 | 27 | 24 | 27 | CE | Active-High Chip Enable. WR is enabled when $\overline{CE} = \text{GND}$ and $\text{CE} = V_{CC}$. WR is disabled when $\overline{CE} = V_{CC}$ and $\text{CE} = \text{GND}$. |
| 17, 19, 21, 23 | 28, 31, 33, 35 | 28, 31, 33, 35 | 25, 27, 29, 31, 33, 35, 37, 39 | 28, 30, 32, 35, 37, 39, 41, 43 | OUT ₋ | Buffer Outputs. Buffer inputs are internally grounded with a 1000 or 1001 command from the D3–D0 lines. |
| 18 | 29 | 15, 29 | 28, 30, 32 | 31, 33, 36 | AGND | Analog Ground. AGND must be at 0.0V, since the gain-setting resistors of the buffers are connected to these pins. |
| 20 | 32 | 32 | 36 | 40 | D3 | Parallel Data Bit when $\text{SER}/\overline{\text{PAR}} = \text{GND}$. When $\text{D3} = \text{GND}$, D0–D2 specify the input channel to be connected to specified buffer. When $\text{D3} = V_{CC}$, D0–D2 specify control codes. D3 is not used in serial mode ($\text{SER}/\overline{\text{PAR}} = V_{CC}$). |
| 22 | 34 | 34 | 38 | 42 | D2 | Parallel Data Bit D2 when $\text{SER}/\overline{\text{PAR}} = \text{GND}$. Not used when $\text{SER}/\overline{\text{PAR}} = V_{CC}$. |
| 24 | 36 | 13, 36 | 16, 26, 40 | 18, 29, 44 | V+ | Positive Supply. All V+ pins must be connected to each other and bypassed to AGND separately (Figure 2). |

MAX4359/MAX4360/MAX4456

Low-Cost 4x4, 8x4, 8x8 Video Crosspoint Switches

Detailed Description

Output Buffers

The MAX4456 video crosspoint switch consists of 64 T-switches in an 8x8 grid (Figure 1). The eight matrix outputs are followed by eight wideband buffers optimized for driving 400Ω and 20pF loads. The MAX4359's core is a 4x4 switch matrix with each of its outputs followed by a wideband buffer. The MAX4360 has an 8x4 matrix and four output buffers. Each buffer has an internal active load on the output that can be readily shut off through the LOAD input (off when LOAD = 0V). The shut-off is useful when two or more crosspoints are connected in parallel to create more input channels. With more input channels, only one set of

buffers can be active and only one set of loads can be driven. When active, the buffer must have either 1) an internal load, 2) the internal load of another buffer in another MAX4359/MAX4360/MAX4456, or 3) an external load.

Each output can be disabled under logic control. When a buffer is disabled, its output enters a high-impedance state. In multichip parallel applications, the disable function prevents inactive outputs from loading lines driven by other devices. Disabling the inactive buffers reduces power consumption.

The outputs connect easily to MAX4395 quad, operational amplifiers when back-terminated 75Ω coaxial cable must be driven.

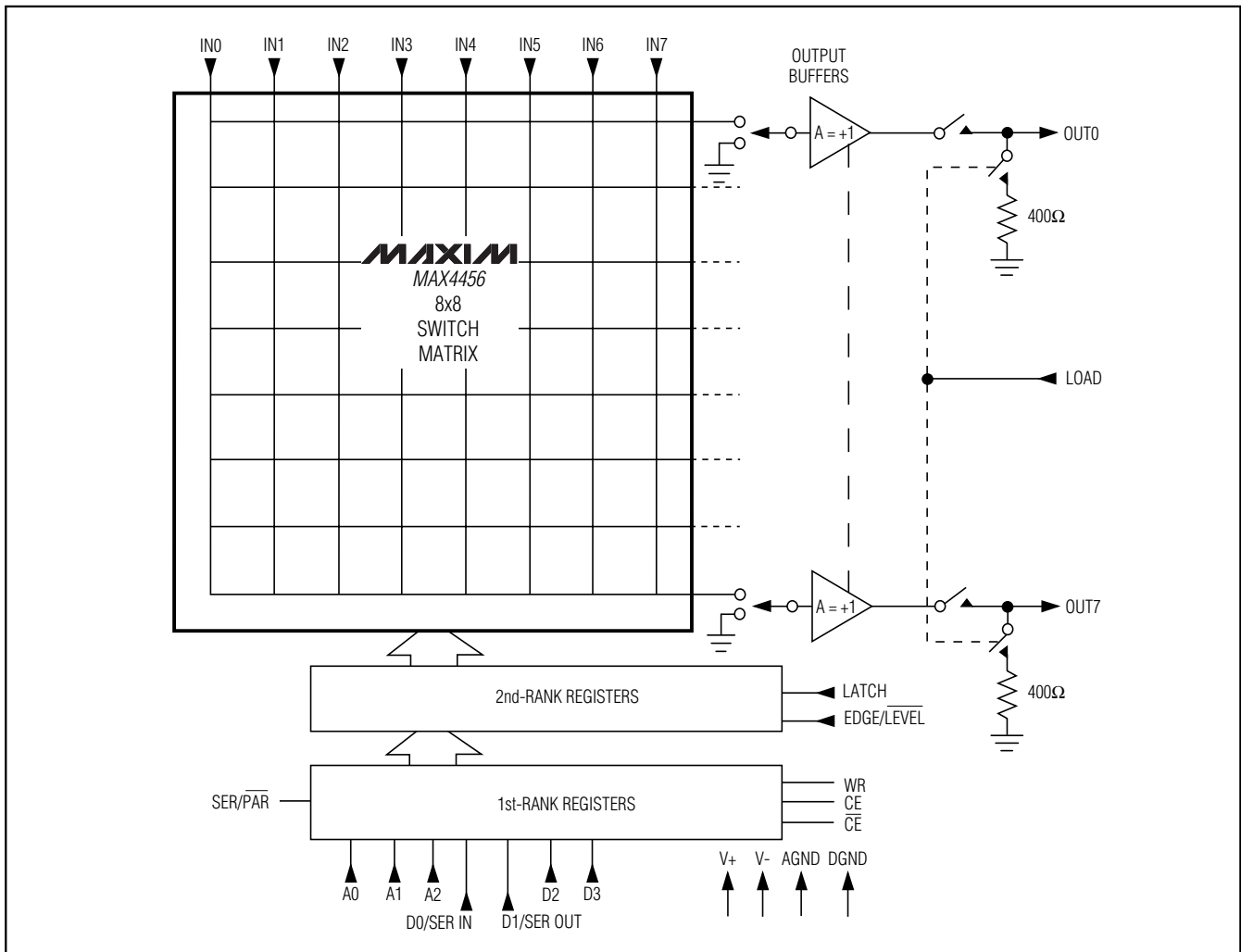


Figure 1. MAX4456 Functional Diagram

Low-Cost 4x4, 8x4, 8x8 Video Crosspoint Switches

MAX4359/MAX4360/MAX4456

Power-On RESET

The MAX4359/MAX4360/MAX4456 have an internal power-on reset (POR) circuit that remains low for 5 μ s after power is applied. POR also remains low if the total supply voltage is less than 4V. **The POR disables all buffer outputs at power-up**, but the switch matrix is not preset to any initial condition. The desired switch state should be programmed before the buffer outputs are enabled.

Digital Interface

The desired switch state can be loaded in a parallel-interface mode or serial-interface mode (Table 3 and Figures 4, 5, 6). All action associated with the WR line occurs on its rising edge. The same is true for the LATCH line if EDGE/LEVEL is high. Otherwise, the second-rank registers update while LATCH is low (when EDGE/LEVEL is low). WR is logically ANDed with CE and $\overline{\text{CE}}$ (when present) to allow active-high or active-low chip enable.

6-Bit Parallel-Interface Mode (MAX4359/MAX4360)

In the MAX4359/MAX4360's parallel-interface mode ($\text{SER}/\overline{\text{PAR}} = \text{GND}$), the six data bits specify an output channel (A1, A0) and the input channel to which it connects (D3–D0). This data is loaded on the rising edge of WR. The input channels are selected by codes 0000

through 0111 (D3–D0) for the MAX4360, and codes 0000 through 0011 (D3–D0) for the MAX4359. Note that the MAX4359 does not use codes 0100 through 0111. The eight codes 1000 through 1111 control other functions, as listed in Table 1.

7-Bit Parallel-Interface Mode (MAX4456)

In the MAX4456's parallel-interface mode ($\text{SER}/\overline{\text{PAR}} = \text{GND}$), the seven data bits specify an output channel (A2, A1, A0) and the input channel to which it connects (D3–D0). This data is loaded on the rising edge of WR. The input channels are selected by codes 0000 through 0111 (D3–D0) for the MAX4456. The remaining eight codes 1000 through 1111 control other functions, as listed in Table 1.

16-Bit Serial-Interface Mode (MAX4359/MAX4360)

In serial mode ($\text{SER}/\overline{\text{PAR}} = \text{VCC}$), all first-rank registers are loaded with data, making it unnecessary to specify an output address (A1, A0). The input data format is D3–D0, starting with OUT0 and ending with OUT3 for 16 total bits. For the MAX4360, only codes 0000 through 1010 are valid. For the MAX4359, only the codes 0000 through 0011 and codes 1000 through 1010 are valid. Code 1010 disables a buffer, while code 1001 enables it. After data is shifted into the 16-bit first-rank register, it is transferred to the second rank by LATCH (Table 2), which updates the switches.

Table 1. Parallel-Interface Mode Functions

| A2, A1, A0 | D3–D0 | FUNCTION |
|-----------------------|---------------|--|
| Selects Output Buffer | 0000 to 0111 | Connect the buffer selected by A2–A0 (MAX4456) or A1–A0 (MAX4359/MAX4360) to the input channel selected by D3–D0. |
| | 1000 | Connect the buffer selected by A2–A0 (MAX4456) or A1–A0 (MAX4359/MAX4360) to DGND. Note, if the buffer output is on, its output is its offset voltage. |
| | 1011 | Shut off the buffer selected by A2–A0 (MAX4456) or A1–A0 (MAX4359/MAX4360) and retain 2nd-rank registers contents. |
| | 1100 | Turn on the buffer selected by A2–A0 (MAX4456) or A1–A0 (MAX4359/MAX4360, and restore the previously connected channel. |
| | 1101 | Turn off all buffers, and leave 2nd-rank registers unchanged. |
| | 1110 | Turn on all buffers, and restore the connected channels. |
| | 1111 | Send a pulse to the 2nd-rank registers to load them with the contents of the 1st-rank registers. When latch is held high, this "software-LATCH" command performs the same function as pulsing LATCH low. |
| | 1001 and 1010 | Do not use these codes in the parallel-interface mode. These codes are for the serial-interface mode only. |
| | 0100 and 0111 | For the MAX4359, unused codes. |

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32-Bit Serial-Interface Mode (MAX4456)

In serial mode (SER/PAR = V_{CC}), all first-rank registers are loaded with data, making it unnecessary to specify an output address (A2, A1, A0). The input data format is D3–D0, starting with OUT0 and ending with OUT7 for 32 total bits. Only codes 0000 through 1010 are valid. Code 1010 disables a buffer, while code 1001 enables it. After data is shifted into the 32-bit first-rank register, it is transferred to the second rank by LATCH (Table 2), which updates the switches.

Table 2. Serial-Interface Mode Functions

| D3–D0 | FUNCTION |
|--------------|--|
| 0000 to 0111 | Connect the selected buffer to the input channel selected by D3–D0. Note that 0100 through 0111 are not valid for the MAX4359. |
| 1000 | Connect the input of the selected buffer to GND. Note: If the buffer output remains on, its input is its offset voltage. |
| 1001 | Turn on the selected buffer and connect its input to GND. Use this code to turn on buffers after power is applied. The default power-up state is all buffers disabled. |
| 1010 | Shut off the selected buffer at the specified channel, and erase data stored in the 2nd rank of registers. The 2nd rank now holds the command word 1010. |
| 1011 to 1111 | Do not use these codes in the serial-interface mode. They inhibit the latching of the 2nd-rank registers, which prevents proper data loading. |

Table 3. Input/Output Line Configurations

| SERIAL / PARALLEL | D3 | D2 | D1 | D0 | (A2), A1, A0 | COMMENT |
|-------------------|----|----------------|----------------|----------------|-----------------------|--------------------------------------|
| H | X | X | Serial Output | Serial Input | X | Serial Mode |
| L | H | Parallel Input | Parallel Input | Parallel Input | Output Buffer Address | Parallel Mode, D0–D2 = Control Code |
| L | L | Parallel Input | Parallel Input | Parallel Input | Output Buffer Address | Parallel Mode, D0–D2 = Input Address |

X = Don't care, H = 5V, L = 0V
() are for MAX4456 only.

Typical Application

Figure 2 shows a typical application of the MAX4456 (PDIP) with the MAX4395 quad, operational amplifiers at the outputs to drive 75Ω loads. This application shows the MAX4456 digital-switch control interface set up in the 7-bit parallel mode. The MAX4456 uses seven data lines and two control lines (WR and LATCH). Two additional lines may be needed to control CE and LOAD when using multiple MAX4456s.

The input/output information is presented to the chip at A2, A1, A0, and D3–D0 by a parallel printer port. The data is stored in the 1st-rank registers on the rising edge of WR. When the LATCH line goes high, the switch configuration is loaded into the 2nd-rank registers, and all eight outputs enter the new configuration at the same time. Each 7-bit word updates only one output buffer at a time. If several buffers are to be updated, the data is individually loaded into the 1st-rank registers. Then, a single LATCH pulse is used to reconfigure all channels simultaneously.

The short BASIC program in Figure 3 loads programming data into the MAX4456 from any IBM PC or compatible. It uses the computer's "LPT1" output to interface to the circuit, then automatically finds the address for LPT1 and displays a table of valid input values to be used. The program does not keep track of previous commands, but it does display the last data sent to LPT1, which is written and latched with each transmission. A similar application is possible with the MAX4359/MAX4360.

Chip Information

MAX4359 TRANSISTOR COUNT: 2372

MAX4360 TRANSISTOR COUNT: 2372

MAX4456 TRANSISTOR COUNT: 3820

Low-Cost 4x4, 8x4, 8x8 Video Crosspoint Switches

MAX4359/MAX4360/MAX4456

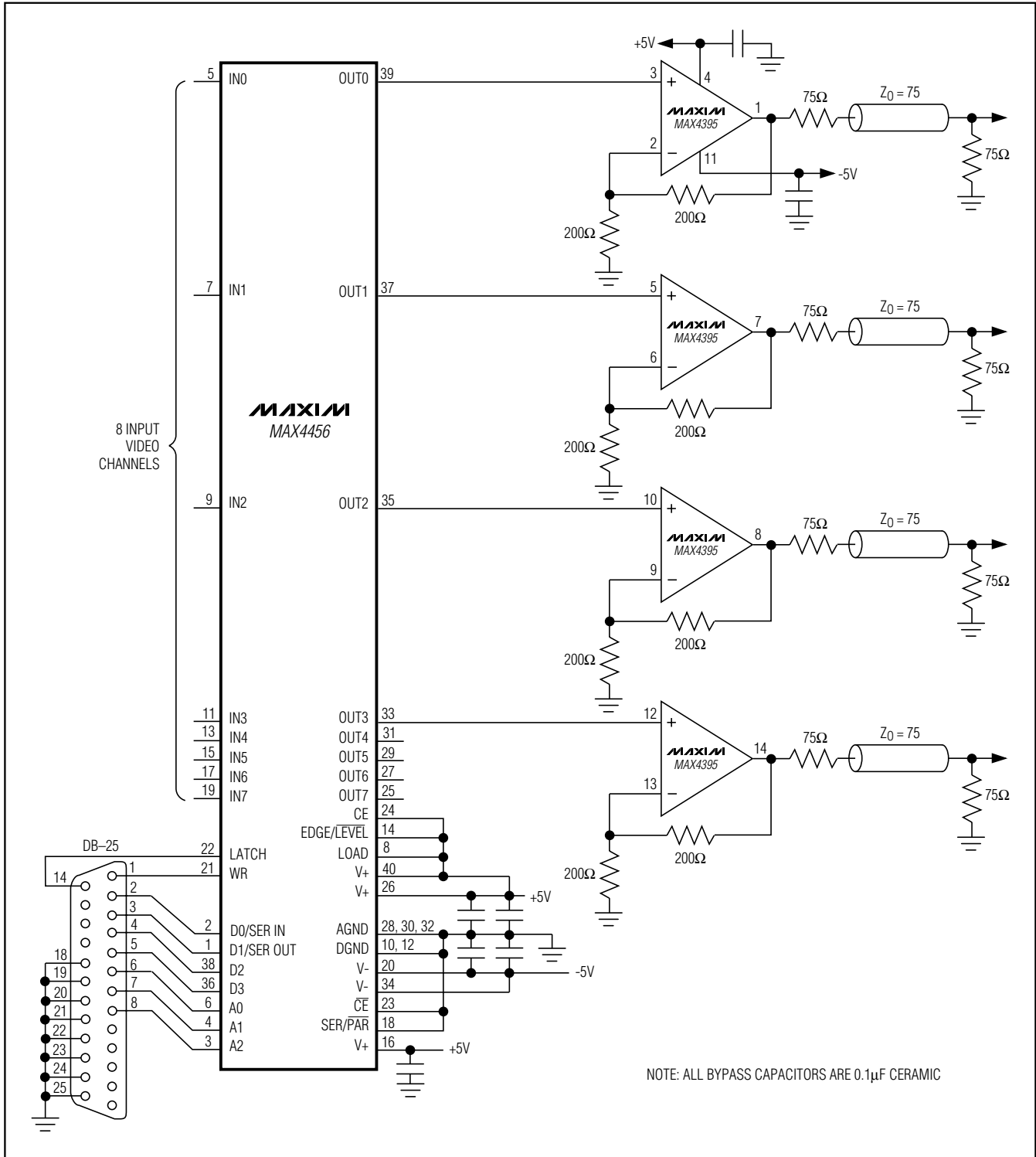


Figure 2. MAX4456 (plastic DIP) Typical Application Circuit

Low-Cost 4x4, 8x4, 8x8 Video Crosspoint Switches

```

10 REM MAX4456st rev. 4/26/90 : CLS
20 DIM VALU(5,5): COL=17 : RO=5
30 DEF SEG=&H0 : ADDRESS=(PEEK(&H409)*256)+(PEEK(&H408))
40 LOCATE RO-4,COL-2 : PRINT"MAX4456 8 X 8 CROSSPOINT SWITCH"
50 LOCATE RO+8,COL-12 : PRINT " Input and control codes:"
60 LOCATE RO+10,COL-16 : PRINT "0 to 7 = Valid channel and buffer input values"
70 LOCATE RO+11,COL-12 : PRINT " 8 = Specify Buffer input to connect to ground"
80 LOCATE RO+12,COL-12 : PRINT "11 = Shut off specified Buffer output"
90 LOCATE RO+13,COL-12 : PRINT "12 = Turn on specified Buffer output"
100 LOCATE RO+14,COL-12 : PRINT "13 = Shut off all Buffer outputs"
110 LOCATE RO+15,COL-12 : PRINT "14 = Turn on all Buffer outputs"
120 LOCATE RO+16,COL-12 : PRINT " E = End Program"
130 LOCATE RO+0,COL+21 : PRINT " "
140 LOCATE RO-1,COL+5 : PRINT "Input Channel or "
150 LOCATE RO+0,COL+5 : INPUT "Control Code ? ",CH$ : REM D0-D3
160 CH=VAL(RIGHT$(CH$,2)) : IF CH<0 OR CH>15 OR CH=9 OR CH=10 THEN 130
170 IF RIGHT$(CH$,1)="E" OR RIGHT$(CH$,1)="e" THEN END
180 LOCATE RO+1,COL+5 : INPUT "Buffer Output ? ",AM$ : REM A0-A2
190 LOCATE RO+1,COL+21 : PRINT " "
200 AM=VAL(RIGHT$(AM$,1)) : IF AM<0 OR AM>7 THEN 180
210 LOCATE RO+3,COL+5 : PRINT "OUTPUT VALUES"
220 LOCATE RO+4,COL+5 : PRINT "DATA=";CH : LOCATE RO+4,COL+15 :PRINT" BUF=";AM
230 OUT ADDRESS,(AM*16)+CH : REM DATA OUT
240 OUT ADDRESS+2,1 : REM Write low DB25-1
250 OUT ADDRESS+2,2 : REM Latch low DB25-14 and WR hi DB25-1
260 OUT ADDRESS+2,0 : REM take Latch hi
270 GOTO 130

```

Figure 3. BASIC Program for Loading Data into the MAX4456 from a PC Using Figure 2's Circuit

Timing Diagrams

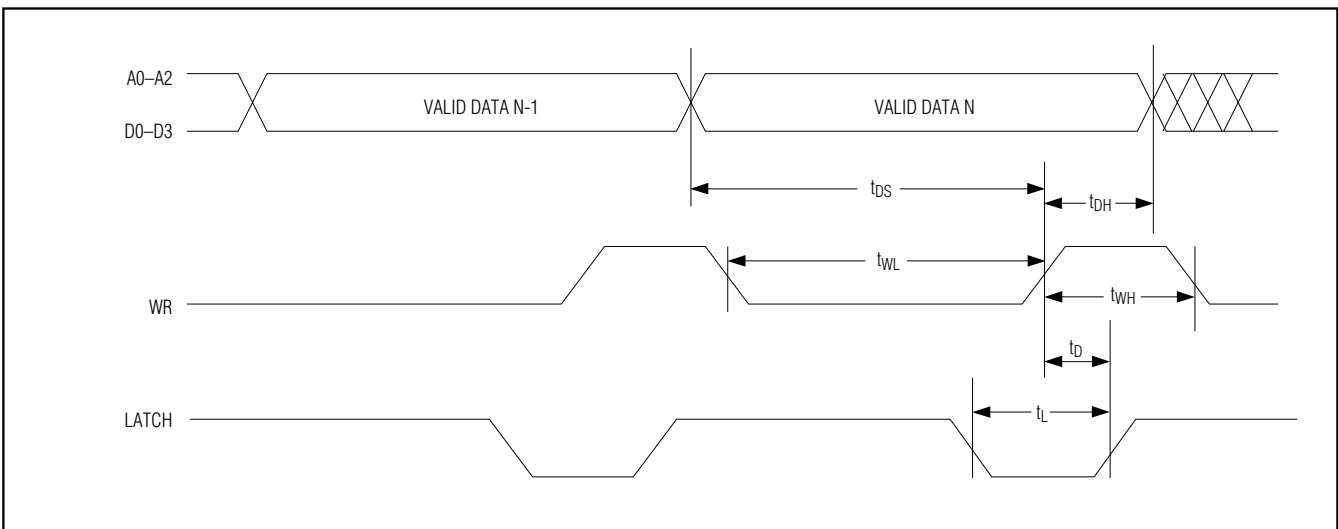


Figure 4. Write Timing for Serial- and Parallel-Interface Modes

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Timing Diagrams (continued)

MAX4359/MAX4360/MAX4456

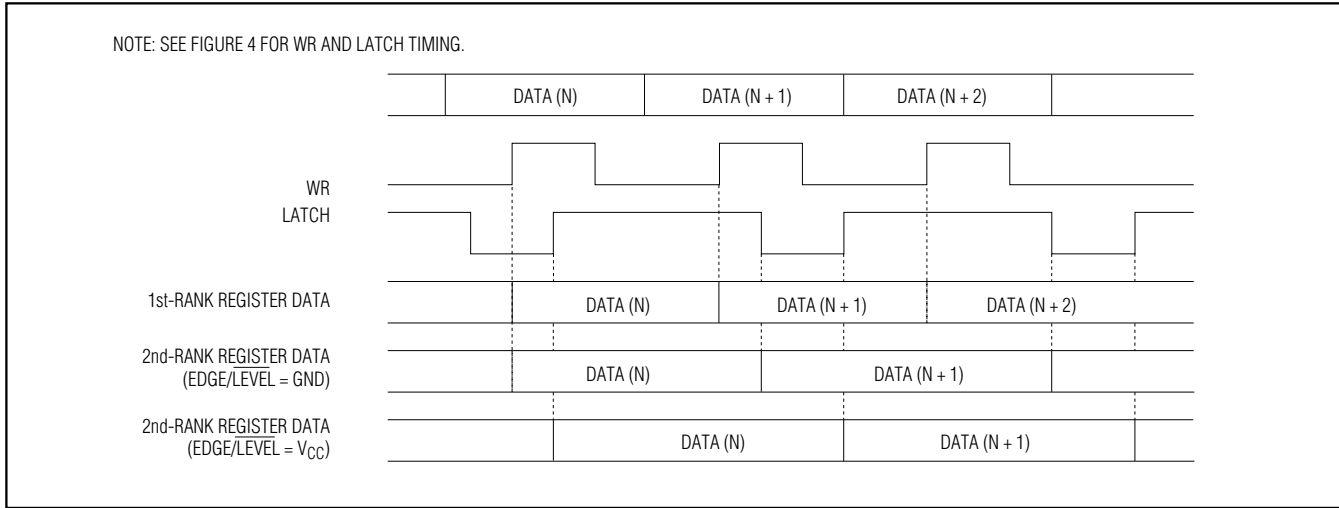


Figure 5. Parallel-Interface Mode Format ($SER/\overline{PAR} = GND$)

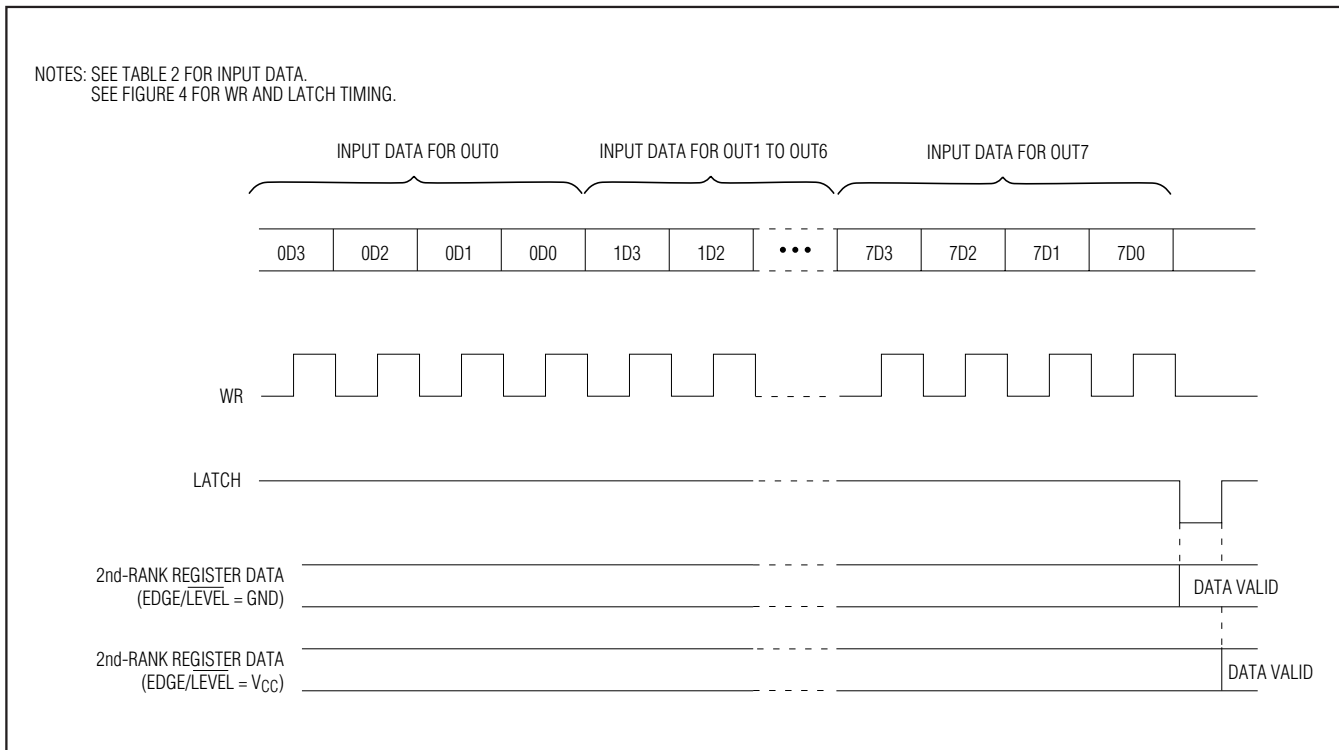
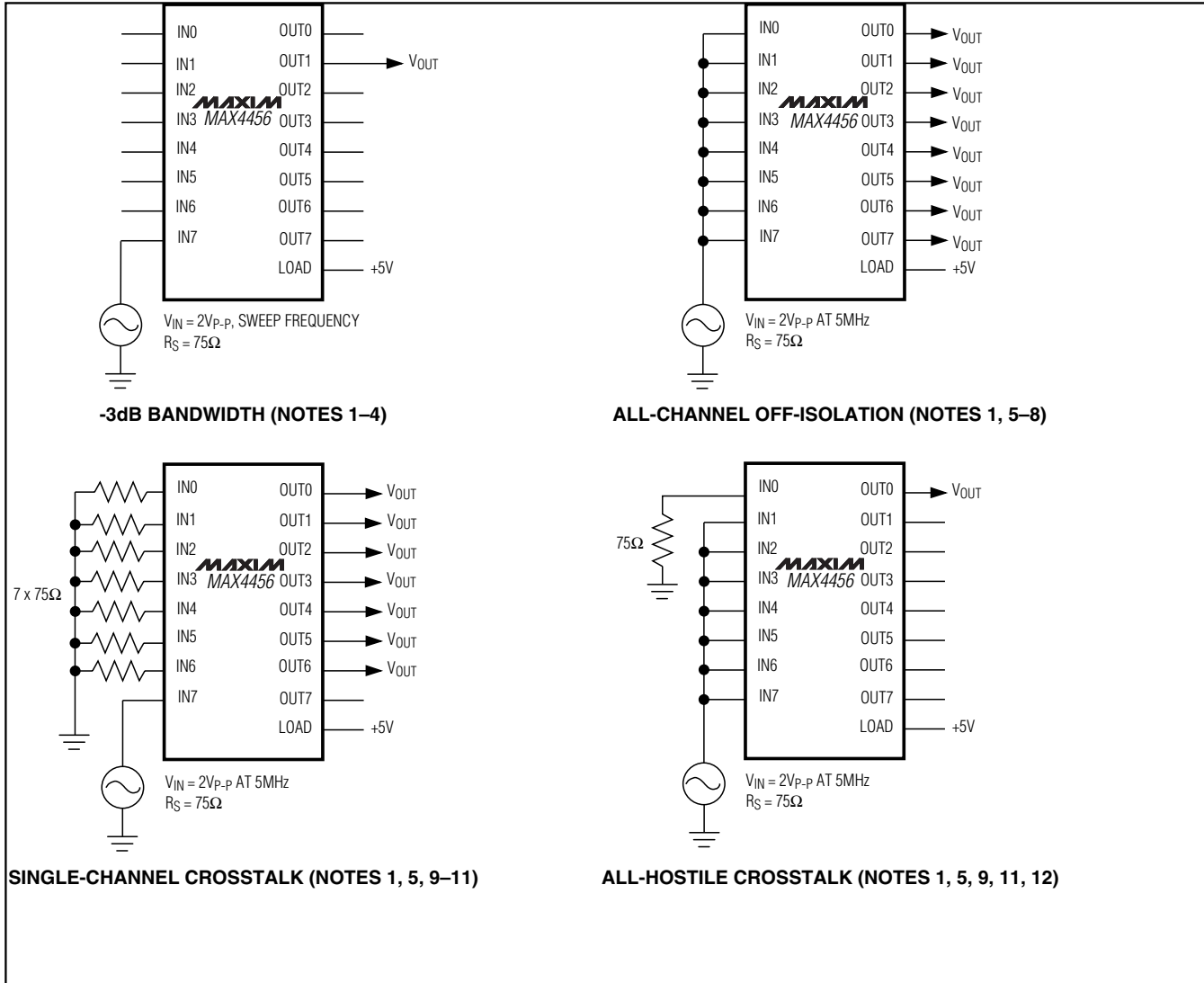


Figure 6. Serial-Mode Interface Format ($SER/\overline{PAR} = VCC$)

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Dynamic Test Circuits

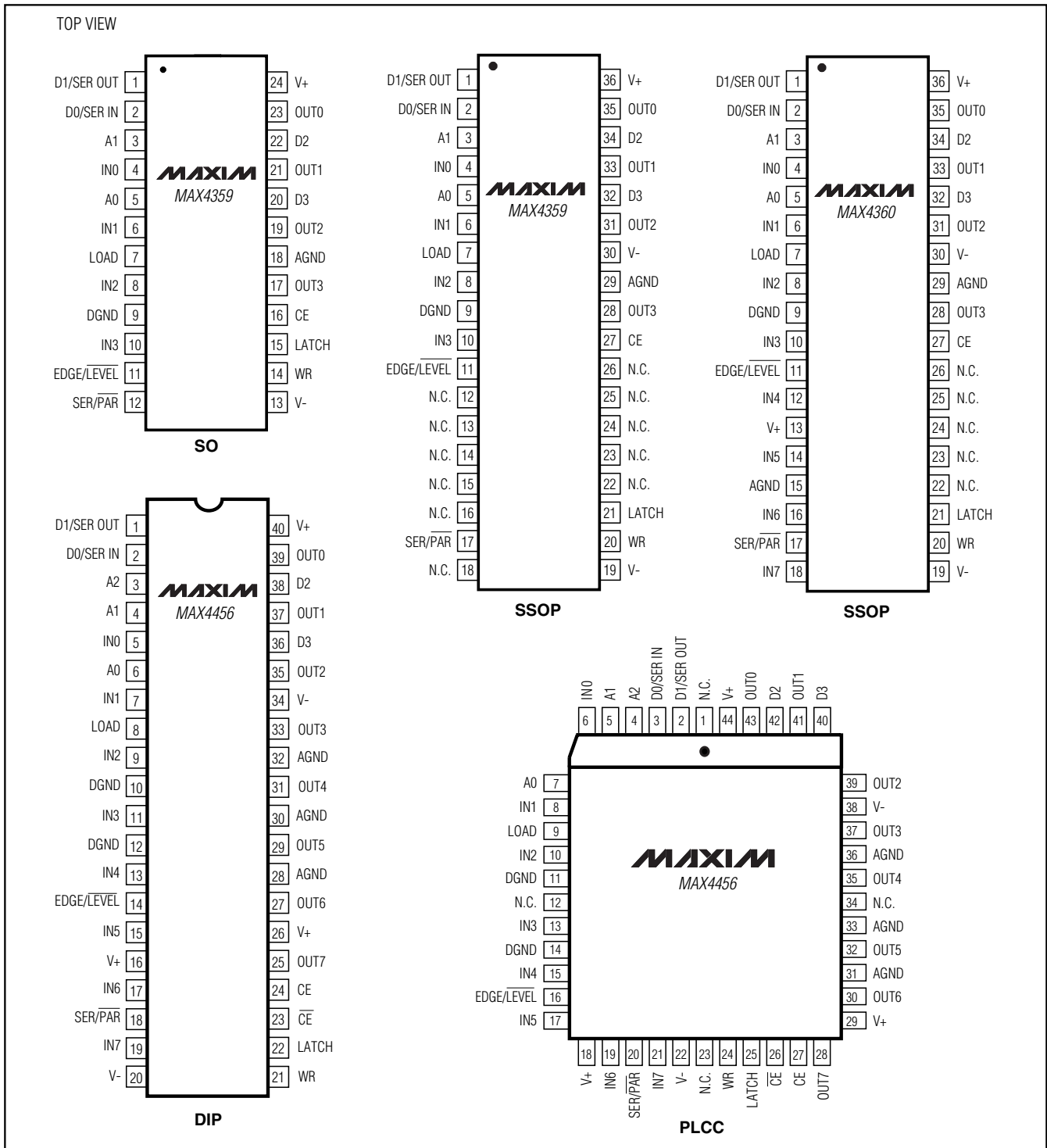


- Note 1:** Connect LOAD to +5V (internal 400Ω loads on at all outputs).
- Note 2:** Program any one input to connect to any one output. See Table 1 or 2 for programming codes.
- Note 3:** Turn on the buffer at the selected output (Table 1 or 2).
- Note 4:** Drive the selected input with V_{IN} , and measure V_{OUT} at the -3dB frequency at the selected output.
- Note 5:** Program each numbered input to connect to the same numbered output (IN0 to OUT0, IN1 to OUT1, etc., for the MAX4456; also IN4 to OUT0, IN5 to OUT1, etc., for the MAX4360.) See Table 1 or 2 for programming codes.
- Note 6:** Turn off all output buffers (Table 1 or 2).
- Note 7:** Drive all inputs with V_{IN} , and measure V_{OUT} at any output.
- Note 8:** Isolation (in dB) = $20\log_{10}(V_{OUT}/V_{IN})$.
- Note 9:** Turn on all output buffers (Table 1 or 2).
- Note 10:** Drive any one input with V_{IN} , and measure V_{OUT} at any undriven output.
- Note 11:** Crosstalk (in dB) = $20\log_{10}(V_{OUT}/V_{IN})$.
- Note 12:** Drive all but one input with V_{IN} , and measure V_{OUT} at the undriven output.

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Pin Configurations

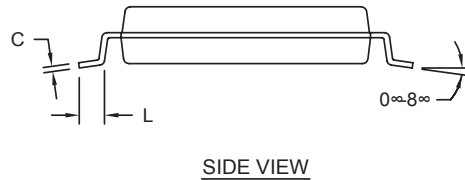
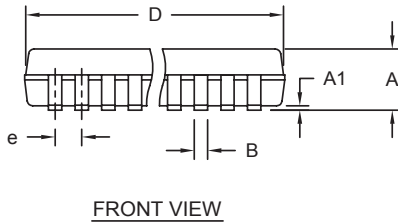
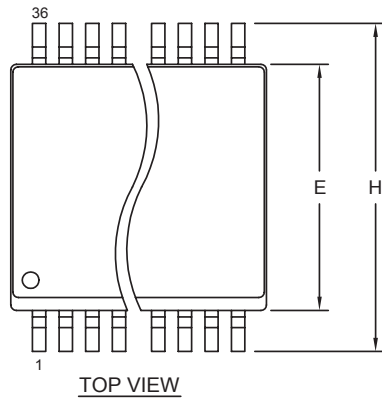
MAX4359/MAX4360/MAX4456



Low-Cost 4x4, 8x4, 8x8 Video Crosspoint Switches

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)



| DIM | INCHES | | MILLIMETERS | |
|-----|------------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.096 | 0.104 | 2.44 | 2.65 |
| A1 | 0.004 | 0.011 | 0.10 | 0.29 |
| B | 0.012 | 0.017 | 0.30 | 0.44 |
| C | 0.009 | 0.013 | 0.23 | 0.32 |
| e | 0.0315 BSC | | 0.80 BSC | |
| E | 0.291 | 0.299 | 7.40 | 7.60 |
| H | 0.398 | 0.414 | 10.11 | 10.51 |
| L | 0.020 | 0.040 | 0.51 | 1.02 |
| D | 0.598 | 0.612 | 15.20 | 15.55 |

NOTES:

1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.

DALLAS SEMICONDUCTOR **MAXIM**
 PROPRIETARY INFORMATION
 TITLE:
 PACKAGE OUTLINE, 36L SSOP, 0.80 MM PITCH
 APPROVAL: _____ DOCUMENT CONTROL NO. 21-0040 REV. E 1/1

SSOP-EPS

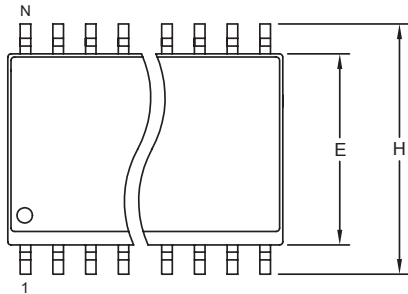
Low-Cost 4x4, 8x4, 8x8 Video Crosspoint Switches

Package Information (continued)

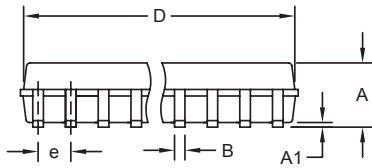
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)

MAX4359/MAX4360/MAX4456

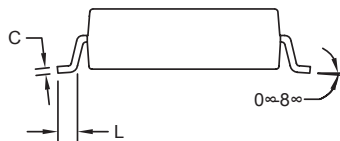
SOICWLEPS



TOP VIEW



FRONT VIEW



SIDE VIEW

| DIM | INCHES | | MILLIMETERS | |
|-----|--------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.093 | 0.104 | 2.35 | 2.65 |
| A1 | 0.004 | 0.012 | 0.10 | 0.30 |
| B | 0.014 | 0.019 | 0.35 | 0.49 |
| C | 0.009 | 0.013 | 0.23 | 0.32 |
| e | 0.050 | | 1.27 | |
| E | 0.291 | 0.299 | 7.40 | 7.60 |
| H | 0.394 | 0.419 | 10.00 | 10.65 |
| L | 0.016 | 0.050 | 0.40 | 1.27 |

VARIATIONS:

| DIM | INCHES | | MILLIMETERS | | N | MS013 |
|-----|--------|-------|-------------|-------|----|-------|
| | MIN | MAX | MIN | MAX | | |
| D | 0.398 | 0.413 | 10.10 | 10.50 | 16 | AA |
| D | 0.447 | 0.463 | 11.35 | 11.75 | 18 | AB |
| D | 0.496 | 0.512 | 12.60 | 13.00 | 20 | AC |
| D | 0.598 | 0.614 | 15.20 | 15.60 | 24 | AD |
| D | 0.697 | 0.713 | 17.70 | 18.10 | 28 | AE |

NOTES:

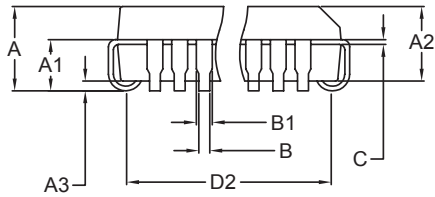
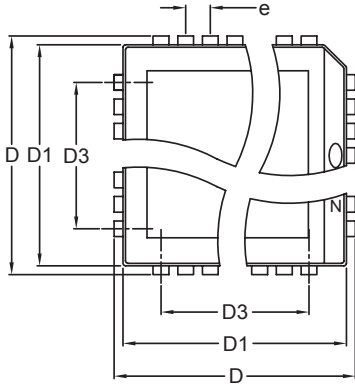
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS013.
6. N = NUMBER OF PINS.

| | | |
|--|---------------------------------|---------------|
| | | |
| <small>PROPRIETARY INFORMATION</small> | | |
| TITLE: PACKAGE OUTLINE, .300" SOIC | | |
| APPROVAL | DOCUMENT CONTROL NO. 21-0042 | REV. B 1/1 |

Low-Cost 4x4, 8x4, 8x8 Video Crosspoint Switches

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)



| | INCHES | | MILLIMETERS | |
|----|--------|-------|-------------|------|
| | MIN | MAX | MIN | MAX |
| A | 0.165 | 0.180 | 4.20 | 4.57 |
| A1 | 0.090 | 0.120 | 2.29 | 3.04 |
| A2 | 0.145 | 0.156 | 3.69 | 3.96 |
| A3 | 0.020 | --- | 0.51 | --- |
| B | 0.013 | 0.021 | 0.33 | 0.53 |
| B1 | 0.026 | 0.032 | 0.66 | 0.81 |
| C | 0.009 | 0.011 | 0.23 | 0.28 |
| e | 0.050 | | 1.27 | |

| | INCHES | | MILLIMETERS | | N | MO047 |
|----|--------|-------|-------------|-------|----|-------|
| | MIN | MAX | MIN | MAX | | |
| D | 0.385 | 0.395 | 9.78 | 10.03 | 20 | AA |
| D1 | 0.350 | 0.356 | 8.89 | 9.04 | | |
| D2 | 0.290 | 0.330 | 7.37 | 8.38 | | |
| D3 | 0.200 | REF | 5.08 | REF | | |

| | | | | | | |
|----|-------|-------|-------|-------|----|----|
| D | 0.485 | 0.495 | 12.32 | 12.57 | 28 | AB |
| D1 | 0.450 | 0.456 | 11.43 | 11.58 | | |
| D2 | 0.390 | 0.430 | 9.91 | 10.92 | | |
| D3 | 0.300 | REF | 7.62 | REF | | |

| | | | | | | |
|----|-------|-------|-------|-------|----|----|
| D | 0.685 | 0.695 | 17.40 | 17.65 | 44 | AC |
| D1 | 0.650 | 0.656 | 16.51 | 16.66 | | |
| D2 | 0.590 | 0.630 | 14.99 | 16.00 | | |
| D3 | 0.500 | REF | 12.70 | REF | | |

| | | | | | | |
|----|-------|-------|-------|-------|----|----|
| D | 0.785 | 0.795 | 19.94 | 20.19 | 52 | AD |
| D1 | 0.750 | 0.756 | 19.05 | 19.20 | | |
| D2 | 0.690 | 0.730 | 17.53 | 18.54 | | |
| D3 | 0.600 | REF | 15.24 | REF | | |

| | | | | | | |
|----|-------|-------|-------|-------|----|----|
| D | 0.985 | 0.995 | 25.02 | 25.27 | 68 | AE |
| D1 | 0.950 | 0.958 | 24.13 | 24.33 | | |
| D2 | 0.890 | 0.930 | 22.61 | 23.62 | | |
| D3 | 0.800 | REF | 20.32 | REF | | |

NOTES:

1. D1 DOES NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .20mm (.008") PER SIDE.
3. LEADS TO BE COPLANAR WITHIN .10mm.
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MO047-XX AS SHOWN IN TABLE.
6. N = NUMBER OF PINS.

| | | |
|--|---------------------------------|---------------|
| | | |
| <small>PROPRIETARY INFORMATION</small> | | |
| TITLE: FAMILY PACKAGE OUTLINE: 20L, 28L, 44L, 52L, 68L PLCC | | |
| APPROVAL | DOCUMENT CONTROL NO. 21-0049 | REV. D 1/1 |

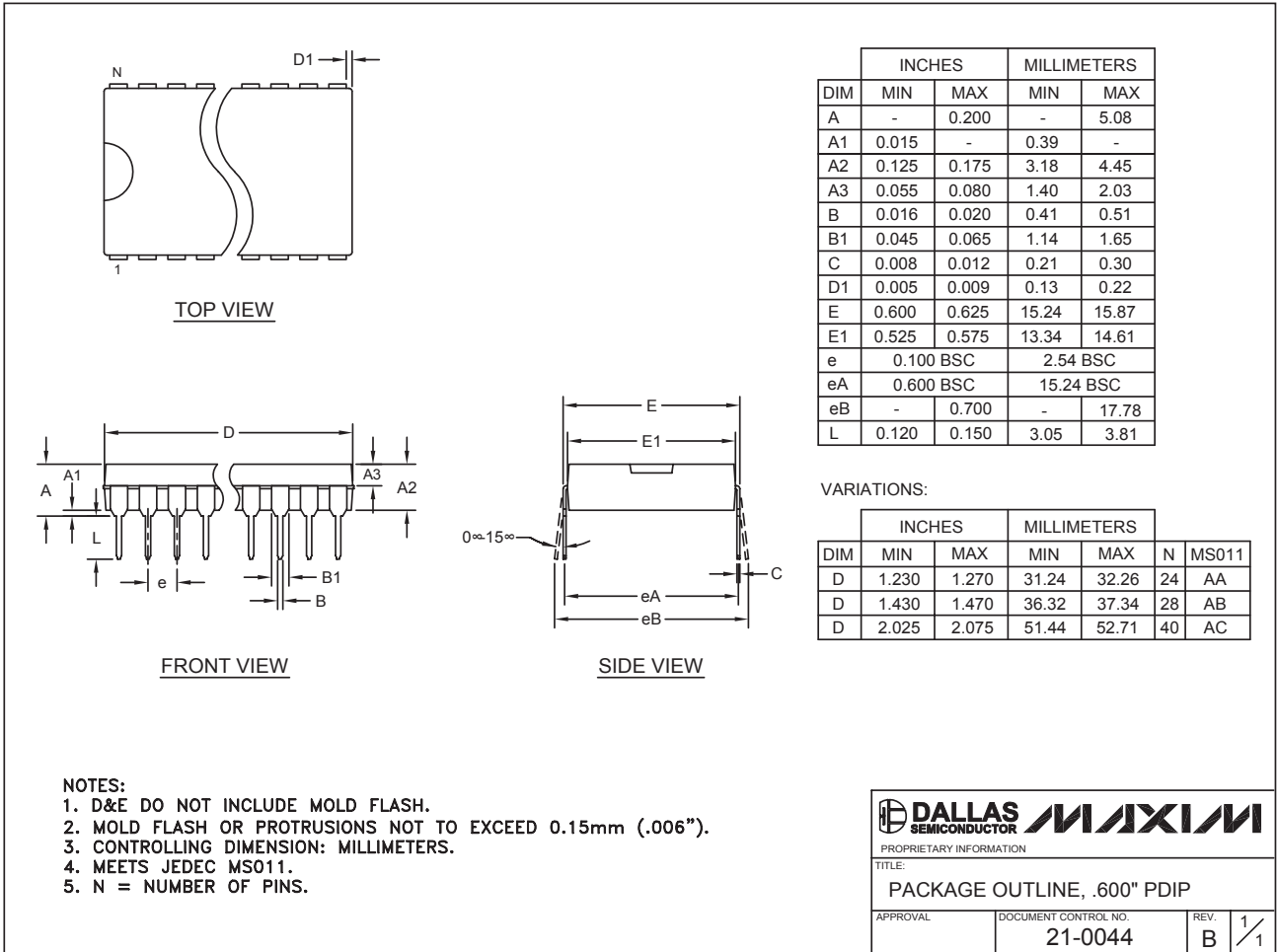
PLCC:EPS

Low-Cost 4x4, 8x4, 8x8 Video Crosspoint Switches

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)

MAX4359/MAX4560/MAX4456



Revision History

Pages changed at Rev 2: 1, 6, 8, 9, 14-17

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