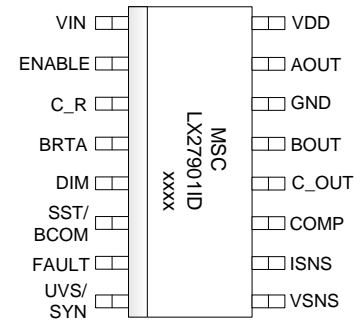


**ABSOLUTE MAXIMUM RATINGS**

|  |                   |
|--|-------------------|
| Supply Input Voltage, VIN  | 0.3V to 36V       |
| Signal Outputs, VDD, AOUT, BOUT, C_OUT                               | -0.3V to 6.5V     |
| Signal Inputs, C_R, BRTA   | -0.3V to VDD+0.3V |
| Signal Inputs, ENABLE, DIM, ISNS, VSNS, UVS/SYN                      | -0.3V to VDD+0.3V |
| Signal Outputs COMP, SST/BCOM, FAULT                                 | -0.3V to VDD      |
| Maximum Junction Temperature   | 150°C             |
| Storage Temperature Range  | -65°C to 150°C    |
| Peak Package Solder Reflow Temperature (40 seconds maximum exposure) | 260°C             |
| Lead Temperature. (Soldering 10 seconds)                             | 300°C             |

Notes: Exceeding these ratings could cause damage to the device. All voltages are with respect to GND. Currents are positive into, negative out of specified terminal. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" are not implied. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.

**PACKAGE PIN OUT**

**LX27901ID  
D PACKAGE**

(Top View)

RoHS / Pb-free Matte Tin Pin Finish

**ELECTRICAL CHARACTERISTICS**

Unless otherwise listed, the following specifications apply over the operating ambient temperature of  $-40^{\circ}\text{C} < \text{Temp} < 85^{\circ}\text{C}$ , and  $\text{VIN} = 7.5\text{V to } 27\text{V}$ , except where otherwise noted and the following test conditions:  $\text{VIN} = 12\text{V}$ ,  $\text{C}_{\text{C}_R} = 330\text{pF}$ ,  $\text{R}_{\text{C}_R} = 15\text{k}\Omega$

| Parameters                           | Symbol               | Test Conditions/Comments  | MIN  | TYP  | MAX  | Units         |
|--------------------------------------|----------------------|---|------|------|------|---------------|
| <b>Power</b>                         |                      |   |      |      |      |               |
| Controller Input Voltage             | VIN                  |   | 7.5  |      | 27   | V             |
| Controller Operating Voltage         | VDD                  | 1 $\mu\text{F}$ bypass cap on VDD pin, $\text{I}_{\text{VDD}} = 0$ to 5mA | 5.0  | 5.25 | 5.5  | V             |
| Power Supply Input Current           | IIN                  | AOUT, BOUT = no load, VDD = no load                                       |      | 7    | 10   | mA            |
| Sleep Mode Current                   | IDD <sub>SLEEP</sub> | VIN = 24V, V <sub>ENABLE</sub> < 0.8V                                     |      | 200  | 400  | $\mu\text{A}$ |
| VDD Off Voltage                      |                      | ENABLE < 0.8V   |      | 0.1  |      | V             |
| <b>Enable</b>                        |                      |   |      |      |      |               |
| ENABLE On                            | EN <sub>H</sub>      |   | 1.7  |      |      | V             |
| Shut Down                            | EN <sub>L</sub>      |   |      |      | 0.8  | V             |
| LLC Resonant Mode Threshold          | V <sub>LLCTH</sub>   | LLC resonant drive mode, VDD = 5.25V $\pm$ 0.25V <sup>①</sup>             | 2    |      | 2.8  | V             |
| PWM Switching Mode Threshold         | V <sub>PWMTH</sub>   | PWM switching drive mode, VDD = 5.25V $\pm$ 0.25V                         | 3.2  | 3.5  | 3.7  | V             |
| Synchronous LED Drive Mode Threshold | V <sub>SYN</sub>     | Synchronous LED drive mode, VDD = 5.25V $\pm$ 0.25V                       | 4.3  |      | VDD  | V             |
| Input High Current                   | EN <sub>IHH</sub>    | ENABLE = 2V   |      |      | 10   | $\mu\text{A}$ |
| Input Low Current                    | EN <sub>IIL</sub>    | 0V < V <sub>ENABLE</sub> < 0.8V   |      |      | 5    | $\mu\text{A}$ |
| <b>Under Voltage Lockout</b>         |                      |   |      |      |      |               |
| VDD Startup Threshold                | VDD <sub>UVLOR</sub> | Rising Threshold.   | 4.3  | 4.6  | 4.9  | V             |
| VDD UVLO Threshold                   | VDD <sub>UVLOF</sub> | Falling Threshold.  | 3.95 | 4.25 | 4.55 | V             |
| VDD UVLO Hysteresis                  | VDD <sub>UVLOH</sub> |   |      | 0.4  |      | V             |

① NOTE: The LX27901 operates at LLC mode when the Enable voltage  $\geq 1.7\text{V}$  @ VIN=12V

**ELECTRICAL CHARACTERISTICS**

Unless otherwise listed, the following specifications apply over the operating ambient temperature of  $-40^{\circ}\text{C} < \text{Temp} < 85^{\circ}\text{C}$ , and  $V_{\text{IN}} = 7.5\text{V}$  to  $27\text{V}$ , except where otherwise noted and the following test conditions:  $V_{\text{IN}} = 12\text{V}$ ,  $C_{\text{C}_R} = 330\text{pF}$ ,  $R_{\text{C}_R} = 15\text{k}\Omega$

| Parameters                             | Symbol                       | Test Conditions/Comments   | MIN   | TYP  | MAX   | Units         |
|--|------------------------------|--|-------|------|-------|---------------|
| <b>Output</b>                          |                              |  |       |      |       |               |
| Output Resistance                      | $R_{\text{SINK}}$            | $I_{\text{SINK}}$ , AOUT and BOUT, $T_A = 25^{\circ}\text{C}$  |       | 5    | 6     | $\Omega$      |
| Output Resistance                      | $R_{\text{SOURCE}}$          | $I_{\text{SOURCE}}$ , AOUT and BOUT, $T_A = 25^{\circ}\text{C}$  |       | 5    | 6     | $\Omega$      |
| Dead Time                              | $\text{OUT}_{\text{DT}}$     | $T_A = 25^{\circ}\text{C}$ , at full duty  | 270   | 350  | 430   | ns            |
| C_OUT Output Resistance                | $R_{\text{C}_\text{OUT}}$    | Source and sink  |       | 10   | 20    | $\Omega$      |
| <b>Switching Frequency Oscillator</b>  |                              |  |       |      |       |               |
| Switching Frequency Tolerance          | OSCIN                        | $T_A = 25^{\circ}\text{C}$ , Frequency of AOUT, BOUT in PWM mode, $C_{\text{C}_R} = 330\text{pF}$ , $R_{\text{C}_R} = 15\text{K}$ .  | 138   | 150  | 162   | kHz           |
| LLC Frequency Control Current Source   |                              | $V_{\text{ENABLE}} < 2.8\text{V}$  | 0     | 160  |       | $\mu\text{A}$ |
| Ramp Valley Voltage                    | OSCVV                        |  |       | 0.5  |       | V             |
| Ramp Peak Voltage                      | OSCPV                        |  |       | 2.5  |       | V             |
| Synchronization Range                  |                              | Ratio of UVS/SYN input over C_R oscillator free run frequency  | 1.05  |      | 3     | Ratio         |
| <b>LED Dimming Control</b>             |                              |  |       |      |       |               |
| ISNS Reference                         | $\text{ISNS}_{\text{REF}}$   | $T_A = 25^{\circ}\text{C}$ , input, Corresponds to 2V after 4.75X internal amplifier.  | 414.6 | 421  | 427.4 | mV            |
| ISNS Linear Input Range                |                              | Linear operation range for internal circuit  | 600   |      |       | mV            |
| BRTA Input Range                       |                              | 4.75X of ISNS signal. Input outside the range is clamped at upper or lower limit internally.   | 0.5   |      | 2.0   | V             |
| Pre-Amplifier Gain                     | $K_{\text{PRAMP}}$           |  |       | 4.75 |       |               |
| Error Amp Output Capacity              |                              | Source and Sink  |       | 100  |       | $\mu\text{A}$ |
| DIM Input Voltage Range                | $V_{\text{DIM}}$             | Effective for duty from 0 to 100%  | 0.5   |      | 2.0   | V             |
| PWM Dimming Mode Control Threshold     | $V_{\text{PDMODETH}}$        | Voltage level of FAULT pin, in ACU_BRITE PWM dimming mode when below threshold; in conventional PWM dimming mode when above threshold.   | 2.8   | 3.0  | 3.2   | V             |
| <b>Fault Monitoring and Protection</b> |                              |  |       |      |       |               |
| VSNS Threshold                         | $\text{VSNS}_{\text{TH}}$    |  | 1.8   | 2.0  | 2.2   | V             |
| $\Delta\text{VCOMP}$ Voltage           | $V_{\text{VCOMP\_diff}}$     | $V_{\text{comp2}}$ when the Aout present @ $V_{\text{sns}}=0\text{V}$ , $\text{ISNS}=0.15\text{V}$ ; $V_{\text{comp1}}$ when the Aout disabled @ $V_{\text{sns}}=3\text{V}$ , $\text{ISNS}=0\text{V}$ ; $T_A = 25^{\circ}\text{C}$<br>$\Delta\text{VCOMP Voltage} = V_{\text{comp2}} - V_{\text{comp1}}$ | 0.1   |      |       | V             |
| UVS/SYN Threshold                      | $\text{UVS/SYN}_{\text{TH}}$ | Fault when below the threshold, positive and negative input  | 0.33  | 0.4  | 0.45  | V             |
| UVS/SYN Input Range                    | $V_{\text{UVS/SYN}}$         | Functional operation range, positive and negative input  | -0.5  |      | 4     | V             |
| ISNS Fault Threshold                   | $V_{\text{ISNSTH}}$          | Fault when below the threshold   | 90    | 110  | 130   | mV            |
| Over Current Threshold                 | $\text{OC}_{\text{TH}}$      | Upper threshold for ISNS input   | 580   | 630  | 680   | mV            |
| Short Circuit Threshold                | $\text{SC}_{\text{TH}}$      | Upper threshold for ISNS input   | 940   | 1000 | 1060  | mV            |

**ELECTRICAL CHARACTERISTICS**

Unless otherwise listed, the following specifications apply over the operating ambient temperature of  $-40^{\circ}\text{C} < \text{Temp} < 85^{\circ}\text{C}$ , and  $\text{VIN} = 7.5\text{V}$  to  $27\text{V}$ , except where otherwise noted and the following test conditions:  $\text{VIN} = 12\text{V}$ ,  $\text{C}_{\text{C}_R} = 330\text{pF}$ ,  $\text{R}_{\text{C}_R} = 15\text{k}\Omega$

| Parameters                    | Symbol               | Test Conditions/Comments   | MIN | TYP   | MAX | Units            |
|-------------------------------|----------------------|--|-----|-------|-----|------------------|
| Fault Count                   | FC                   | At clock frequency of AOUT, BOUT   |     | 256   |     | Count            |
| Fault reset Interval          | $F_{\text{RESET}_1}$ | Interval for resetting fault counter after POR, At clock frequency of AOUT, BOUT |     | 32768 |     | Count            |
| Fault reset Interval          | $F_{\text{RESET}_R}$ | Periodic Interval for resetting fault counter, At clock frequency of AOUT, BOUT  |     | 65536 |     | Count            |
| Fault Output Sinking Capacity | $F_{\text{SINK}}$    | $\text{V}_{\text{FAULT}} \leq 0.8\text{V}$ , $\text{TA} = 25^{\circ}\text{C}$    | 4   | 6     |     | mA               |
| Fault Output Open Impedance   | $R_{\text{F}}$       | When in open state   | 5   |       |     | $\text{M}\Omega$ |

**Bias & References**

|                            |                  |                                 |  |   |  |               |
|----------------------------|------------------|---------------------------------|--|---|--|---------------|
| Soft Start Charging Source | $I_{\text{SSC}}$ | C_B Charging source at start up |  | 2 |  | $\mu\text{A}$ |
|----------------------------|------------------|---------------------------------|--|---|--|---------------|

**Power-Up Sequencing**

|                   |        |           |  |       |  |       |
|-------------------|--------|-----------|--|-------|--|-------|
| Start up Time Out | TSTART | After POR |  | 32768 |  | Count |
|-------------------|--------|-----------|--|-------|--|-------|

**FUNCTIONAL PIN DESCRIPTION**

| Name     | Pin # | Description  |
|----------|-------|--|
| VIN      | 1     | Input voltage pin. A built-in regulator is connected to this pin to step down the input voltage to the internal operating voltage VDD. This pin can accept input voltage from 7.5V to 27V to provide the flexibility of interfacing with either 12V or 24V system supply. A low ESR decoupling capacitor of not less than $1\mu\text{F}$ should be connected from this pin to GND with low impedance traces.   |
| ENABLE   | 2     | Enable pin to control the on/off operation of the controller. A logic low signal $< 0.8\text{V}$ on this pin sets the controller in sleep mode to save energy, and a signal $> 1.7\text{V}$ activates the controller operation. The DC signal level on this pin also sets the drive mode of the controller. With $\text{VDD} = 5.25\text{V} \pm 5\%$ , when $1.7\text{V} < \text{V}_{\text{ENABLE}} < 2.8\text{V}$ the AOUT, BOUT signal is set in LLC resonant drive mode; when $3.2\text{V} < \text{V}_{\text{ENABLE}} < 3.7\text{V}$ the controller drives the power converter in normal PWM drive mode; and when $\text{V}_{\text{ENABLE}} > 4.3\text{V}$ the controller is set in synchronous LED drive mode.   |
| C_R      | 3     | Converter operating frequency programming terminal. A pull-up resistor from this pin to VDD and a capacitor connected from this pin to ground determines the operating frequency of the inverter.  |
| BRTA     | 4     | Terminal for programming the analog LED current setting. An analog signal is accepted from this pin to set the reference level for the LED current control loop.   |
| DIM      | 5     | PWM dimming control input. $\text{V}_{\text{DIM}} > 2\text{V}$ sets the dimming operation in continuous analog mode. A PWM signal of low level $< 0.5\text{V}$ and high level $> 2\text{V}$ will force the PWM dimming operation to follow the PWM signal directly. Input level $< 0.5\text{V}$ will stop the controller output.   |
| SST/BCOM | 6     | For PWM dimming brightness compensation and soft start. The elapsed dimming demand and the accumulated LED current over the active dimming period are compared at this pin. The comparison result is used to control the LED light output to exactly match the dimming demand with compensation for the distortion of the LED current during dimming operation. At start up this pin is connected to a $2\mu\text{A}$ charging current source to control the soft start process. An internal active pull down circuit is connected from this pin to COMP to force the COMP voltage rise slowly with the charge of the capacitor at this pin. Soft start completes when the voltage rises to $2.5\text{V}$ and the control enters normal operation mode. The $2\mu\text{A}$ charging source and the COMP pull down circuit are disconnected then, and this pin is connected to the brightness compensation circuit. |
| FAULT    | 7     | Fault indication pin with open drain output. Internally pulled down when an open LED string,   |



#### FUNCTIONAL PIN DESCRIPTION

| Name         | Pin #    | Description  |
|--------------|----------|--|
|              |          | severely shorted LED string, over voltage of the LED strings, or over current occurs. Once latched, the fault signal can only be reset by ENABLE or power recycling. The voltage level at this pin during normal operation also sets the operation mode of dimming control. When the voltage is above 3V the COMP signal is turned on and off by the digital dimming control signal and AOUT, BOUT and C_OUT are turned on and off accordingly by the COMP signal. When the voltage at the FAULT pin is below 3V the COMP signal is turned on and off by the control signal from the ACU_BRITE dimming control algorithm, and AOUT, BOUT and C_OUT are turned on and off accordingly by the COMP signal. The voltage level of this pin during normal operation can be set by an external resistive divider.  |
| UVS/SYN      | 8        | Sense for under voltage conditions. A threshold of 0.4V is set internally to compare the sense feedback signal to this pin when the LED strings are on. A fault will be declared if the sensed signal stays below the threshold over certain counts set by the internal circuitry. LED string current and voltage sense signals can be fed to this pin to detect open or short string conditions. When the controller is set in synchronous regulation mode UVS/SYN will receive the synchronization signal from the power supply to synchronize the switching frequency of AOUT and BOUT. An internal rectifier circuit is included to allow an AC input signal to be connected to this pin directly.   |
| VSNS         | 9        | Voltage sense input pin. The voltage signal on this pin feeds the over voltage detection circuit. A threshold of 2V is set internally for fault detection. When the voltage sense signal reaches the threshold of 2V, a clamping current source will be activated to pull down COMP signal to limit the sensed voltage. In the meanwhile, the fault monitoring circuit will start counting the accumulated fault duration and set up the fault flag when the fault count reaches pre-determined counts.  |
| ISNS         | 10       | Current sense input pin. A full wave rectifier circuit is built in to allow AC input to this pin. The regulation point at this pin is 421mV which is amplified by 4.75 times and then fed to the error amplifier to compare with a reference signal of 2V to regulate the LED current. This signal is also used to detect open LED, over current and short circuit conditions. The threshold for open LED is 110mV, the threshold of over current is 630mV, and the threshold for short circuit is 1000mV. A fault flag will be declared if ISNS signal stays below 110mV or above 630mV over defined counts, and the operation will be cut off immediately when ISNS signal goes above 1000mV.  |
| COMP         | 11       | Output of the error amplifier. The error amplifier is a Gm type that provides robust control behavior and simple compensation. The signal on this pin feeds to the PWM modulation circuit to control the drive output to regulate the LED current. At start up the voltage of this pin is controlled by the soft start circuit.  |
| C_OUT        | 12       | Gate signal to drive an additional MOSFET for LED current regulation. The signal is in synchronous with the C_R oscillator frequency and is leading edge modulated by the output of the error amplifier in LLC and synchronous regulation modes and trailing edge modulated in PWM half bridge drive mode. This signal can be used in combination with AOUT and BOUT to extend the regulation range in LLC operation mode or provide additional driving capabilities in synchronous regulation mode.   |
| AOUT<br>BOUT | 15<br>13 | Gate drive output. These driver outputs are capable of providing 0.8A source and sink current at nominal operating voltage. Dead time is inserted to prevent possible shoot through at full duty cycle when these signals are used for half bridge or full bridge driving. Internal pull down resistors of 20kΩ is provided at each pin. When the controller is in resonant drive mode AOUT and BOUT are driven to maximum duty and their switching frequency varies with COMP signal level; when the controller is in PWM drive mode these two outputs generate pulse width modulated drive signals at fixed frequency; and when the controller is in synchronous LED drive mode, UVS/SYN receives the synchronization signal, AOUT outputs a NFET drive signal in synchronous with the positive cycle of the UVS/SYN input and BOUT outputs a PFET drive signal in synchronous with the negative cycle of the UVS/SYN input to drive respective external power devices to control the LED current directly. Different from the PWM drive mode, the pulse width of AOUT and BOUT is leading edge modulated in synchronous drive mode. |
| GND          | 14       | Ground return of the on chip circuit. It is important to provide a low impedance ground plane to this pin and the signal control circuitry in PCB layout, and not let the ground return current of the   |

**FUNCTIONAL PIN DESCRIPTION**

| Name | Pin # | Description   |
|------|-------|---|
|      |       | inverter power circuit flow through the signal ground plane. Low ESR bypass capacitors for VDD and VDD should be connected with lowest possible impedance to this pin through the signal ground plane.  |
| VDD  | 16    | The operating voltage of the IC. A built-in regulator supplies a regulated 5.25V derived from VIN supply to this pin. A low ESR decoupling capacitor of not less than 1 $\mu$ F should be connected from this pin to GND with low impedance traces. |

**FUNCTIONAL BLOCK DIAGRAM**

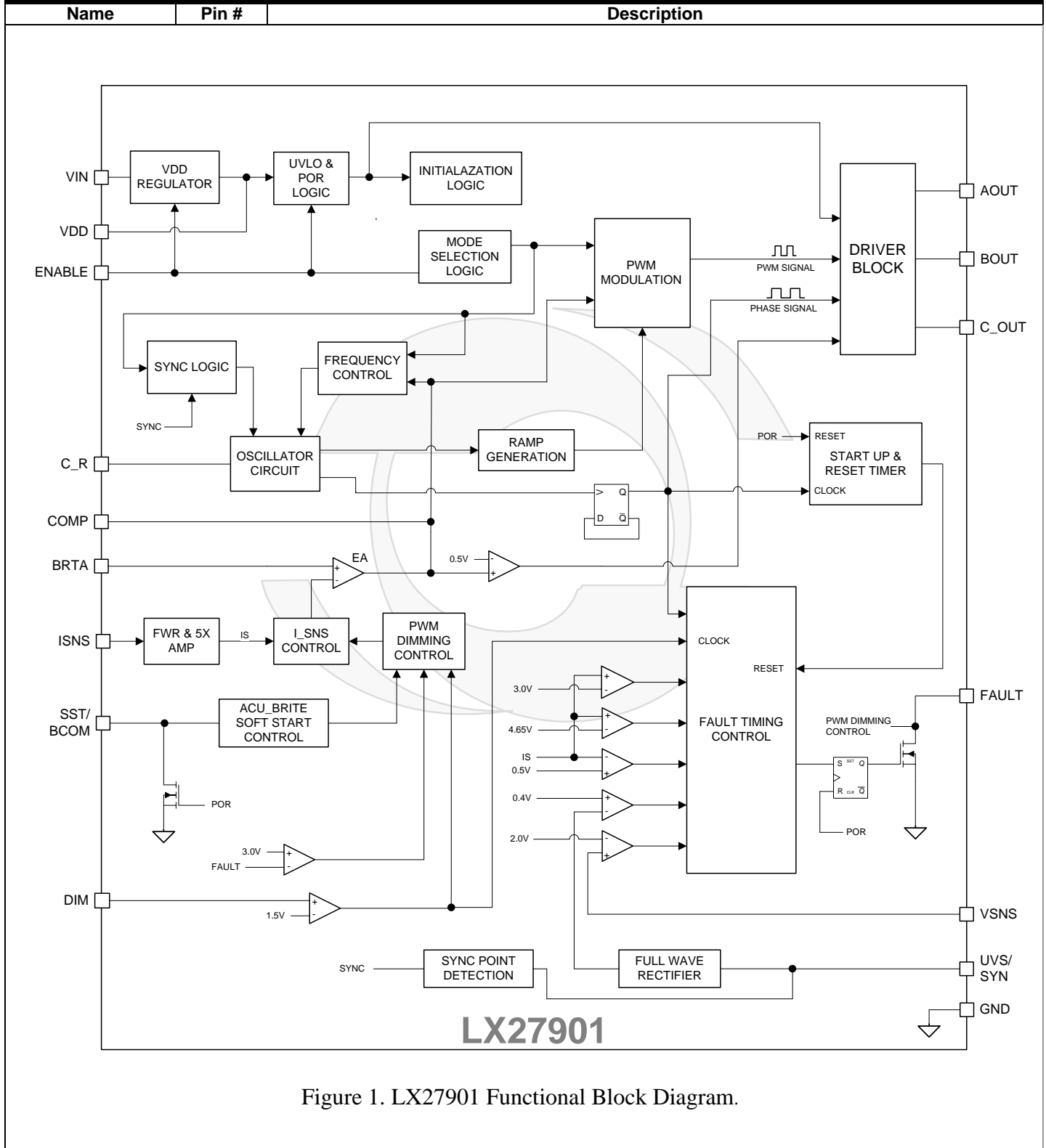
**FUNCTIONAL PIN DESCRIPTION**


Figure 1. LX27901 Functional Block Diagram.



### TYPICAL PERFORMANCE CHARACTERISTICS

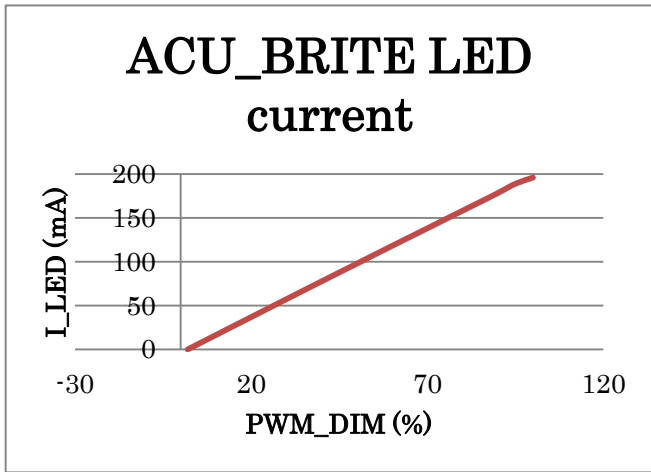


Figure 2

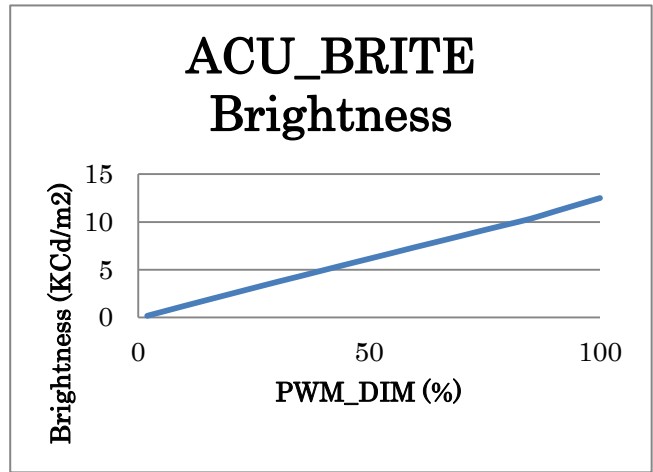


Figure 3

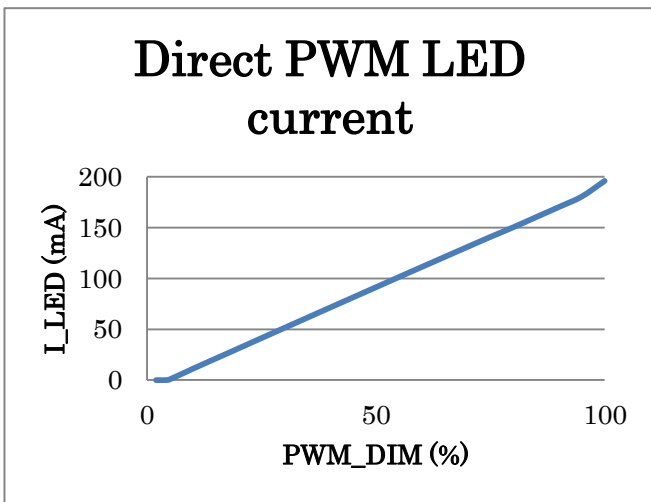


Figure 4

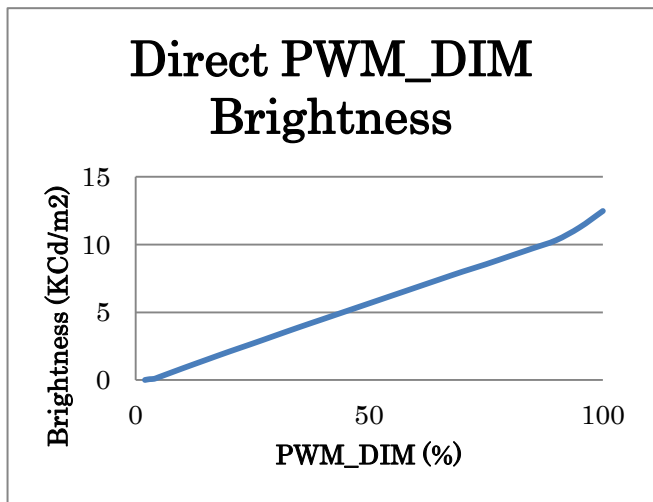


Figure 5

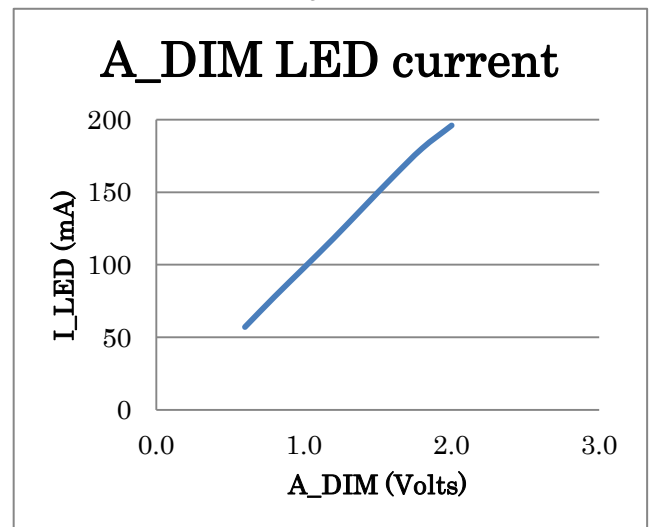


Figure 6

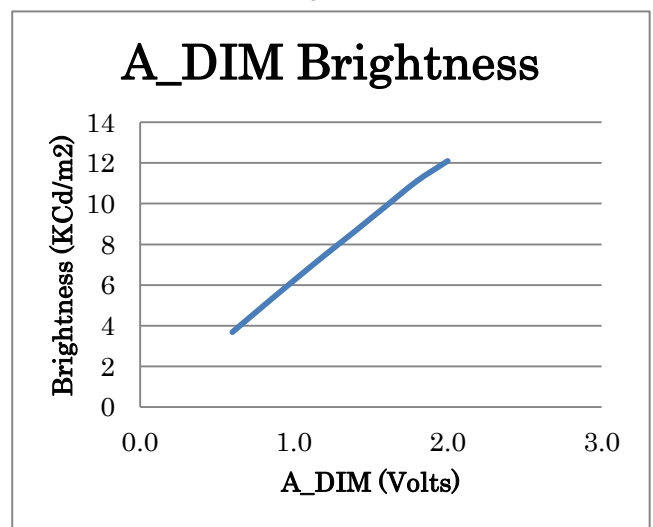


Figure 7



### TYPICAL PERFORMANCE CHARACTERISTICS

#### STARTUP WITH ENABLE LLC MODE

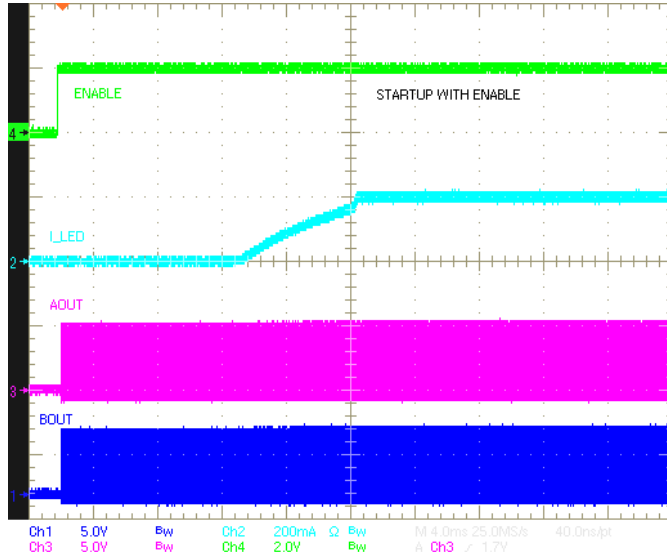


Figure 8  
Channel 1: BOUT, Channel 2: I\_LED  
Channel 3: AOUT, Channel 4: ENABLE

#### OUTPUT TIMING SYNC MODE

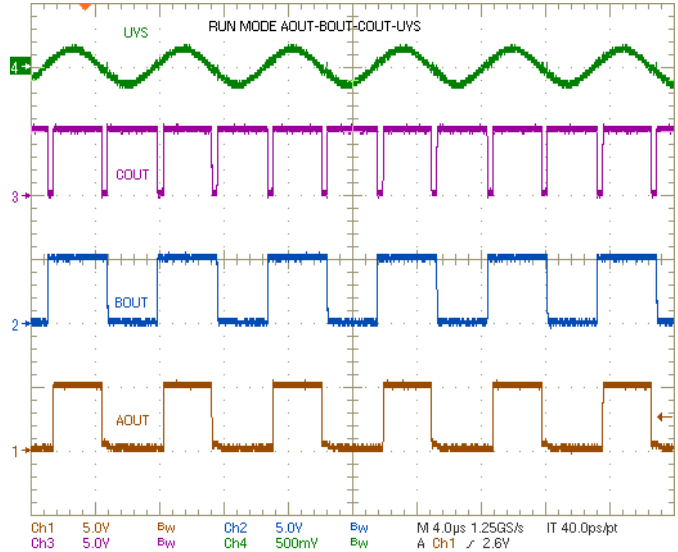


Figure 9  
Channel 1: AOUT, Channel 2: BOUT  
Channel 3: COUT, Channel 4: UVS

#### DIMMING SYNC MODE

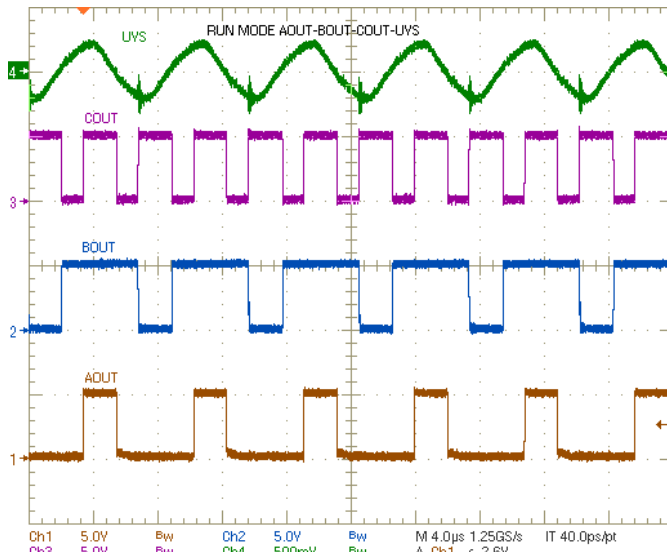


Figure 10  
Channel 1: AOUT, Channel 2: BOUT  
Channel 3: COUT, Channel 4: UVS

#### VSNS OV PROTECTION MODE

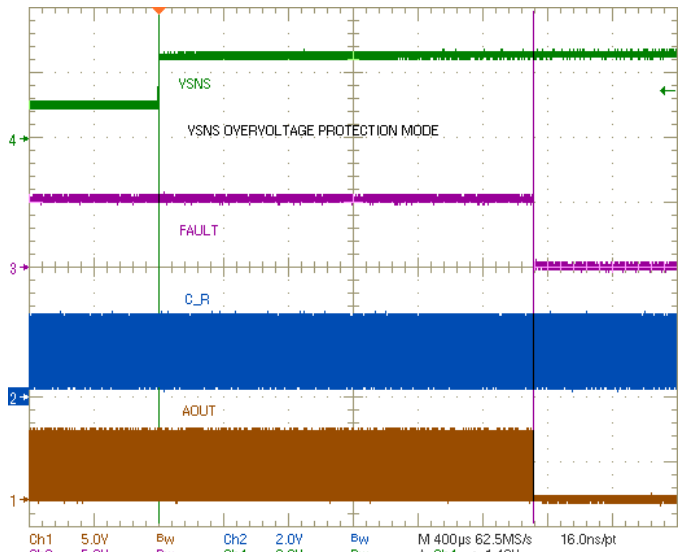


Figure 11  
Channel 1: AOUT, Channel 2: C\_R  
Channel 3: FAULT, Channel 4: VSNS





### TYPICAL PERFORMANCE CHARACTERISTICS

#### LLC DIMMING MODE

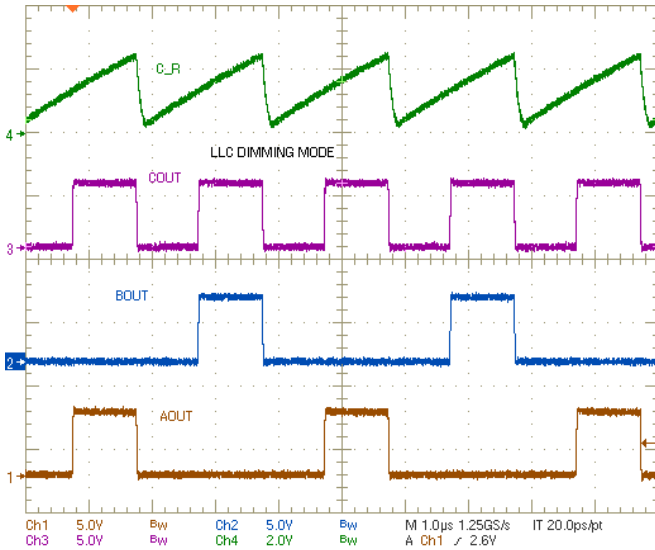


Figure 12  
Channel 1: AOUT, Channel 2: BOUT  
Channel 3: COUT, Channel 4: C\_R

#### PWM DIMMING MODE

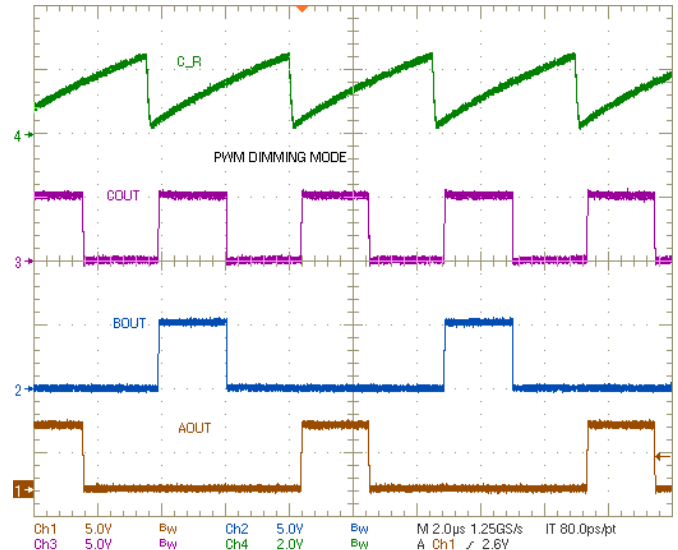


Figure 13  
Channel 1: AOUT, Channel 2: BOUT  
Channel 3: COUT, Channel 4: C\_R

#### ACU\_BRITE DIMMING MODE

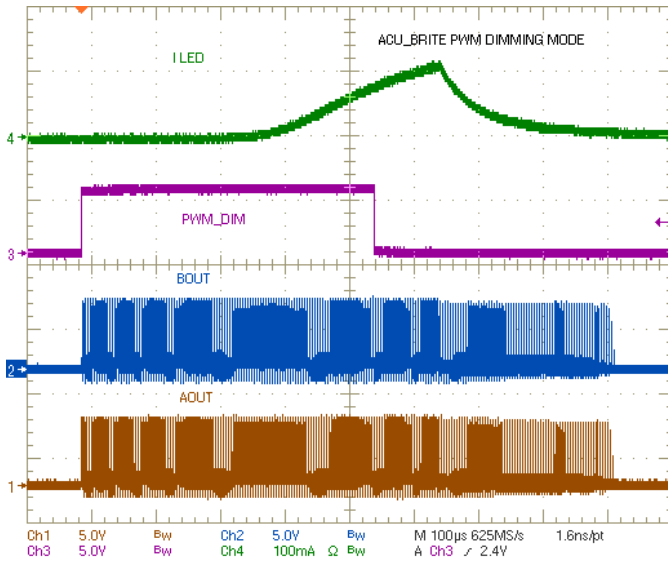


Figure 14  
Channel 1: AOUT, Channel 2: BOUT  
Channel 3: PWM\_DIM, Channel 4: ILED

#### DIRECT PWM DIMMING MODE

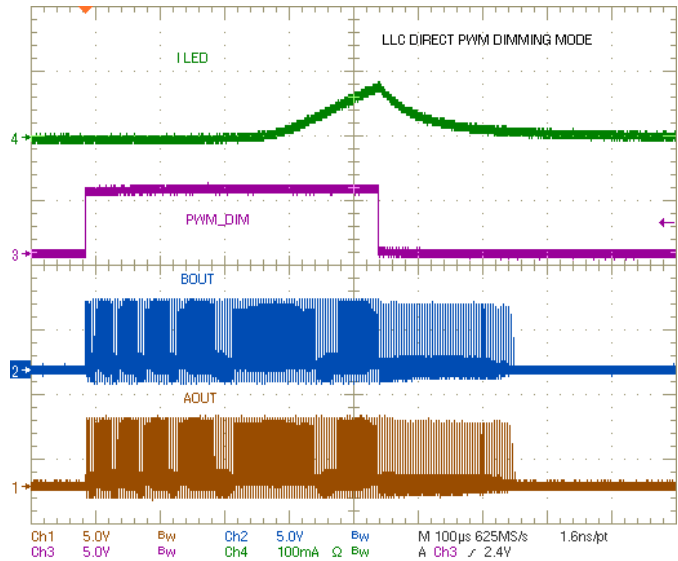


Figure 15  
Channel 1: AOUT, Channel 2: BOUT  
Channel 3: PWM\_DIM, Channel 4: ILED



### TYPICAL PERFORMANCE CHARACTERISTICS

#### ACU\_BRITE DIMMING MODE

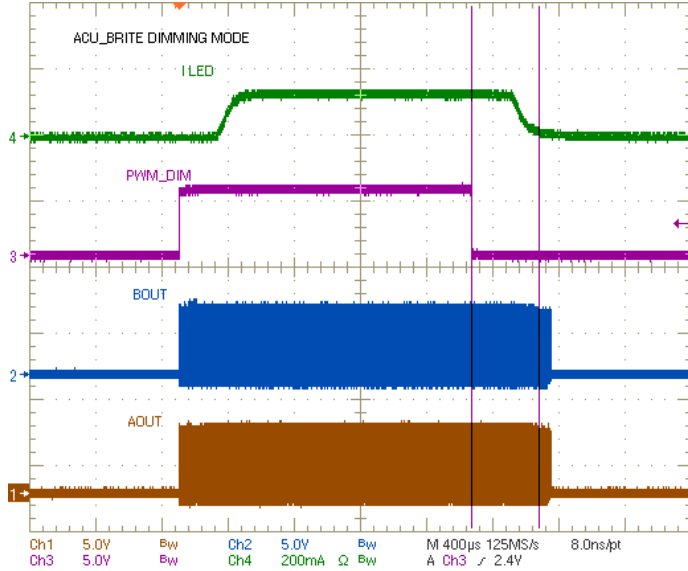


Figure 16

Channel 1: AOUT, Channel 2: BOUT  
Channel 3: PWM\_DIM, Channel 4: ILED

#### DIRECT PWM DIMMING MODE

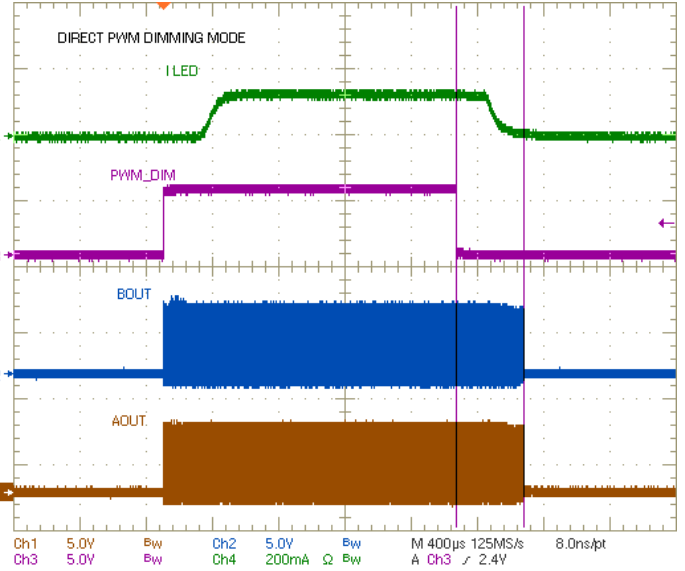


Figure 17

Channel 1: AOUT, Channel 2: BOUT  
Channel 3: PWM\_DIM, Channel 4: ILED



### TYPICAL APPLICATION SCHEMATIC

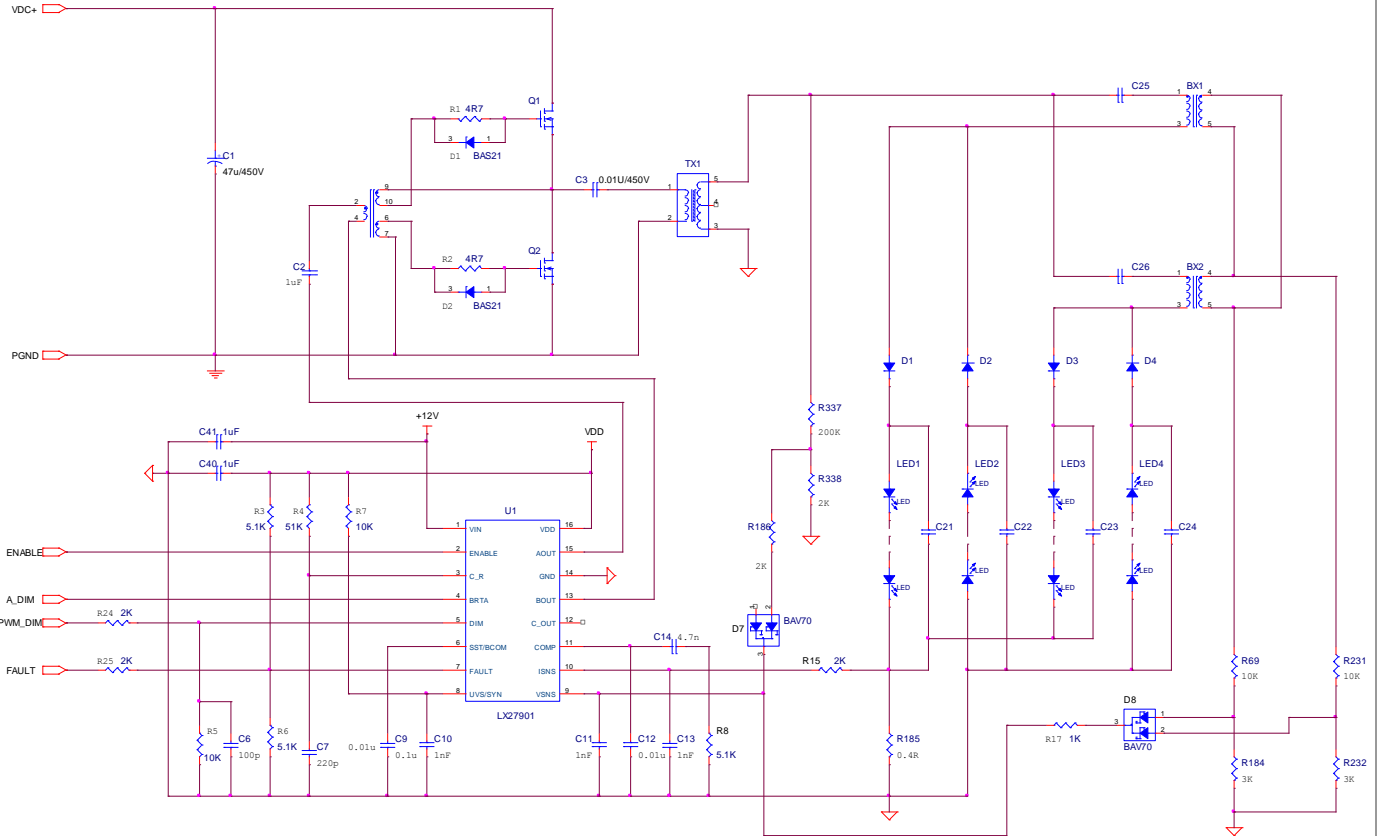


Figure 18  
 LLC CONTROL MODE

(The component values are for reference only, modifications may be necessary for a particular application requirement.)



### TYPICAL APPLICATION SCHEMATIC

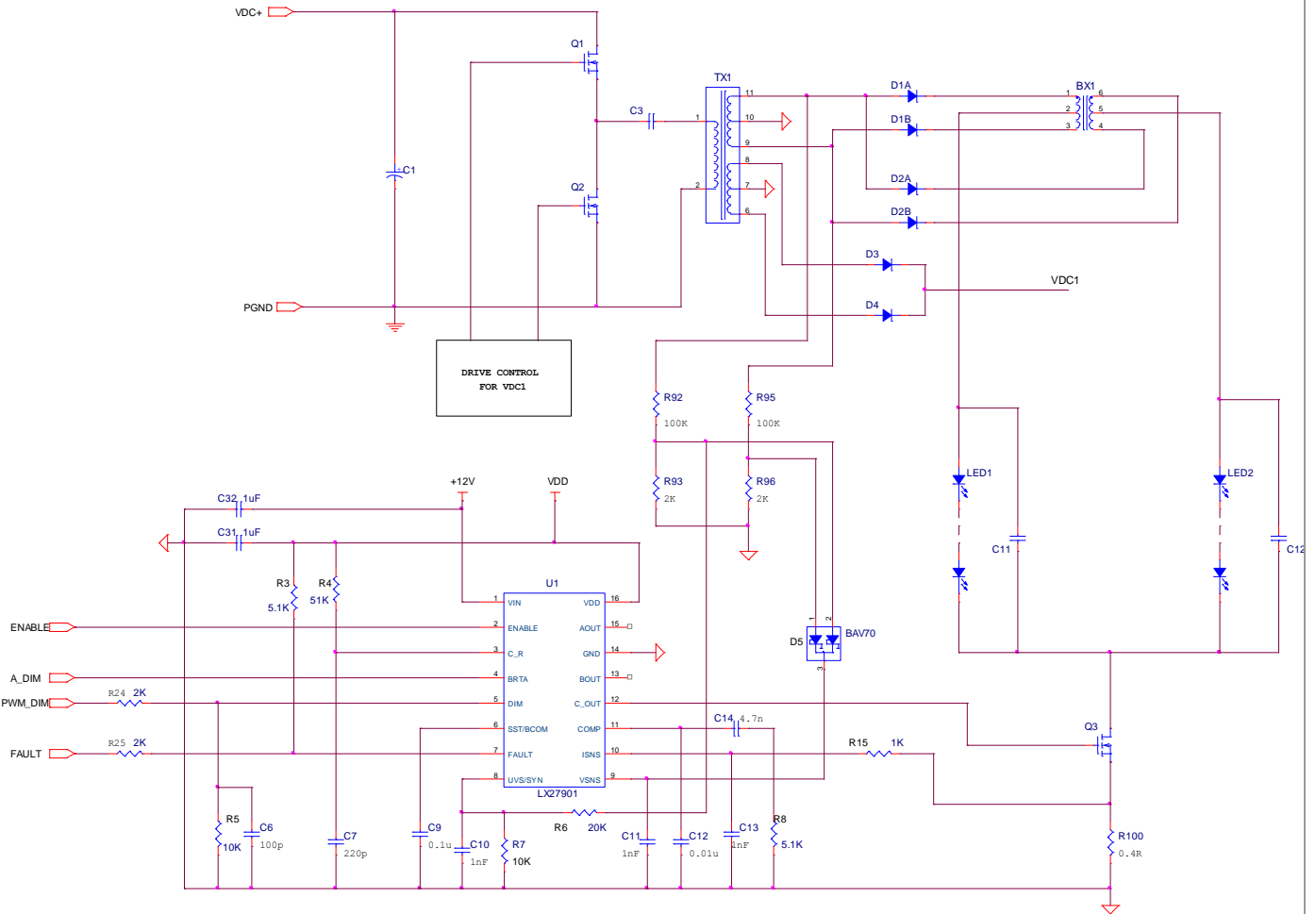


Figure 19  
**SYNCHRONOUS REGULATION MODE**

(The component values are for reference only, modifications may be necessary for a particular application requirement.)

**OPERATION DESCRIPTION****INTRODUCTION**

This section describes the operation of LX27901 LED drive controller. LX27901 is primarily designed for LIPS power systems for LED backlit LCD TV and other large screen CCFL backlight applications that addresses the need to drive a half bridge or full bridge inverter stage from the 400V PFC output across the safety isolation barrier. It provides an optimized low cost solution for such applications while providing a set of comprehensive control features to fully satisfy the technical requirements.

**1. SYSTEM OVERVIEW**

The system contains the following main function blocks:

- Power and Start-Up Logic
- Oscillator and Frequency Control Circuit
- Regulation Control Circuit
- Dimming Control Circuit
- Drive Control Circuitry
- Fault Detection and Protection Circuitry

The power and start-up logic provides regulated power to the on chip circuitry and controls the start-up sequencing, power on reset, and soft start operation etc. The oscillator and frequency logic generates the clock signals for the LLC and PWM operation and timing for the operation and protection. The regulation and dimming control logic handles the LED current regulation and dimming control operation with Microsemi's proprietary ACU\_BRITE technology to provide accurate brightness control with non-dissipative operation of the power devices. The drive control circuit converts the PWM signal from the regulation and control circuit to power drive signals to drive the external power devices of the power supply and LED string control. The fault detection and protection logic monitors the operation of the internal and external circuits and provides fault warning and protection for the system.

**2. POWER CONTROL AND START UP**

The LX27901 has a built in regulator to step down the input voltage VIN to a regulated 5.25V supply VDD to support the on chip circuitry. The regulator is controlled by the ENABLE signal and is only activated when ENABLE voltage goes above its logic threshold and thus minimizing the power consumption at sleep mode. An UVLO circuit is employed to monitor the VDD voltage. The UVLO circuit releases the lock out function when VDD reaches its rising threshold and initiates the Power On Reset (POR) signal.

The POR signal initializes the whole control circuitry by resetting the counters, registers, fault latch, setting the analog signals such as the SST/BCOM voltage to pre-determined initial values, while holding off the output signals to pre-determined inactive states. After the preset delay time the POR signal is released and the controller operation starts.

**3. OSCILLATOR AND FREQUENCY CONTROL**

The system has a built in switching frequency oscillator to provide ramp signal and clock signal to the power supply LLC and PWM control logic and internal counter-timer etc. A resistor and a capacitor is required to connect between VDD and the switching frequency oscillator programming terminal C\_R and from C\_R to ground respectively to set the oscillating frequency. A controlled charging current source is also provided internally to the C\_R pin to adjust the oscillator frequency when the ENABLE voltage level is set in LLC resonance control mode. When the ENABLE voltage level is set in PWM mode, the current source is disconnected and the oscillator returns to the free run frequency set by the external RC components.

**4. REGULATION CONTROL**

The regulation circuit controls the LED current through a closed loop regulation. The LED current is sensed and fed to the ISNS pin as a feedback signal where it is regulated by an internal error amplifier to match the current reference threshold. The error amplifier is a Gm type which is essentially a voltage controlled current source. The output signal feeds the PWM control circuit to adjust the PWM drive signals to control the power device operation of the external power circuit. The output of the error amplifier is also connected to COMP pin to allow the user to adjust the compensation for the control loop with external components connected to this pin. Three power supply control modes are incorporated into the Controller operation: LLC Resonant control mode, PWM control mode, and synchronous regulation mode. In LLC resonant mode the PWM drive output signals AOUT and BOUT remain at full duty cycle, and the output signal from the error amplifier controls the internal charging current source at C\_R pin to adjust the switching frequency of AOUT and BOUT to regulate the LED current. Note that in this mode the operating frequency of the drive signals should be always higher than the resonance frequency of the external power circuit in order to maintain stable regulation of the output.

**OPERATION DESCRIPTION**

In PWM control mode the internal current source at C\_R pin is disconnected and AOUT and BOUT signals remain at the fixed frequency set by the RC components at C\_R pin, and the LED current is regulated by adjusting the pulse width of the AOUT and BOUT signals. In synchronous regulation mode the synchronization signal from the power supply is received from UVS/SYN pin and AOUT and BOUT output drive signals in synchronous with the synchronization signal to drive respective external switches in series with the LED strings to control the LED current. In this mode AOUT and BOUT are leading edge modulated PWM drive signals controlled by the closed current loop from ISNS feedback. The three control modes are selectable by the voltage level of ENABLE signal. With  $V_{DD}=5.25V\pm 5\%$ , when  $1.7V < V_{ENABLE} < 2.8V$  the controller is in LLC resonant drive mode; when  $3.2V < V_{ENABLE} < 3.7V$  the controller drives the power supply in PWM drive mode; and when  $V_{ENABLE} > 4.3V$  the controller drives the external device in synchronous regulation mode. Note that when the Enable voltage is reached to 1.7V, it operates at LLC mode.

**5. DIMMING CONTROL**

The LX27901 supports external burst dimming and analog dimming functions. In external digital dimming mode a dimming pulse train is supplied to DIM pin and the dimming operation follows the input pulse train directly. It is recommended that the high state of the pulse train should be higher than 2V and the low state should be lower than 0.5V. This signal is compared with an internal DC level of 1.5V to generate an internal PWM pulse train to control the burst dimming operation.

A unique feature called ACU\_BRITE is incorporated to compensate the LED current error by digital dimming duty adjustment. A capacitor from SST/BCOM pin to ground provides an integration function for such control. A controlled charging current source and a controlled discharging current source are connected internally to the SST/BCOM pin. The charging current source is linearly proportional to the internal current regulation reference and turned on and off by the internal digital dimming signal. The discharging current source is proportional to the ISNS signal at the same ratio as the charging source to the internal reference. At power on reset the SST/BCOM capacitor is discharged to zero and the capacitor is used for soft start operation. When the capacitor voltage reaches 2.5V it switches over to ACU\_BRITE dimming control function. The voltage of SST/BCOM is fed to a comparator and compared with a threshold level of 2.5V. When  $V_{SST/BCOM}$  is greater than 2.5V, the LED current is turned on, and when  $V_{SST/BCOM}$  is lower than 2.5V, the LED current is turned off.

With such control mechanism the integration of the LED current always matches the integration of its reference over the digital dimming operation to yield an accurate brightness control. This feature essentially enables the control of dimming operation by turning on and off the power supply directly without losing dimming accuracy, instead of putting an additional control device in series with the LED string to control the LED on/off. The LED current distortion at the rising and falling edge of the digital dimming operation is accurately compensated by the dimming duty adjustment, the no load power supply losses at LED off state are eliminated, and the serial control device is removed.

**6. DRIVE CONTROL CIRCUIT**

The drive control circuit converts the PWM signal from the regulation and control circuit to the drive output signals AOUT, BOUT and C\_OUT to drive the external power devices for the power supply and LED string control. The signals from AOUT and BOUT are 180° out of phase. When the controller is in LLC resonant mode AOUT and BOUT remain at full duty, and their switching frequency varies with the COMP signal level to adjust the power supply output. When the controller is in the PWM control mode AOUT and BOUT remain at a fixed switching frequency but their duty cycle varies with the COMP signal level. When in synchronous regulation mode AOUT outputs a NFET drive signal in synchronous with the positive cycle of the synchronization signal from UVS/SYN pin, and BOUT outputs a PFET drive signal in synchronous with the negative cycle of the synchronization signal from UVS/SYN to drive the external devices. In this mode the AOUT and BOUT signal is a leading edge modulated PWM signal with their falling edge in synchronous with the zero crossing point of the synchronization signal to minimize their turn off transient and their pulse width is controlled by the closed current loop from ISNS feedback. The driving capacity of AOUT and BOUT is 0.8A in both the sourcing and sinking mode.

The signal from C\_OUT provides the user additional control for LED current regulation. The signal is in synchronous with the C\_R oscillator frequency and is leading edge modulated by the output of the error amplifier in LLC and synchronous regulation modes, and trailing edge modulated in PWM half bridge drive mode. This signal can be used in combination with AOUT and BOUT to extend regulation range in LLC operation mode or provide additional driving capabilities in synchronous regulation mode.



#### OPERATION DESCRIPTION

##### 7. SOFT START

Soft start is accomplished by internal circuitry in combination with the SST/BCOM capacitor charging control. At power on the SST/BCOM capacitor is discharged to zero during POR. When the operation commences following POR the SST/BCOM pin is disconnected from the dimming control circuit and a small soft start current source of 2  $\mu$ A is turned on to charge the SST/BCOM capacitor slowly.

The voltage of the SST/BCOM capacitor pulls down the COMP signal through the soft start circuit to force the  $V_{COMP}$  signal to rise slowly together with it. During this course the voltage amplitude of SST/BCOM is monitored. When the SST/BCOM signal rises to 2.5V, the soft start current source is turned off and the SST/BCOM pin switches over to the internal dimming control circuit. The capacitor at SST/BCOM is charged and discharged by the ACU\_BRITE brightness compensation circuit and its voltage is compared with a 2.5V reference to turn on and off the AOUT, BOUT and C\_OUT signals while the COMP signal resumes its role in the regulation function. During start up a timer-counter circuit is also furnished to monitor the system operation. If the ISNS signal does not reach 100mV after the counter reaches the full count of 32k (15 bit) clock cycles, the start-up is considered failed and a fault flag is raised by pulling down the FAULT pin signal.

##### 8. FAULT DETECTION AND PROTECTION

The following system operating conditions are monitored with fault report or protection actions:

- a) Open LED string
- b) Short LED string
- c) Power supply failure
- d) Over voltage
- e) Over current

The above fault conditions are monitored from the ISNS, VSNS and UVS/SYN inputs. The ISNS signal is used to monitor open LED, power supply failure and over current conditions. Open LED detection is disabled during start up until the 15 bit counter times out. After the counter time out if ISNS signal is still below 100mV while the LED is on, it indicates an open LED or power supply failure condition.

A fault counter will start to count the fault. When the counter reaches the full count of 256, a fault condition is confirmed and the FAULT pin is pulled to low state to indicate a fault condition.

The fault counter is incremented by a clock at the same frequency as AOUT, BOUT and reset at 32768 clock pulses and after that it periodically reset at an interval of 65536 clock pulses.

In addition, during the interval if there is any single occurrence of  $ISNS > 110mV$  it will reset the fault counter and the fault counting has to start all over again. Such reset mechanism guarantees reliable fault detection and prevents noise triggered false fault reporting. The ISNS signal is also used to monitor over current and short circuit conditions.

A typical threshold of 630mV is set for over current detection and a typical threshold of 1000mV is set for short circuit detection. The fault counter will start counting when  $ISNS > 630mV$  occurs and reports a fault when the counter reaches full count of 256. The Fault counter is reset at 32768 clock cycle and then periodical reset at every 65536 clock cycle interval is also employed.

In addition, a time delay circuit, similar to a one shot, is employed to hold the over current status for about 50 $\mu$ s. The fault counter will be reset if the over current condition does not persist when the elapsed holding time is over. When ISNS signal exceeds 1000mV typically it will be recognized as a short circuit. The output signal will be shut off immediately with a fault flag raised. The short circuit detection is active all the time after POR release.

The VSNS signal is used to limit and monitor over voltage condition. When the voltage sense signal reaches the threshold of 2V, a clamping current source will be activated to pull down COMP signal to limit the sensed voltage, and when the comp voltage decreases below 0.5V, then it disables the gate-drive outputs. It provides the regulation operation to keep the output voltage at VSNS 2V.

The UVS/SYN signal provides further means for fault detection. A threshold of 0.4V is set internally for the UVS/SYN signal. When  $UVS/SYN < 0.4V$  occurs, the fault counter also starts counting and reports a fault condition when the counter reaches full count.

The counter is reset at 32768 clock cycle and then periodical reset at every 65536 clock cycle interval also applies to the UVS/SYN fault count. Similarly a time delay circuit is also employed to hold the over voltage status for about 50 $\mu$ s. The fault counter will be reset if the over current condition does not persist when the elapsed holding time is over.



### APPLICATION INFORMATION

#### SETTING OPERATING FREQUENCY

The switching frequency of AOUT and BOUT is programmed with the external capacitor and resistor,  $R_{C\_R}$  and  $C_{C\_R}$ .

$$f \approx \frac{374200}{R_{C\_R}^{0.94} \cdot C_{C\_R}^{0.91}}$$

$f_{SW}$  is the switching frequency in kHz,  $R_{C\_R}$  is in k $\Omega$ , and  $C_{C\_R}$  is in pF. For most applications, The switching frequency (minimum operating frequency in LLC Mode) is set at less than 150kHz. Normally  $C_{C\_R}$  can be chosen from 220pF to 470pF, and the value of  $R_{C\_R}$  can also be used to adjust the frequency control range in LLC mode. In LLC mode, maximum operating frequency is approximately  $f_{max} \approx 0.84 \times (0.0452 \cdot R_{C\_R} + 0.92) \times f_{min}$ , and the ratio  $f_m = f_{max}/f_{min}$ , and the operating frequency at arbitrary  $V_{comp}$  voltage can be expressed as  $f \approx f_{min} \{0.2(6f_m - 1) - 0.4(f_m - 1)V_{comp}\}$

#### SETTING COMP PIN CAPACITOR

An external capacitor  $C_{COMP}$  is connected from this pin to ground to adjust loop response of the inverter module. The error amplifier is a GM type that provides robust control behavior and simple compensation. The ideal current error amplifier compensation depends on the dimming mode operation range. If minimal dimming is required by the application the loop response can be slower, but for wide range digital dimming it must be fast enough to allow the lamp current to get to full amplitude within a few current cycles.

If value of  $C_{COMP}$  is small the gain will be increased and may result in overshoot, and the loop could become unstable. However as the capacitor value is increased it will reduce the gain and the loop response may be too slow. Therefore it is necessary to choose an optimal value, typical recommended values range from 1nF to 10nF, but should be adjusted depending on the application requirements.

#### VIN, VDD BYPASS CAPACITOR

The LX27901 has internal Low Dropout Regulator to generate an accurate 5V supply for the internal control circuitry. In order to have stable operation, it is required to provide bypass capacitor with low ESR between both VIN and VDD and ground. It is recommended to use a capacitance of not less than 1 $\mu$ F for VIN and 1 $\mu$ F for VDD.

#### LAYOUT GUIDELINES

It is important to have a good PCB layout to achieve stable operation. Especially, high voltage section and the power switching section of the circuit layout require particular attention. High voltage section layout also needs to be planned carefully to meet Safety requirement as well as proper isolation from the control circuit. Following are guidelines for inverter PCB layout

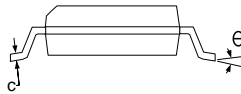
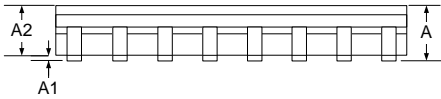
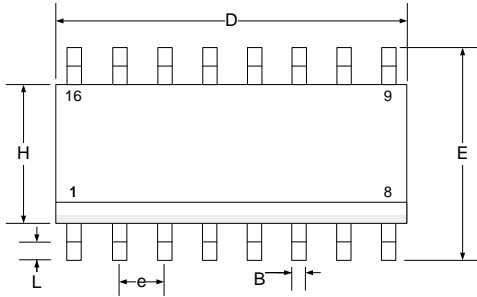
- 1) Use a star-ground connection for analog and power ground. Analog ground should be isolated from power ground except one connection point, GND pin.
- 2) Route high speed digital signal traces away from sensitive analog signals.
- 3) Place decoupling cap as close to related pin as possible.
- 4) Make shortest and direct connection from feedback sources.
- 5) Keep short and wide for high current signal paths especially ground.
- 6) Make trace as thick as possible
- 7) Route current sense and voltage divider traces away from high voltage field.





### PACKAGE DIMENSIONS

#### D 16-Pin Plastic Narrow Body SOIC



| DIM | MILLIMETERS |       | INCHES    |       |
|-----|-------------|-------|-----------|-------|
|     | MIN         | MAX   | MIN       | MAX   |
| A   | 1.35        | 1.75  | 0.053     | 0.069 |
| A1  | 0.10        | 0.25  | 0.004     | 0.010 |
| A2  | 1.25        | 1.52  | 0.049     | 0.060 |
| b   | 0.33        | 0.51  | 0.013     | 0.020 |
| c   | 0.19        | 0.25  | 0.007     | 0.010 |
| D   | 9.78        | 10.01 | 0.385     | 0.394 |
| E   | 5.79        | 6.20  | 0.228     | 0.244 |
| e   | 1.27 BSC    |       | 0.050 BSC |       |
| H   | 3.81        | 4.01  | 0.150     | 0.158 |
| L   | 0.40        | 1.27  | 0.016     | 0.050 |
| Θ   | 0           | 8     | 0         | 8     |
| *LC |             | 0.10  |           | 0.004 |

\*Lead Coplanarity

#### Note:

- Controlled dimensions are in mm, inches are for reference only.
- Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm (.006") on any side. Lead dimension shall not include solder coverage.



#### NOTES

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