ABSOLUTE MAXIMUM RATINGS

$\overline{OFF}$, DR1, DR2 to GND ....-0.3V to +6V
IN1, IN2/3, IN4/5, DIN (SDA) to GND ....-0.3V to +6V
SCLK (SCK), BP, $\overline{ON}$ to GND ....-0.3V to +6V
$\overline{RSO}$, ONO to GND ....-0.3V to (V_{OUT1} + 0.3V)
PGND to GND ....±0.3V
OUT1, $\overline{CS}$ (AS) to GND ....-0.3V to (V_{IN1} + 0.3V)
OUT2, OUT3 to GND..............................-0.3V to ($V_{IN2/3}$ + 0.3V)
OUT4, OUT5 to GND..............................-0.3V to ($V_{IN4/5}$ + 0.3V)
Continuous Sink Current
DR1, DR2..100mA_{RMS}
$\overline{RSO}$..25mA
Continuous Power Dissipation (T_A = +70°C)
20-Pin TQFN (derate 33.8mW/°C above +70°C) 2W
20-Pin TSSOP (derate 37.7mW/°C above +70°C) 2W
Operating Temperature Range ....-40°C to +85°C
Junction Temperature...+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

-ELECTRICAL CHARACTERISTICS

(V_{IN1} = $V_{IN2/3}$ = $V_{IN4/5}$ = $V_{SCLK\ (SCK)}$ = $V_{DIN\ (SDA)}$ = $V_{\overline{CS}\ (AS)}$ = $V_{\overline{OFF}}$ = 3.6V; $\overline{ON}$ = GND = PGND = 0; RSO, ONO, DR1, DR2 = open; BP bypassed with 0.01µF, OUT1 bypassed with 4.7µF; OUT2, OUT3, OUT4, OUT5 bypassed with 2.2µF; OUT1–5 set to 2.98V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IN1, IN2/3, IN4/5 Operating Voltage			2.5		5.5	V
Undervoltage Lockout IN1	V_{UVLO-1}	IN1 rising edge	2.10	2.30	2.45	V
Undervoltage Lockout IN2/3	$V_{UVLO-2/3}$	IN2/3 rising edge	2.10	2.30	2.45	V
Undervoltage Lockout IN4/5	$V_{UVLO-4/5}$	IN4/5 rising edge	2.10	2.30	2.45	V
Power-On Reset Threshold		IN1 falling edge	0.9		2.1	V
Supply Current in Shutdown	I_{SHDN}	$\overline{OFF}$ = 0, $\overline{ON}$ = IN1		1	10	µA
Supply Current (Standby)	I_{ON}	OUT1 ON, other regulators OFF I_{OUT1} = 0		113	230	µA
Supply Current (All Outputs On)		All regulators ON, $I_{OUT\_}$ = 0		367	680	µA
BP Voltage		I_{BP} ≤ 1nA	1.231	1.250	1.269	V
BP Supply Rejection		2.5V ≤ V_{IN1} ≤ 5.5V		0.2	5	mV
OUT1 REGULATOR						
Output Accuracy		I_{OUT1} = 70mA (Note 3)	-2		2	%
Output Accuracy (Line and Load)		1mA ≤ I_{OUT1} ≤ 300mA, 2.5V ≤ V_{IN1} ≤ 5.5V, V_{OUT1} = 1.8V (Note 3)	-3		3	%
Nominal Voltage Adjust Range		32 steps through serial interface; Tables 2, 3	1.8		3.3	V
Dropout Voltage		I_{OUT1} = 1mA (Notes 1, 3)		1		mV
		I_{OUT1} = 200mA (Notes 1, 3)		73	125	
Load Regulation		0.1mA ≤ I_{OUT1} ≤ 300mA		-0.003		%/mA
Line Regulation		2.5V ≤ V_{IN1} ≤ 5.5V, V_{OUT1} = 1.8V (Note 3)	-0.15	-0.03	0.11	%/V
Current Limit			320	500	850	mA
Output-Discharge Switch Resistance in Shutdown		Regulator output turned off		25	300	Ω
OUT1 Reset Threshold		OUT1 rising and falling (MAX1798/MAX1799)	-9.5	-7.5	-5.5	%
		OUT1 rising and falling (MAX1798A/MAX1799A)	-15	-13	-11	
Output Voltage Noise		f = 10Hz to 100kHz, C_{OUT} = 4.7µF		45		$µV_{RMS}$

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN1} = $V_{IN2/3}$ = $V_{IN4/5}$ = $V_{SCLK\ (SCK)}$ = $V_{DIN\ (SDA)}$ = $V_{\overline{CS}\ (AS)}$ = $V_{\overline{OFF}}$ = 3.6V; $\overline{ON}$ = GND = PGND = 0; RSO, ONO, DR1, DR2 = open; BP bypassed with 0.01µF, OUT1 bypassed with 4.7µF; OUT2, OUT3, OUT4, OUT5 bypassed with 2.2µF; OUT1–5 set to 2.98V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUT2–5 REGULATORS						
Output Accuracy		$I_{OUT\_}$ = 50mA (Note 3)	-2		2	%
Output Accuracy (Line and Load)		1mA ≤ $I_{OUT\_}$ ≤ 150mA, 2.5V ≤ $V_{IN\_}$ ≤ 5.5V, $V_{OUT\_}$ = 1.8V (Note 3)	-3		3	%
Nominal Voltage Adjust Range		32 steps through serial interface; Tables 2, 3	1.8		3.3	V
Dropout Voltage		$I_{OUT\_}$ = 1mA (Notes 1, 3)		1		mV
		$I_{OUT\_}$ = 100mA (Notes 1, 3)		50	100	
Load Regulation		1mA ≤ $I_{OUT\_}$ ≤ 150mA		-0.005		%/mA
Line Regulation		2.5V ≤ $V_{IN\_}$ ≤ 5.5V, $V_{OUT\_}$ = 1.8V (Note 3)	-0.15	-0.02	0.11	%/V
Current Limit			160	250	500	mA
Output-Discharge Switch Resistance		Regulator output turned off		110	300	Ω
Output Voltage Noise		f = 10Hz to 100kHz, C_{OUT} = 2.2µF		45		$µV_{RMS}$
LOGIC AND CONTROL INPUTS ($\overline{ON}$, $\overline{OFF}$, $\overline{RSO}$, DIN (SDA), SCLK (SCK), $\overline{CS}$ (AS))						
Reset Timer			140	235	430	ms
Watchdog Timer			35	60	110	ms
OUT1 Shutdown Timer (MAX1798A/MAX1799A only)			175	295	540	ms
Input Low Level	V_{IL}				0.4	V
Input High Level	V_{IH}		1.6			V
SDA Output Low Level (MAX1799 only)		$I_{DIN\ (SDA)}$ = 3mA			0.4	V
		$I_{DIN\ (SDA)}$ = 6mA			0.6	
$\overline{OFF}$ Pulldown Resistance		$\overline{OFF}$ = 5.5V	80	155	360	kΩ
ONO Output Low Level		I_{ONO} = 1mA		0.05	0.5	V
ONO Output High Level		I_{ONO} = -1mA	V_{OUT1} - 0.5			V
$\overline{RSO}$ Output Low Level		I_{RSO} = 1mA, V_{IN1} = 1V			0.5	V
$\overline{RSO}$ Output High Level (Internal Pullup Resistor)		I_{RSO} = 0	V_{OUT1} - 0.5			V
$\overline{RSO}$ Reset Resistance		$\overline{RSO}$ = 2.48V	9	14	19	kΩ
DR1, DR2 Output Low Level		I_{DR1} = I_{DR2} = 100mA (Note 3)		0.2	0.5	V
DR1, DR2 OFF Current (Leakage)	I_{OFF}	V_{DR1} = V_{DR2} = 5.5V	-1		1	µA
THERMAL SHUTDOWN						
Threshold				160		°C
Hysteresis				10		°C

CDMA Cellular/PCS System Power Supplies

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN1} = $V_{IN2/3}$ = $V_{IN4/5}$ = $V_{SCLK\ (SCK)}$ = $V_{DIN\ (SDA)}$ = $V_{\overline{CS}\ (AS)}$ = $V_{\overline{OFF}}$ = 3.6V; $\overline{ON}$ = GND = PGND = 0; RSO, ONO, DR1, DR2 = open; BP bypassed with 0.01µF, OUT1 bypassed with 4.7µF; OUT2, OUT3, OUT4, OUT5 bypassed with 2.2µF; OUT1–5 set to 2.98V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I²C (SMB) TIMING (MAX1799/MAX1799A)						
Clock Frequency	SCK				400	kHz
Bus-Free Time Between START and STOP	t_{BUF}		1.3			µs
Hold Time Repeated START Condition	t_{HD_STA}		0.6			µs
SCK Low Period	t_{LOW}		1.3			µs
SCK High Period	t_{HIGH}		0.6			µs
Setup Time Repeated START Condition	t_{SU_STA}		0.6			µs
Data Hold Time	t_{HD_DAT}		0			µs
Data Setup Time	t_{SU_DAT}		100			ns
Maximum Pulse Width of Spikes that Must Be Suppressed by the Input Filter of Both SDA and SCK Signals	t_{SP}			50		ns
Setup Time for STOP Condition	t_{SU_STO}		0.6			µs
SPI TIMING (MAX1798/MAX1798A)						
SCLK Clock Frequency	f_{SCLK}				2	MHz
SCLK Low Period	t_{cl}		125			ns
SCLK High Period	t_{ch}		125			ns
Data Hold Time	t_{HD_DAT}		0			ns
Data Setup Time	t_{SU_DAT}		125			ns
$\overline{CS}$ Assertion to SCLK Rising Edge Setup Time	t_{CSS}		200			ns
$\overline{CS}$ Deassertion to SCLK Rising Edge Setup Time	t_{CS1}		200			ns
SCLK Rising Edge to $\overline{CS}$ Deassertion	t_{CSH}		200			ns
SCLK Rising Edge to $\overline{CS}$ Assertion	t_{CSO}		200			ns
$\overline{CS}$ High Period	t_{CSW}		300			ns

ELECTRICAL CHARACTERISTICS

(V_{IN1} = $V_{IN2/3}$ = $V_{IN4/5}$ = $V_{SCLK\ (SCK)}$ = $V_{DIN\ (SDA)}$ = $V_{\overline{CS}\ (AS)}$ = $V_{\overline{OFF}}$ = 3.6V; $\overline{ON}$ = GND = PGND = 0; RSO, ONO, DR1, DR2 = open; BP bypassed with 0.01µF, OUT1 bypassed with 4.7µF; OUT2, OUT3, OUT4, OUT5 bypassed with 2.2µF; OUT1–5 set to 2.98V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
IN1, IN2/3, IN4/5 Operating Voltage		(Note 1)		2.5		5.5	V
Undervoltage Lockout IN1	V_{UVLO-1}	IN1 rising edge		2.10		2.45	V
Undervoltage Lockout IN2/3	$V_{UVLO-2/3}$	IN2/3 rising edge		2.10		2.45	V
Undervoltage Lockout IN4/5	$V_{UVLO-4/5}$	IN4/5 rising edge		2.10		2.45	V
Power-On Reset Threshold		IN1 falling edge		0.9		2.1	V
Supply Current in Shutdown	I_{SHDN}	$\overline{OFF}$ = 0, $\overline{ON}$ = IN1				10	µA
Supply Current (Standby)	I_{ON}	OUT1 ON, other regulators OFF I_{OUT1} = 0				230	µA
Supply Current (All Outputs On)		All regulators ON, $I_{OUT\_}$ = 0				680	µA
BP Voltage		I_{BP} ≤ 1nA		1.225		1.275	V
OUT1 REGULATOR							
Output Accuracy		I_{OUT1} = 70mA (Note 3)		-2.5		2.5	%
Output Accuracy (Line and Load)		1mA ≤ I_{OUT1} ≤ 300mA, 2.5V ≤ V_{IN1} ≤ 5.5V, V_{OUT1} = 1.8V (Note 3)		-3.5		3.5	%
Nominal-Voltage Adjust Range		32 steps through serial interface; Tables 2, 3		1.8		3.3	V
Dropout Voltage		I_{OUT1} = 200mA (Notes 1, 3)				125	mV
Line Regulation		2.5V ≤ V_{IN1} ≤ 5.5V, V_{OUT1} = 1.8V (Note 3)		-0.15		0.11	%/V
Current Limit				320		850	mA
Output-Discharge Switch Resistance in Shutdown		Regulator output turned off				300	Ω
OUT1 Reset Threshold		OUT1 rising and falling	MAX1798/MAX1799	-9.5		-5.5	%
			MAX1798A/MAX1799A	-15		-11	
OUT2–5 REGULATORS							
Output Accuracy		$I_{OUT\_}$ = 50mA (Note 3)		-2.5		2.5	%
Output Accuracy (Line and Load)		1mA ≤ $I_{OUT\_}$ ≤ 150mA, 2.5V ≤ $V_{IN\_}$ ≤ 5.5V, $V_{OUT\_}$ = 1.8V (Note 3)		-3.5		3.5	%
Nominal-Voltage Adjust Range		32 steps through serial interface; Tables 2, 3		1.8		3.3	V
Dropout Voltage		$I_{OUT\_}$ = 100mA (Notes 1, 3)				100	mV
Line Regulation		2.5V ≤ $V_{IN\_}$ ≤ 5.5V, $V_{OUT\_}$ = 1.8V (Note 3)		-0.15		0.11	%/V
Current Limit				160		500	mA
Output-Discharge Switch Resistance in Shutdown		Regulator output turned off				300	Ω

CDMA Cellular/PCS System Power Supplies

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN1} = $V_{IN2/3}$ = $V_{IN4/5}$ = $V_{SCLK\ (SCK)}$ = $V_{DIN\ (SDA)}$ = $V_{\overline{CS}\ (AS)}$ = $V_{\overline{OFF}}$ = 3.6V; $\overline{ON}$ = GND = PGND = 0; RSO, ONO, DR1, DR2 = open; BP bypassed with 0.01µF, OUT1 bypassed with 4.7µF; OUT2, OUT3, OUT4, OUT5 bypassed with 2.2µF; OUT1–5 set to 2.98V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC AND CONTROL INPUTS ($\overline{ON}$, $\overline{OFF}$, $\overline{RSO}$ DIN (SDA), SCLK (SCK), $\overline{CS}$ (AS))						
Reset Timer			140		430	ms
Watchdog Timer			35		110	ms
OUT1 Shutdown Timer (MAX1798A/MAX1799A only)			175		540	ms
Input Low Level	V_{IL}				0.4	V
Input High Level	V_{IH}		1.6			V
SDA Output Low Level (MAX1799 only)		$I_{DIN\ (SDA)}$ = 3mA			0.4	V
		$I_{DIN\ (SDA)}$ = 6mA			0.6	
Logic Input Current		0 ≤ V_{IN} ≤ V_{IN1}; $\overline{ON}$, DIN (SDA), SCLK (SCK), and $\overline{CS}$ (AS) only	-1		1	µA
$\overline{OFF}$ Pulldown Resistance		$\overline{OFF}$ = 5.5V	80		360	kΩ
ONO Output Low Level		I_{ONO} = 1mA			0.5	V
ONO Output High Level		I_{ONO} = -1mA	V_{OUT1} - 0.5			V
$\overline{RSO}$ Output Low Level		I_{RSO} = 1mA, V_{IN1} = 1V			0.5	V
$\overline{RSO}$ Output High Level (Internal Pullup Resistor)		I_{RSO} = 0	V_{OUT1} - 0.5			V
$\overline{RSO}$ Reset Resistance		$\overline{RSO}$ = 2.48V	9		19	kΩ
DR1, DR2 Output Low Level		I_{DR1} = I_{DR2} = 100mA (Note 3)			0.5	V
DR1, DR2 OFF Current (Leakage)	I_{OFF}	V_{DR1} = V_{DR2} = 5.5V	-1		1	µA
I^2C (SMB) TIMING (MAX1799/MAX1799A)						
Clock Frequency	SCK				400	kHz
Bus-Free Time Between START and STOP	t_{BUF}		1.3			µs
Hold Time Repeated START Condition	t_{HD_STA}		0.6			µs
SCK Low Period	t_{LOW}		1.3			µs
SCK High Period	t_{HIGH}		0.6			µs
Setup Time Repeated START Condition	t_{SU_STA}		0.6			µs
Data Hold Time	t_{HD_DAT}		0	89		µs
Data Setup Time	t_{SU_DAT}		100			ns
Setup Time for STOP Condition	t_{SU_STO}		0.6			µs

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN1} = $V_{IN2/3}$ = $V_{IN4/5}$ = $V_{SCLK\ (SCK)}$ = $V_{DIN\ (SDA)}$ = $V_{\overline{CS}\ (AS)}$ = $V_{\overline{OFF}}$ = 3.6V; $\overline{ON}$ = GND = PGND = 0; RSO, ONO, DR1, DR2 = open; BP bypassed with 0.01µF, OUT1 bypassed with 4.7µF; OUT2, OUT3, OUT4, OUT5 bypassed with 2.2µF; OUT1–5 set to 2.98V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

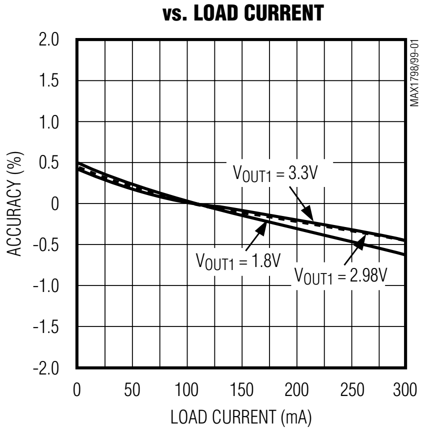
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SPI TIMING (MAX1798/MAX1798A)						
SCLK Clock Frequency	f_{SCLK}				2	MHz
SCLK Low Period	t_{cl}		125			ns
SCLK High Period	t_{ch}		125			ns
Data Hold Time	t_{HD_DAT}		0			ns
Data Setup Time	t_{SU_DAT}		125			ns
$\overline{CS}$ Assertion to SCLK Rising Edge Setup Time	t_{CSS}		200			ns
$\overline{CS}$ Deassertion to SCLK Rising Edge Setup Time	t_{CS1}		200			ns
SCLK Rising Edge to $\overline{CS}$ Deassertion	t_{CSH}		200			ns
SCLK Rising Edge to $\overline{CS}$ Assertion	t_{CSO}		200			ns
$\overline{CS}$ High Period	t_{CSW}		300			ns

Note 1: The dropout voltage is defined as (V_{IN} - V_{OUT}) when V_{OUT} is 100mV below the value of V_{OUT} for V_{IN} = V_{OUT} + 1V.
Note 2: Specifications to -40°C are guaranteed by design, not production tested.
Note 3: Specifications are guaranteed by design, not production tested in the ETP (TQFN) packages.

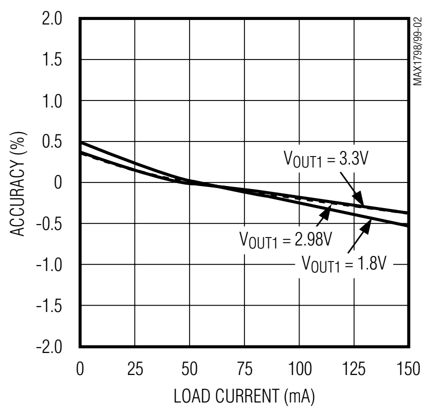
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

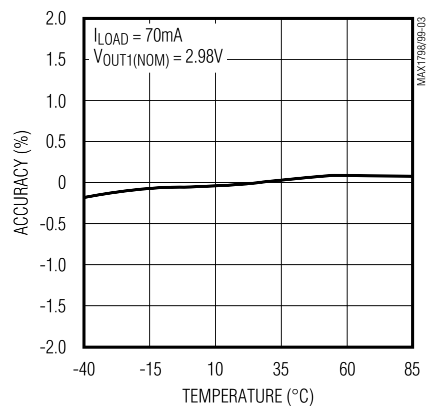
OUTPUT VOLTAGE ACCURACY (OUT1) vs. LOAD CURRENT



OUTPUT VOLTAGE ACCURACY (OUT2–5) vs. LOAD CURRENT



OUTPUT VOLTAGE ACCURACY (OUT1) vs. TEMPERATURE

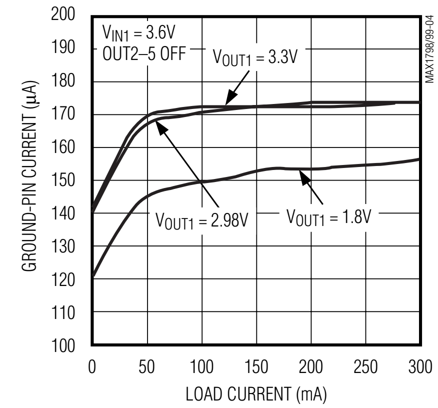


CDMA Cellular/PCS System Power Supplies

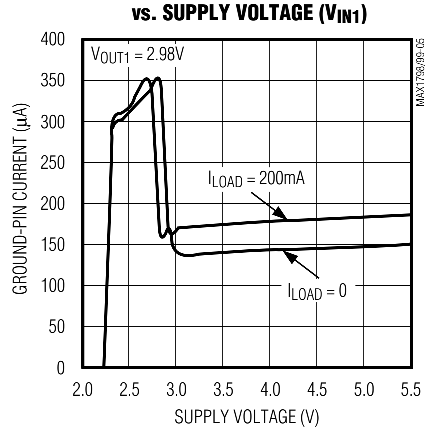
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

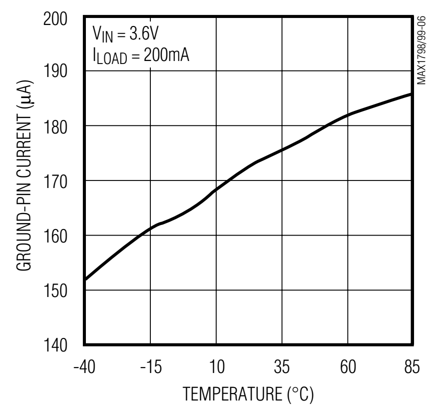
GROUND-PIN CURRENT (OUT1) vs. LOAD CURRENT



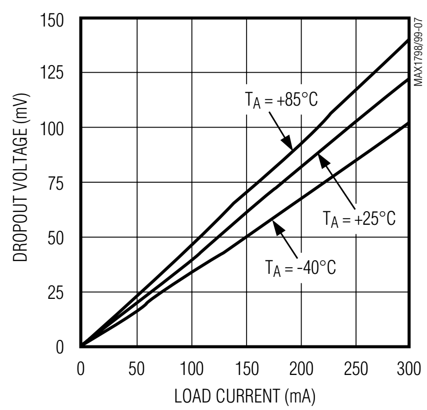
GROUND-PIN CURRENT (OUT1) vs. SUPPLY VOLTAGE (V_{IN1})



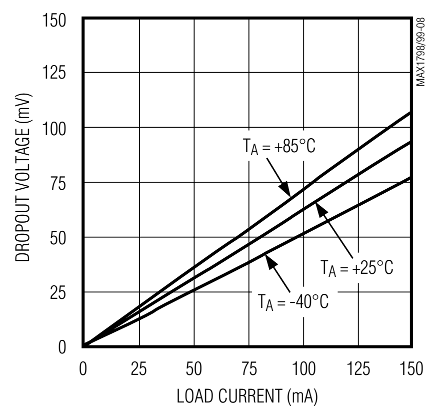
GROUND-PIN CURRENT (OUT1) vs. TEMPERATURE



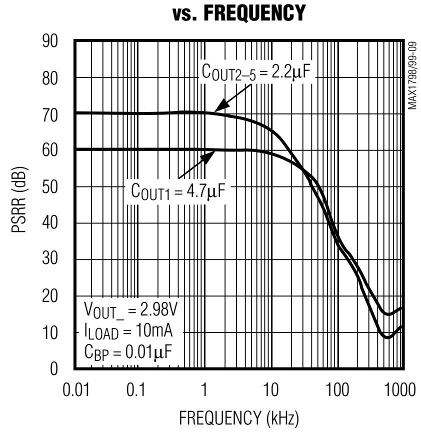
DROPOUT VOLTAGE (OUT1) vs. LOAD CURRENT



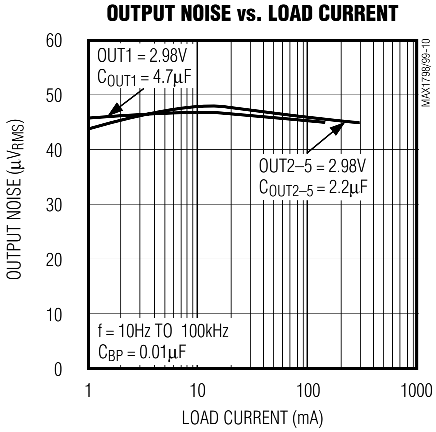
DROPOUT VOLTAGE (OUT2–5) vs. LOAD CURRENT



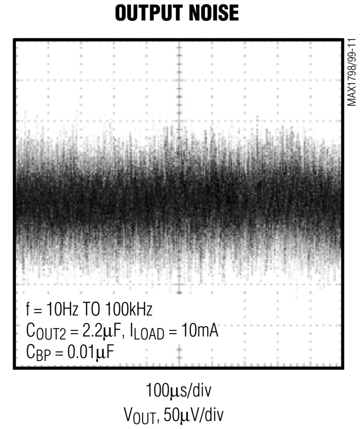
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



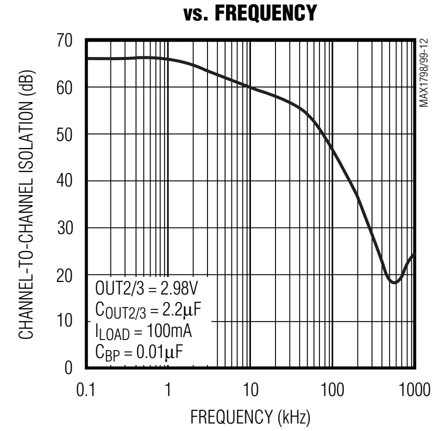
OUTPUT NOISE vs. LOAD CURRENT



OUTPUT NOISE



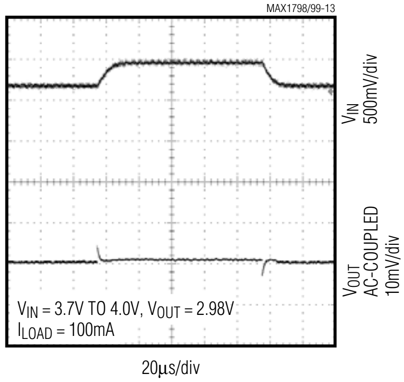
CHANNEL-TO-CHANNEL ISOLATION vs. FREQUENCY



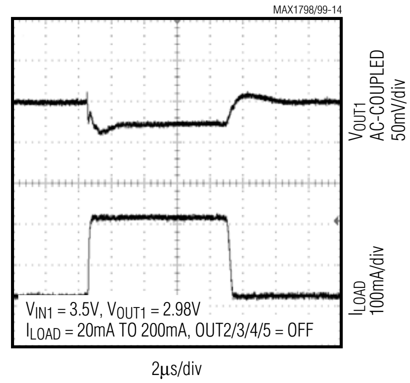
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

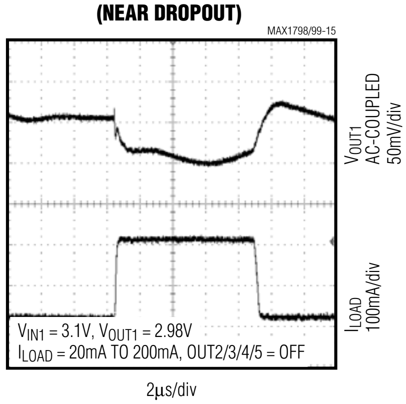
LINE-TRANSIENT RESPONSE



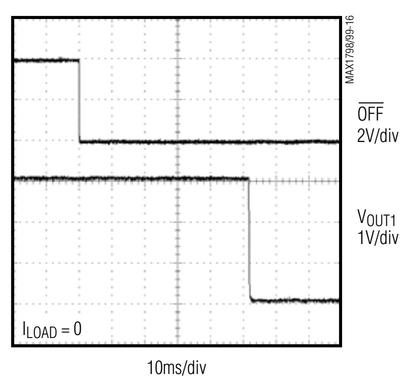
LOAD-TRANSIENT RESPONSE



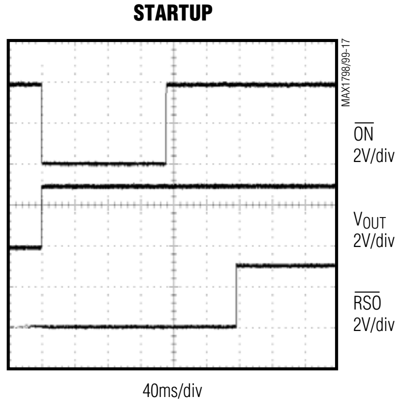
LOAD-TRANSIENT RESPONSE (NEAR DROPOUT)



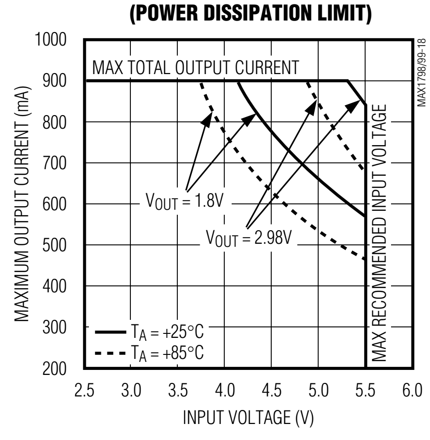
ENTERING SHUTDOWN



STARTUP



TSSOP/TQFN SAFE OPERATING AREA (POWER DISSIPATION LIMIT)



CDMA Cellular/PCS System Power Supplies

Pin Description

PIN		NAME	FUNCTION
TSSOP	QFN		
1	19	$\overline{CS}$ (AS)	Chip-Select Input for SPI (MAX1798/MAX1798A). Address Select Input for I^2C (MAX1799/MAX1799A).
2	20	SCLK (SCK)	Clock Input for Serial Interface. Data is read on the rising edge of the clock. SCLK for MAX1798/MAX1798A. SCK for MAX1799/MAX1799A.
3	1	DIN (SDA)	Data Input for Serial Interface. Data is read on the rising edge of the clock. DIN for MAX1798/MAX1798A. SDA for MAX1799/MAX1799A.
4	2	ONO	On Output. Indicates the state of $\overline{ON}$. After initial power-up, the logic level of this pin follows that of $\overline{ON}$. Used to signal the microcontroller (µC) for an OFF request (allows push-on/push-off).
5	3	GND	Ground
6	4	BP	1.25V Reference Bypass. Connect a 0.01µF bypass capacitor to GND for reduced noise. **Do not load this pin**.
7	5	PGND	Power Ground
8	6	$\overline{RSO}$	Reset Output. Holds the µC system reset line low during initial startup and whenever OUT1 falls out of regulation. $\overline{RSO}$ has a 140ms (min) timeout period and is an open-drain output with an internal 14kΩ pullup to OUT1. The $\overline{RSO}$ line maintains a valid low output level for IN1 as low as 1V.
9	7	DR1	2Ω Open-Drain Driver Output 1. Maximum sink current is 150mA (100mA_{RMS}). Can drive up to 10 LEDs for backlight or a vibrator motor.
10	8	DR2	2Ω Open-Drain Driver Output 2. Maximum sink current is 150mA (100mA_{RMS}). Can drive up to 10 LEDs for backlight or a vibrator motor.
11	9	OFF	OFF Input. A low level to this pin when $\overline{ON}$ is high turns off the IC once the watchdog timer has timed out. A high-level input keeps the chip on. There is an internal 155kΩ pulldown resistor at this input.
12	10	OUT5	Output 5, Output of Linear Regulator 5; 150mA (max) Output Current. Connect a 2.2µF ceramic bypass capacitor to PGND.
13	11	IN4/5	Supply Inputs 4 and 5. Voltage supply for linear regulators 4 and 5.
14	12	OUT4	Output 4, Output of Linear Regulator 4; 150mA (max) Output Current. Connect a 2.2µF ceramic bypass capacitor to PGND.
15	13	OUT1	Output 1, Output of Linear Regulator 1; 300mA (max) Output Current. Connect a 4.7µF ceramic bypass capacitor to PGND.
16	14	IN1	Supply Input 1. Voltage supply for linear regulator 1 and serial interface.
17	15	OUT3	Output 3, Output of Linear Regulator 3; 150mA (max) Output Current. Connect a 2.2µF ceramic bypass capacitor to PGND.
18	16	IN2/3	Supply Inputs 2 and 3. Voltage supply for linear regulators 2 and 3.
19	17	OUT2	Output 2, Output of Linear Regulator 2; 150mA (max) Output Current. Connect a 2.2µF ceramic bypass capacitor to PGND
20	18	$\overline{ON}$	ON Input. An active-low turns on the device, enabling LDO1, RESET, the ON/OFF logic, and the serial interface.
—	—	EP	Exposed Pad. Connect the exposed pad to a ground plane to provide heat sinking.

Table 1. Control Data Byte

FUNCTION	COMMAND			DIN (SDA)				
	C2	C1	C0	D4	D3	D2	D1	D0
Update DAC Outputs	0	0	0	U5			U2	U1
OUT1 DAC	0	0	1	DAC1 (Table 2)				
OUT2 DAC	0	1	0	DAC1 (Table 2)				
OUT3 DAC	0	1	1	DAC1 (Table 2)				
OUT4 DAC	1	0	0	DAC1 (Table 2)				
OUT5 DAC	1	0	1	DAC1 (Table 2)				
Driver Outputs	1	1	0	X	X	X	DR2	DR1
ON/OFF Conrol	1	1	1	ON5	ON4	ON3	ON2	ON1

Note: *C2 is MSB, and D0 is LSB. X = Don't care.*

Detailed Description

The MAX1798/MAX1798A/MAX1799/MAX1799A drive CDMA cellular and PCS handsets or systems with inputs from 2.5V to 5.5V. The devices contain five LDOs, two open-drain outputs, and a reset output as shown in Figure 1. All outputs are individually programmable through either an SPI (MAX1798/MAX1798A) or I^2C (MAX1799/MAX1799A) serial-port interface. The outputs may be turned on or off individually through the serial interface. Their output voltages are adjustable from 1.8V to 3.3V in 32 increments. At power-up, all outputs are at a default value of 2.98V, but only OUT1 is on. OUT1 is rated for 300mA and optimized for low dropout. OUT2–5 are rated for 150mA. All LDOs are optimized for low noise, high isolation, and low dropout.

Linear Regulator 1

Regulator 1 is a low-dropout linear regulator that sources 300mA (max), operating from a 2.5V to 5.5V input voltage (V_{IN1}). OUT1 is turned on by using the on button. OUT1 is turned off by using either the off pin or the serial port. Its output can be adjusted from 1.8V to 3.3V from the SPI or I^2C serial-port interface by setting the control data byte (Table 1). OUT1 is always on when the MAX1798/MAX1798A/MAX1799/MAX1799A are on. If OUT1 is turned off, the entire IC shuts down. If V_{IN1} falls below 1V, a POR circuit resets all LDO voltages to 2.98V and OUT1 is left on while OUT2–5 are turned off.

Linear Regulators 2–5

Regulators 2–5 are LDOs that source 150mA (max) from input voltages ($V_{IN2/3}$ and $V_{IN4/5}$) of 2.5V to 5.5V. OUT2–5 can be turned on or off and adjusted from 1.8V to 3.3V through the SPI or I^2C serial-port interface by setting the control data byte (Table 1). At power-up, OUT2–5 are set to 2.98V, but turned off. The control data byte must be used to turn them on. If V_{IN1} falls below 1V, a POR circuit resets all LDO voltages to 2.98V and OUT2–5 are turned off. If $V_{IN2/3}$ or $V_{IN4/5}$ fall below 2.15V, the UVLO circuit turns off the corresponding output, but all LDO voltages remain at their prior settings. OUT2–5 are optimized for low noise and high isolation.

Open-Drain Outputs

The open-drain N-channel MOSFETs (DR1 and DR2, Figure 2) have a nominal 2Ω on-resistance and can be used to drive up to 10 LEDs for backlight or a vibrator motor. DR1 and DR2 can sink $100mA_{RMS}$ (max). At power-up, DR1 and DR2 are high impedance and are commanded on by the control data byte.

$\overline{RSO}$

$\overline{RSO}$ is an open-drain output, connected to OUT1 through an internal 14kΩ resistor. At power-up, OUT1 turns on and $\overline{RSO}$ is held low for 140ms (min). When $\overline{RSO}$ goes high, $\overline{OFF}$ must be brought high within 35ms to keep OUT1 on. Otherwise, if $\overline{OFF}$ is low, the watchdog timer circuit counts down 35ms (min), and $\overline{RSO}$ is actively held low while the entire device turns off.

The MAX1798/MAX1799 $\overline{RSO}$ goes low when OUT1 droops by more than 7.5% ±2% of its programmed output voltage. The MAX1798A/MAX1799A $\overline{RSO}$ goes low when OUT1 droops by more than 13% ±2% of its programmed output voltage. $\overline{RSO}$ stays low for 140ms (min) after OUT1 rises above the threshold. During this time, the watchdog timer circuit is inactive.

The MAX1798A/MAX1799A have an additional timer circuit to shut down the regulators when the $\overline{RSO}$ and watchdog timer time out. If the OUT1 voltage level ever exceeds the $\overline{RSO}$ threshold level before the reset and

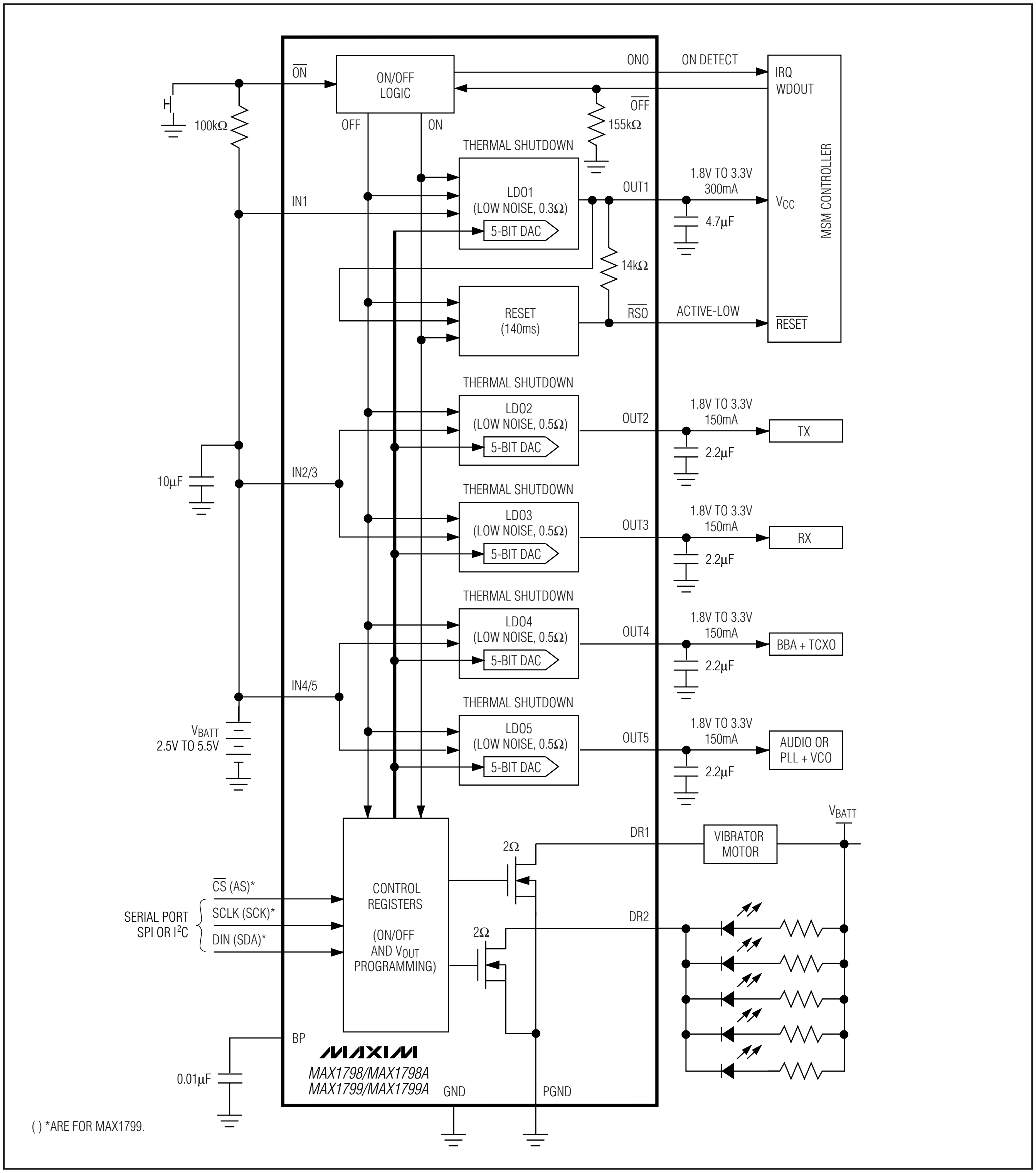


Figure 1. Typical Application Circuit/Functional Diagram

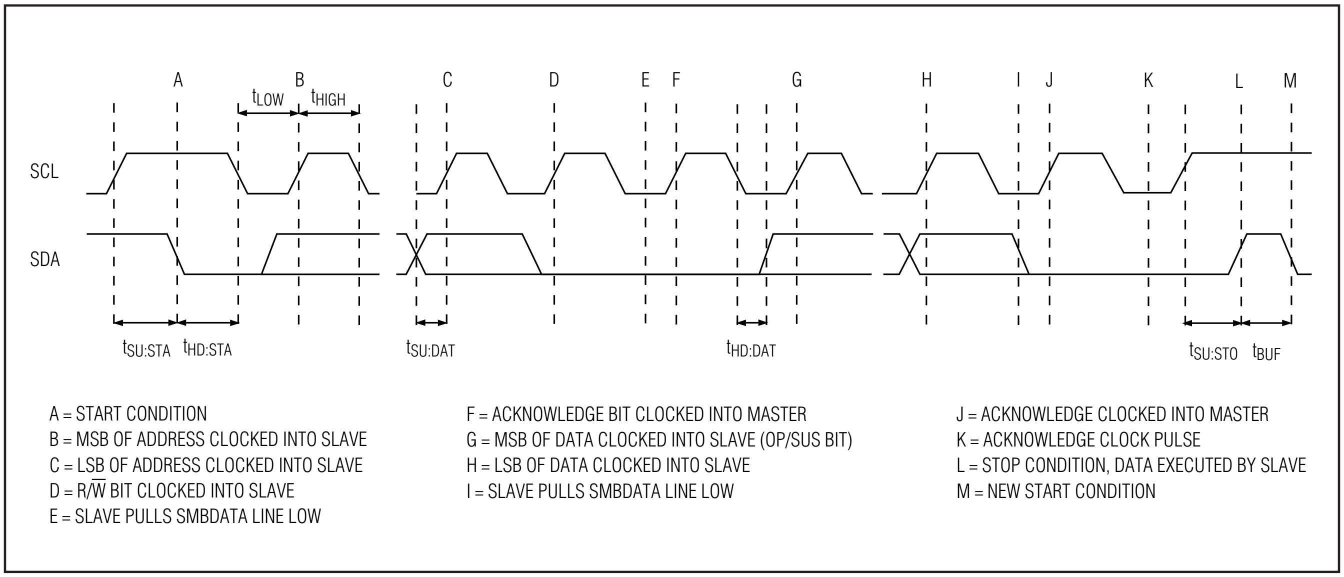


Figure 2. I²C-Compatible Serial-Interface Timing Diagram

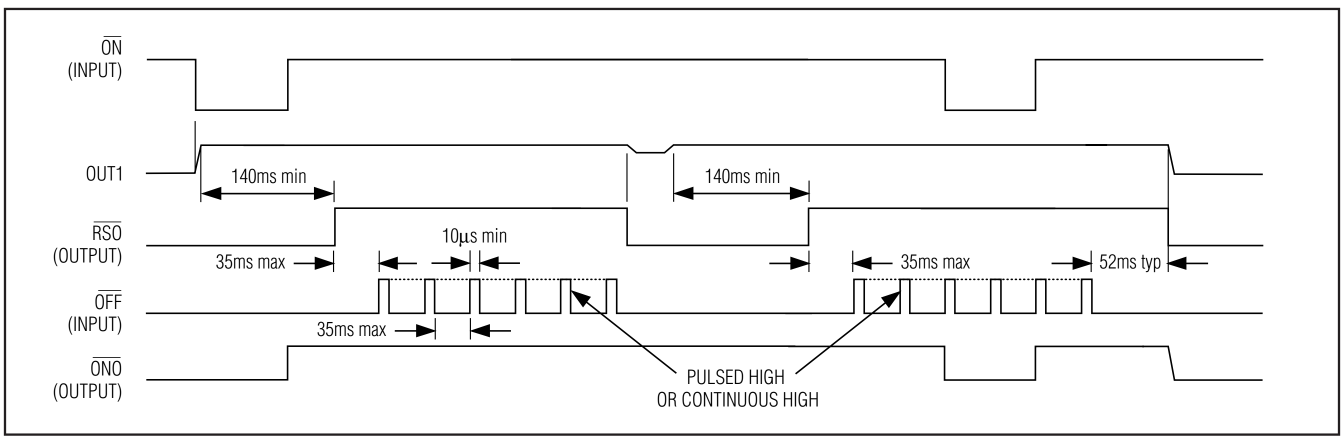


Figure 3. Push-On/Push-Off Startup and Shutdown Timing Diagram

watchdog timers time out, the shutdown timer is reset. The shutdown timer requires continuous low $\overline{RSO}$ signal and continuous nontriggered watchdog timer to shut down the regulators.

$\overline{ON}$ and $\overline{OFF}$ Logic

See Figure 3. The MAX1798/MAX1798A/MAX1799/MAX1799A power up when V_{IN1} is greater than 2.5V and $\overline{ON}$ is low ($\overline{ON}$ button is pressed down momentarily). When $\overline{ON}$ returns high, the device remains on. It turns on OUT1 and the serial interface port. Once OUT1 is in regulation, $\overline{RSO}$ stays low an additional 140ms (min). At this time, OUT1 is on and set to 2.98V, while OUT2–5 are disabled and set to 2.98V. To stay on, the $\overline{OFF}$ pin must be in a high state within 35ms (min) or the device will shut down and can only be turned on by pressing the $\overline{ON}$ button. While $\overline{ON}$ is held low, the status of $\overline{OFF}$ is irrelevant and OUT1 and the serial port are on.

After initial power-up, the logic level of ONO follows the logic level of $\overline{ON}$ but is level-shifted to OUT1 high voltage. This signal can be used to interrupt the system controller, which can subsequently manage an orderly shutdown through the serial port by turning off OUT1.

CDMA Cellular/PCS System Power Supplies

Hard Shutdown

To shut down the MAX1798/MAX1798A/MAX1799/MAX1799A, drive $\overline{OFF}$ low or allow the internal resistor to pull down $\overline{OFF}$ while $\overline{ON}$ is high. The device shuts down after the watchdog timer has cleared (35ms min, 52ms typ). During shutdown, all LDO outputs and $\overline{RSO}$ are actively pulled to GND, the open-drain drivers are in a high-impedance state, and the serial port and reset timer are inactive. Previously programmed output voltage data is retained in the internal registers as long as V_{IN1} > 2.1V. If the device is turned back on by the $\overline{ON}$ button, OUT1 automatically is enabled with the preshutdown output voltage. OUT2–5 automatically return to their preshutdown voltages once they are enabled through the serial interface.

Soft Shutdown

The serial port can also be used to shut down the MAX1798/MAX1798A/MAX1799/MAX1799A. Using the control data byte to disable OUT1 will shut down the entire device. Once shut down, the only means to turn on the device is through a momentary low on the $\overline{ON}$ button.

Control Data Byte

The control data byte is 8 bits long (3 command bits and 5 data bits). The first 3 bits specify the action to be taken, while the last 5 bits set the output voltage or ON/OFF status. Each regulator has an individual DAC that sets the output voltage. The DAC registers are double buffered to allow for simultaneous updating of all outputs. The output voltage is programmed per Table 2 or Table 3. At power-up, if no specific voltage is programmed, OUT1–5 will be set for 2.98V. All DAC programming must be shifted from the double buffer to the DACs with the update DAC command (Table 1, 000XXXXX) for the programmed voltages to be seen at the LDO outputs. The DACs can be updated one at a time or all at once after all desired outputs are programmed. The ON/OFF status of the LDOs and drivers is not double-buffered and takes immediate effect upon $\overline{CS}$ returning high (SPI compatible) or upon the ninth rising edge of SCK during the command byte (Figure 2, edge L). A one turns on the LDO output or driver output, and a zero turns it off.

SPI-Compatible Serial Interface

Use an SPI-compatible 3-wire serial interface with the MAX1798/MAX1798A to control the ON/OFF state and output voltage of each regulator, the ON/OFF state of the drivers, and to shut down the device. Figures 4a and 4b are timing diagrams for the SPI protocol. The MAX1798/MAX1798A is a write-only device and uses $\overline{CS}$ along with SCLK and DIN to communicate. The serial port operates when the device is enabled, even when $\overline{RSO}$ is low. The MAX1798/MAX1798A can support a 2MHz (max) data rate. This SPI-compatible port uses the CPOL = CPHA = 0 protocol.

I²C-Compatible Serial Interface

Use an I²C-compatible 2-wire serial interface with the MAX1799/MAX1799A to control the ON/OFF state and output voltage of each regulator, the ON/OFF state of the drivers, and to shut down the device. Use standard I²C-compatible write-byte commands to program the IC. Figure 2 is a timing diagram for the I²C protocol. The MAX1799/MAX1799A is always a slave to the bus master. The serial port operates when the device is enabled, even when OUT1 and $\overline{RSO}$ are low. When AS is high, the address is 0111111. When AS is low, the address is 1001111. Two MAX1799/MAX1799A devices can be controlled by a single bus master.

Output Voltage

The MAX1798/MAX1798A/MAX1799/MAX1799A are supplied with factory-set output voltages. At power-up, all DACS are set for 2.98V, while only OUT1 is enabled; all other LDO outputs and drivers are off. OUT2–5, DR1, and DR2 must be enabled on with the serial port. OUT2–5 can be individually programmed through the serial port from 1.8V to 3.3V in 32 steps, either while on or off. OUT1 can be programmed in 32 steps from 1.8V to 3.3V only while on. (If OUT1 is off, the serial port is also off, and OUT1 cannot be programmed.) If OUT1 is turned off through the serial port or the $\overline{OFF}$ pin, the entire chip, including the serial port, will be shut down. However, all previously programmed DAC settings will be retained as long as a valid supply voltage is maintained on IN1 (V_{IN1} > 2.1V).

Current Limit

The MAX1798/MAX1798A/MAX1799/MAX1799A include current limiting on each LDO output. OUT1 has a current limit set at 500mA (320mA min), while OUT2–5 have current limits set at 250mA (160mA min). When the LDO output is in current limit, the current-limiter device monitors and controls the pass transistor's gate voltage, limiting the output current available from the LDO. Once the excessive load is removed, normal function resumes automatically.

Table 2. OUT1–5 Output Voltages (Binary Format)

REGULATOR OUTPUT VOLTAGE (V)	DAC_ DATA				
OUT1–OUT5	D4	D3	D2	D1	D0
1.800	0	0	0	0	0
1.827	0	0	0	0	1
1.854	0	0	0	1	0
1.883	0	0	0	1	1
1.912	0	0	1	0	0
1.942	0	0	1	0	1
1.974	0	0	1	1	0
2.006	0	0	1	1	1
2.039	0	1	0	0	0
2.074	0	1	0	0	1
2.109	0	1	0	1	0
2.146	0	1	0	1	1
2.184	0	1	1	0	0
2.224	0	1	1	0	1
2.265	0	1	1	1	0
2.308	0	1	1	1	1
2.352	1	0	0	0	0
2.398	1	0	0	0	1
2.445	1	0	0	1	0
2.495	1	0	0	1	1
2.547	1	0	1	0	0
2.601	1	0	1	0	1
2.657	1	0	1	1	0
2.716	1	0	1	1	1
2.777	1	1	0	0	0
2.842	1	1	0	0	1
2.909	1	1	0	1	0
2.980	1	1	0	1	1
3.054	1	1	1	0	0
3.132	1	1	1	0	1
3.214	1	1	1	1	0
3.300	1	1	1	1	1

Table 3. OUT1–5 Output Voltages (Hexadecimal Format)

REGULATOR OUTPUT VOLTAGE (V)	DAC_ DATA				
OUT1–OUT5	OUT5	OUT4	OUT3	OUT2	OUT1
1.800	A0	80	60	40	20
1.827	A1	81	61	41	21
1.854	A2	82	62	42	22
1.883	A3	83	63	43	23
1.912	A4	84	64	44	24
1.942	A5	85	65	45	25
1.974	A6	86	66	46	26
2.006	A7	87	67	47	27
2.039	A8	88	68	48	28
2.074	A9	89	69	49	29
2.109	AA	8A	6A	4A	2A
2.146	AB	8B	6B	4B	2B
2.184	AC	8C	6C	4C	2C
2.224	AD	8D	6D	4D	2D
2.265	AE	8E	6E	4E	2E
2.308	AF	8F	6F	4F	2F
2.352	B0	90	70	50	30
2.398	B1	91	71	51	31
2.445	B2	92	72	52	32
2.495	B3	93	73	53	33
2.547	B4	94	74	54	34
2.601	B5	95	75	55	35
2.657	B6	96	76	56	36
2.716	B7	97	77	57	37
2.777	B8	98	78	58	38
2.842	B9	99	79	59	39
2.909	BA	9A	7A	5A	3A
2.980	BB	9B	7B	5B	3B
3.054	BC	9C	7C	5C	3C
3.132	BD	9D	7D	5D	3D
3.214	BE	9E	7E	5E	3E
3.300	BF	9F	7F	5F	3F

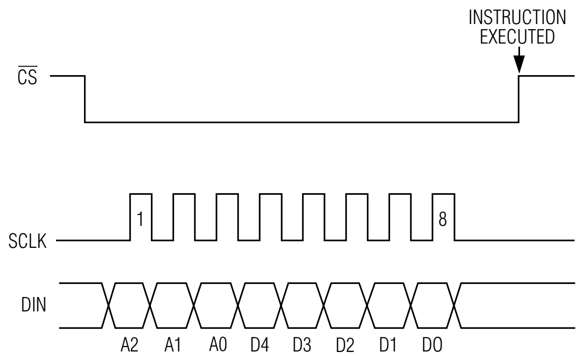


Figure 4a. Serial-Interface Timing Diagram

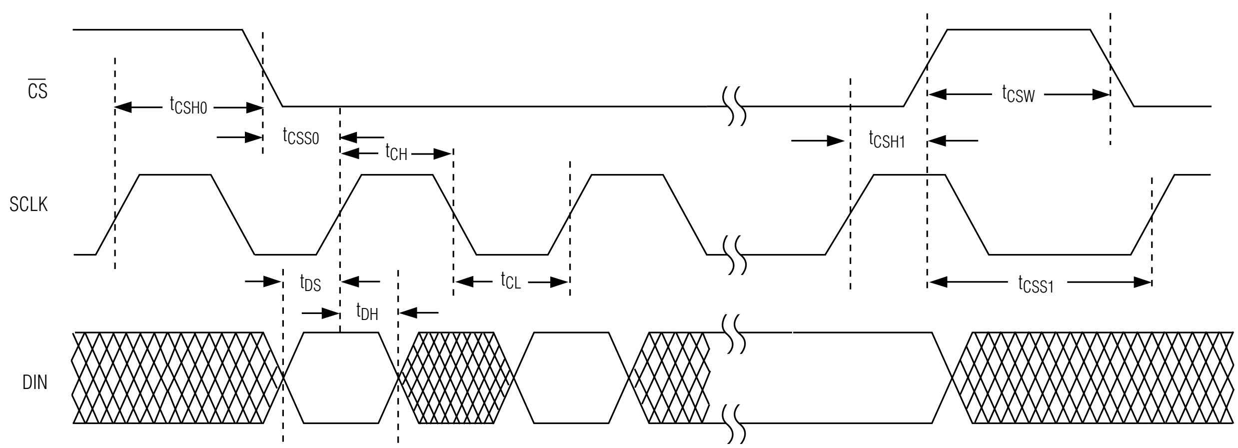


Figure 4b. Detailed Serial-Interface Timing Diagram

Thermal-Overload Protection

The MAX1798/MAX1798A/MAX1799/MAX1799A integrate a separate thermal monitor for each linear regulator. When the junction temperature of any LDO exceeds T_J = +160°C, the specific thermal sensor signals the shutdown logic, turning off the pass transistor and allowing that LDO to cool. The thermal sensor turns the pass transistor on again after the LDO's junction temperature cools by 10°C, resulting in a pulsed output during continuous thermal-overload conditions. Due to the substrate's thermal conductivity, a thermal overload on one LDO may possibly affect other LDOs on the device.

Thermal-overload protection is designed to protect the MAX1798/MAX1798A/MAX1799/MAX1799A in the event of fault conditions. For continual operation, do not exceed the absolute maximum junction-temperature rating of T_J = +150°C.

Noise Reduction

Bypass BP to GND with an external 0.01µF bypass capacitor. The MAX1798/MAX1798A/MAX1799/MAX1799A exhibit 45µV_{RMS} of output voltage noise. Graphs of Output Noise vs. Load Current, Output Noise (10Hz to 100kHz), PSRR vs. Frequency, and Channel-to-Channel Isolation vs. Frequency appear in the *Typical Operating Characteristics.*

Applications Information

Capacitor Selection and Regulator Stability

Use a 10µF low-ESR ceramic capacitor on the MAX1798/MAX1798A/MAX1799/MAX1799A's input if all the supply inputs are connected together. Larger input capacitance and lower ESR provide better supply noise rejection and line-transient response. If IN1, IN2/3, and IN4/5 are connected to different supply voltages, bypass each input with a 4.7µF low-ESR ceramic capacitor.

A minimum 4.7µF low-ESR ceramic capacitor is recommended on OUT1, and a minimum 2.2µF low-ESR ceramic capacitor is recommended on OUT2–5. The MAX1798/MAX1798A/MAX1799/MAX1799A are stable with output capacitors in the ESR range of 10mΩ to 1Ω. Use larger capacitors to reduce noise and improve load-transient response, stability, and power-supply rejection.

Note that some ceramic dielectrics exhibit large capacitance and ESR variation with temperature. With dielectrics such as Z5U and Y5V, it may be necessary to use a minimum 4.7µF on OUT2–5 to ensure stability at temperatures below -10°C. With X7R or X5R dielectrics, 2.2µF should be sufficient at all operating temperatures. Tantalum capacitors may cause instability with the MAX1798/MAX1798A/MAX1799/MAX1799A and are not recommended for this application.

Use a 0.01µF bypass capacitor at BP for low output-voltage noise. Increasing the capacitance will slightly decrease the output noise but will increase the startup time. Values above 0.1µF provide no performance advantage and are not recommended.

Line-Transient Considerations

The MAX1798/MAX1798A/MAX1799/MAX1799A are designed to deliver low dropout voltages and low quiescent currents in battery-powered systems. Power-supply rejection is >60dB at low frequencies and rolls off above 10kHz. See the Power-Supply Rejection Ratio (PSRR) vs. Frequency graph in the *Typical Operating Characteristics.*

When operating from sources other than batteries, improved supply noise rejection and transient response can be achieved by increasing the values of the input and output bypass capacitors and through passive filtering techniques. The *Typical Operating Characteristics* show the MAX1798/MAX1798A/MAX1799/MAX1799A line- and load-transient responses.

Load-Transient Considerations

The MAX1798/MAX1798A/MAX1799/MAX1799A load-transient response graphs (see *Typical Operating Characteristics*) show three components of the output response: the output capacitor's ESR spike, the regulator's transient settling response, and the DC shift due to the LDO's load regulation. Increasing the output capacitor's value and decreasing the ESR reduce the overshoot.

Dropout Voltage

A regulator's minimum input-output voltage differential (dropout voltage) determines the lowest usable supply voltage. In battery-powered systems, this determines the useful end-of-life battery voltage. Because the MAX1798/MAX1798A/MAX1799/MAX1799A use P-channel MOSFET pass transistors, their dropout voltage is a function of drain-to-source on-resistance ($R_{DS(ON)}$) multiplied by the load current. See the Dropout Voltage (OUT1) vs. Load Current graph in the *Typical Operating Characteristics.*

Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE	INTERFACE
MAX1799ETP+	-40°C to +85°C	20 TQFN	I^2C
MAX1799EUP+	-40°C to +85°C	20 TSSOP-EP	I^2C
MAX1799AETP+	-40°C to +85°C	20 TQFN	I^2C
MAX1799AEUP+	-40°C to +85°C	20 TSSOP-EP	I^2C

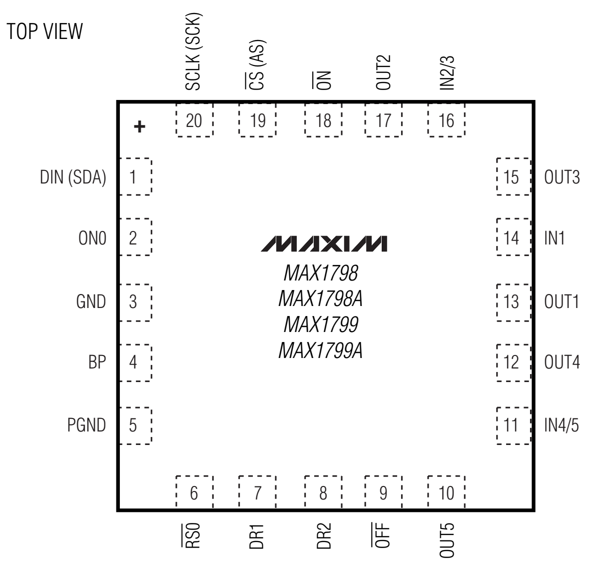
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

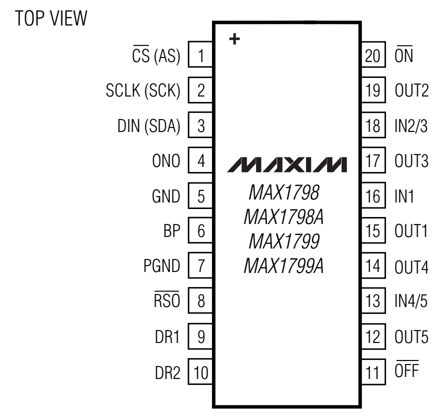
CDMA Cellular/PCS System Power Supplies

Pin Configurations



THIN QFN
5mm × 5mm × 0.75mm

( ) ARE FOR MAX1799/MAX1799A ONLY.



TSSOP

( ) ARE FOR MAX1799/MAX1799A ONLY.

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
20 TQFN	T2055+4	**21-0140**
20 TSSOP-EP	U20E+1	**21-0108**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
2	5/10	Replaced QFN package with TQFN package	1, 2, 7, 9, 10, 17, 18

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

© 2010 Maxim Integrated Products Maxim is a registered trademark of Maxim Integrated Products, Inc.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Maxim Integrated:

MAX1798EGP MAX1798EGP-T MAX1799EGP MAX1799EGP+ MAX1799EGP-T MAX1798EGP+ MAX1798EGP+T MAX1799EGP+T MAX1798AEUP MAX1798EUP MAX1798AEUP-T MAX1798EUP-T