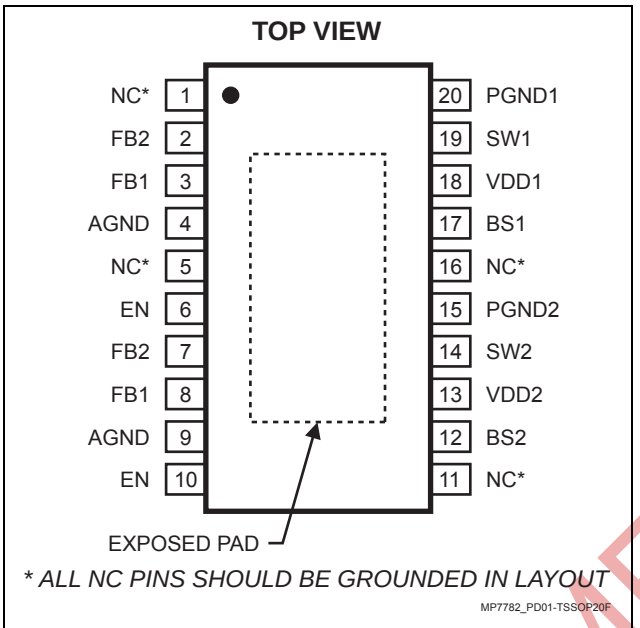
## PACKAGE REFERENCE




| Part Number* | Package | Temperature |
|---|---|---|
| MP7782DF | TSSOP20F | –40°C to +85°C |

* For Tape & Reel, add suffix –Z (eg. MP7782DF–Z)
For Lead Free, add suffix –LF (eg. MP7782DF–LF–Z)

## ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage $V_{DD}$ ..... 26V
BS Voltage ..... $V_{SW}$ – 0.3V to $V_{SW}$ + 6.5V
Enable Voltage $V_{EN}$ ..... –0.3V to +6V
$V_{SW}$, $V_{FB2}$, $V_{FB1}$ ..... –1V to $V_{DD}$ + 1V
AGND to PGND ..... –0.3V to +0.3V
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... –65°C to +150°C

### *Recommended Operating Conditions* (2)

Supply Voltage $V_{DD}$ ..... 9.5V to 24V
Operating Temperature $T_A$ ..... –40°C to +85°C

### *Thermal Resistance* (3)

| | $\theta_{JA}$ | $\theta_{JC}$ | |
|---|---|---|---|
| TSSOP20F ..... | 40 ..... | 6.... | °C/W |

**Notes:**
1) Exceeding these ratings may damage the device.
2) The device is not guaranteed to function outside of its operating conditions.
3) Measured on approximately 1" square of 1 oz copper.

## ELECTRICAL CHARACTERISTICS

**($V_{DD}$ = 24V, $V_{EN}$ = 5V, $T_A$ = +25°C, unless otherwise noted.)**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Supply Current** | | | | | | |
| Standby Current | | $V_{EN}$ = 0V | | 2 | 10 | µA |
| Quiescent Current | | | | 3 | 6 | mA |
| **Output Drivers** | | | | | | |
| SW On Resistance | | Sourcing and Sinking | | 0.18 | | Ω |
| Short Circuit Current | | Sourcing and Sinking | | 5.0 | | A |
| **Inputs** | | | | | | |
| FB1, FB2 Input Common Mode Voltage Range | | | 0 | $V_{DD}$/2 | $V_{DD}$–1.5 | V |
| FB1, FB2 Input Current | | $V_{FB2}$ = $V_{FB1}$ = 8V | | 1 | 5 | µA |
| EN Enable Threshold Voltage | | $V_{EN}$ Rising | | 1.4 | 2.0 | V |
| | | $V_{EN}$ Falling | 0.4 | 1.2 | | V |
| EN Enable Input Current | | $V_{EN}$ = 5V | | 1 | | µA |
| **Thermal Shutdown** | | | | | | |
| Thermal Shutdown Trip Point | | $T_J$ Rising | | 150 | | °C |
| Thermal Shutdown Hysteresis | | | | 30 | | °C |

## OPERATING SPECIFICATIONS

**(Circuit of Figure 1, $V_{DD}$ = 24V, $V_{EN}$ = 5V, $T_A$ = +25°C, unless otherwise noted.)**

| Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Standby Current | $V_{EN}$ = 0V | | 700 | | µA |
| Quiescent Current | | | 28 | | mA |
| Power Output | f = 1KHz, THD+N = 10%, $R_L$ = 6Ω | | 50 | | W |
| | f = 1KHz, THD+N = 10%, $R_L$ = 8Ω | | 40 | | |
| THD+ Noise | $P_{OUT}$ = 1W, f = 1KHz, $R_L$ = 6Ω | | 0.06 | | % |
| | $P_{OUT}$ = 1W, f = 1KHz, $R_L$ = 8Ω | | 0.08 | | |
| Efficiency | f = 1KHz, $P_{OUT}$ = 50W | | 90 | | % |
| Dynamic Range | | | 100 | | dB |
| Noise Floor | A-Weighted | | 187 | | µV |
| Power Supply Rejection | f = 1KHz | | 60 | | dB |

## PIN FUNCTIONS

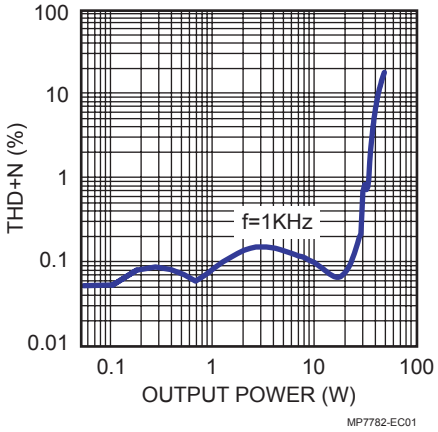
| Pin # | Name | Description |
|---|---|---|
| 1, 5, 11, 16 | NC | No Connect. Not internally connected. |
| 3, 8 | FB1 | First Feedback. Receives feedback from SW1 via resistor(s) and the positive input signal via resistor and capacitor. Both pins must be tied together. |
| 2, 7 | FB2 | Second Feedback. Receives feedback from SW2 via resistor(s) and the negative input signal via resistor and capacitor. Both pins must be tied together. |
| 4, 9 | AGND | Analog Ground. Both pins must be tied together. |
| 6, 10 | EN | Enable Input. Drive high to enable the MP7782, drive low to disable it. Both pins must be tied together. |
| 12 | BS2 | High-Side MOSFET Bootstrap Input for Channel 2. A capacitor from BS2 to SW2 supplies the gate drive current to the internal high-side MOSFET. Connect a 1µF capacitor from SW2 to BS2. See Figure 1. |
| 13 | VDD2 | Power Supply Input. Bypass VDD2 to PGND2 with a 1µF X7R capacitor (in addition to the main bulk capacitor), placed close to pins 13 and 15. |
| 14 | SW2 | Switched Power Output. SW2 is the output of Channel 2. Connect the LC filter to this pin. See Figure 1. |
| 15 | PGND2 | Power Ground for Channel 2. Connect PGND2 to PGND1. See Figure 1. |
| 17 | BS1 | High-Side MOSFET Bootstrap Input for Channel 1. A capacitor from BS1 to SW1 supplies the gate drive current to the internal high-side MOSFET. Connect a 1µF capacitor from SW1 to BS1. See Figure 1. |
| 18 | VDD1 | Power Supply Input. Bypass VDD1 to PGND1 with a 1µF X7R capacitor (in addition to the main bulk capacitor), placed close to pins 18 and 20. |
| 19 | SW1 | Switched Power Output. SW1 is the output of Channel 1. Connect the LC filter to this pin. See Figure 1. |
| 20 | PGND1 | Power Ground for Channel 1. Connect PGND1 to PGND2. See Figure 1. |

## TYPICAL PERFORMANCE CHARACTERISTICS

**Circuit of Figure 1, $V_{DD}$ = 24V, $T_A$ = +25˚C**

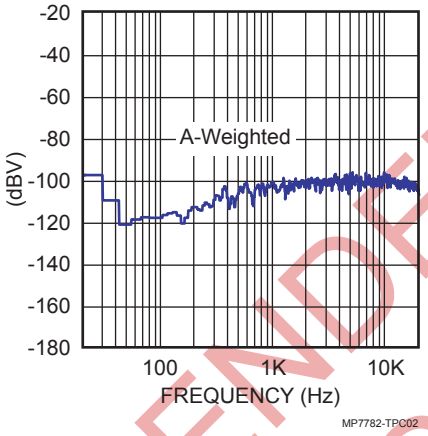
**THD+N vs. Output Power**

$V_{DD}$ = 24V, $R_L$ = 8Ω, $A_V$ = 30



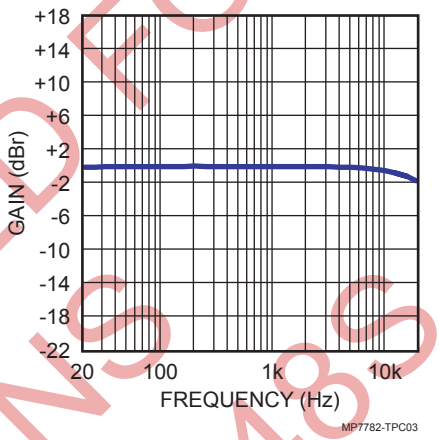

**FFT Noise Floor**

$V_{DD}$ = 24V, $R_L$ = 8Ω, $A_V$ = 30



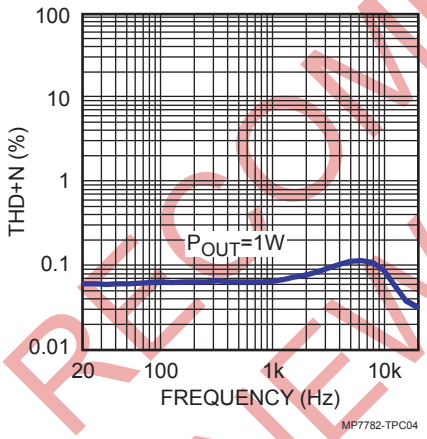

**Frequency Response**

$V_{DD}$ = 24V, $R_L$ = 8Ω, $A_V$ = 30



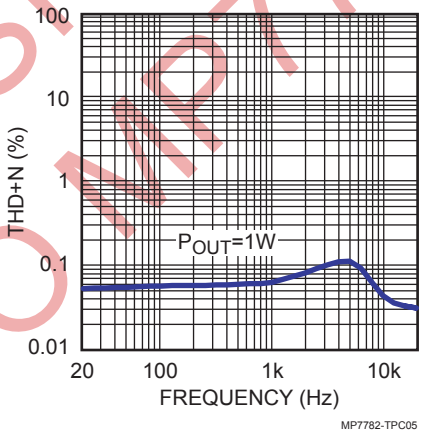

**THD+N vs. Output Power**

$V_{DD}$ = 24V, $R_L$ = 8Ω, $A_V$ = 30



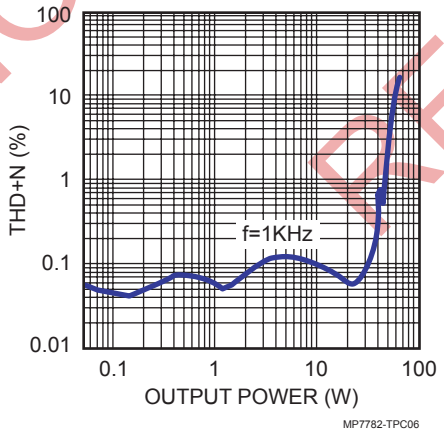

**THD+N vs. Output Power**

$V_{DD}$ = 24V, $R_L$ = 6Ω, $A_V$ = 30



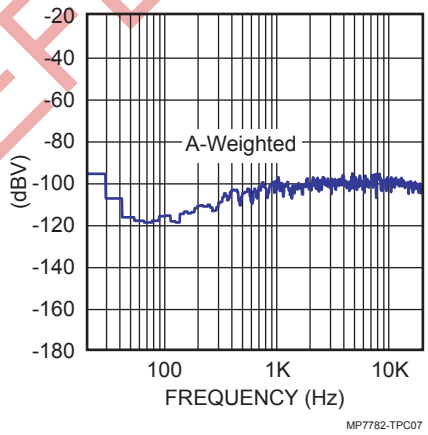

**THD+N vs. Output Power**

$V_{DD}$ = 24V, $R_L$ = 6Ω, $A_V$ = 30



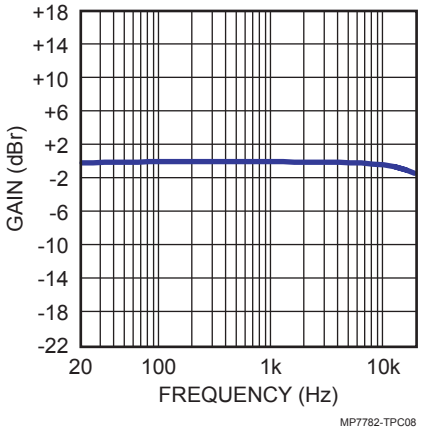

**FFT Noise Floor**

$V_{DD}$ = 24V, $R_L$ = 6Ω, $A_V$ = 30




**Frequency Response**

$V_{DD}$ = 24V, $R_L$ = 6Ω, $A_V$ = 30



## TYPICAL APPLICATION CIRCUIT

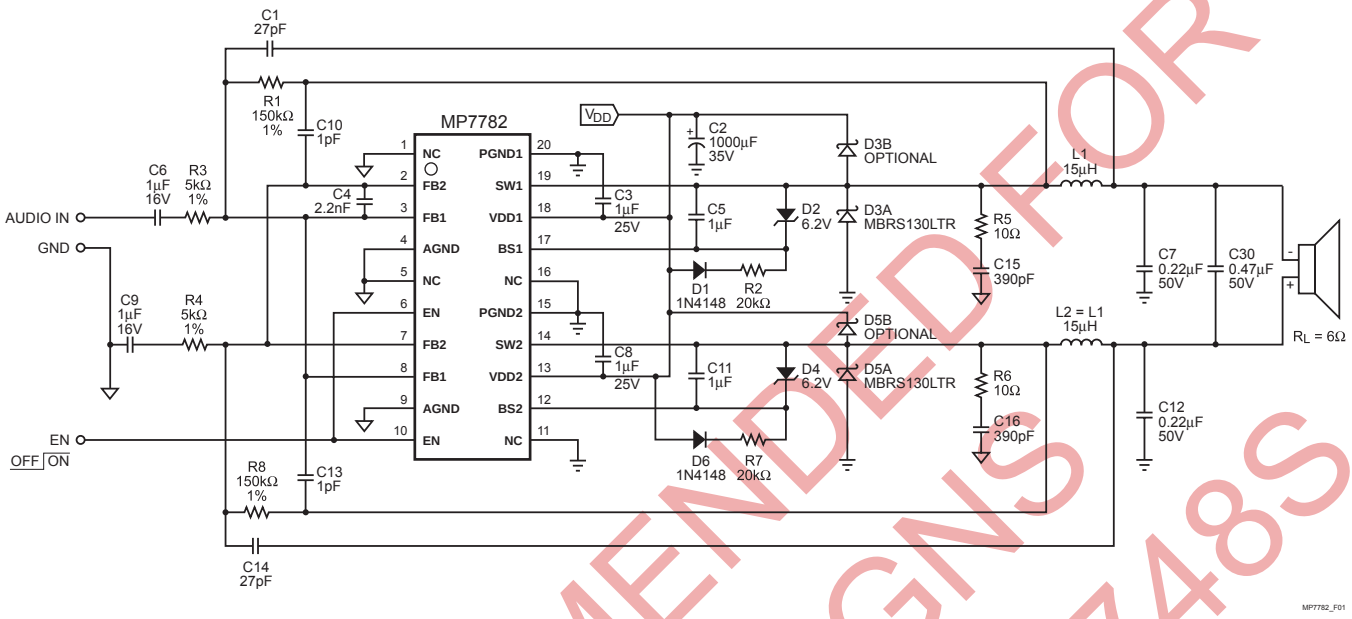



**Figure 1 — 50W Class D BTL Amplifier ($V_{DD}$ = 24V)**



## APPLICATION INFORMATION

### COMPONENT SELECTION

The MP7782 uses a minimum number of external components to complete a fully bridged Class D audio amplifier. The circuit in Figure 1 shows a typical application. Use the following sections to customize the amplifier for your particular application.

#### Setting the Voltage Gain

The voltage gain sets the output voltage swing for a given input voltage swing and is set by the following equation:

$$A_V = \frac{R_1}{R_3}$$

$$R8 = R1$$

$$R4 = R3$$

The maximum output voltage swing is limited by the power supply. The MP7782 is a bridged amplifier and the output load is driven differentially. Each side of the load is limited to a maximum peak-to-peak voltage swing approximately equal to $V_{DD}$. To achieve the maximum output power of the MP7782 amplifier, set the amplifier gain such that the maximum peak-to-peak input signal results in at least the maximum peak-to-peak output voltage swing.

#### Setting the Switching Frequency

The idle switching frequency (the switching frequency with no audio input signal) is a function of the supply voltage, $V_{DD}$, capacitors C4, C10 and C13 and resistors R1, R3, R4 and R8. Lower switching frequencies result in more inductor ripple, causing more quiescent output voltage ripple, increasing the output noise. Higher switching frequencies result in more power loss. The optimum quiescent switching frequency is approximately 400KHz to 600KHz. C10 and C13 are typically 1pF to 2.2pF. C4 is used to program the idle switching frequency.

### Choosing the LC Filter

Two identical LC filters are required in the typical application. The inductor-capacitor (LC) filter is a second order filter that converts the pulse train at SW (pins 14, 19) to the output differential signal that drives the speaker. Typical values for the LC filters are shown in Figure 1. The characteristic frequency of the LC filter needs to be high enough to allow high frequency audio to reach the output, yet needs to be low enough to filter out high frequency contents of the pulses from SW. The characteristic frequency of the LC filter is:

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

where:

$$L = L1 + L2,\ L1 = L2$$

$$C = C30 + \frac{C7 \times C12}{C7 + C12},\ C7 = C12$$

The quality factor (Q) of the LC filter is important. If this is too low, output noise will increase. If the Q factor is too high, then peaking may occur at high signal frequencies, reducing the pass-band flatness. The Q value is calculated as:

$$Q = \frac{R}{\sqrt{\frac{L}{C}}}$$

Where R is the load (speaker) resistance.

Use an LC filter with a Q between 0.7 and 2. The actual output ripple and noise is greatly affected by the type of inductor and capacitor used in the LC filter. Use a film capacitor and an inductor with sufficient power handling capability to supply the output current to the load. The inductor should exhibit soft saturation characteristics. If the inductor exhibits hard saturation, it should operate well below the saturation current. Gapped ferrite, MPP, Powdered Iron or similar type toroidal cores are recommended. If open or shielded bobbin ferrite cores are used, make sure that the start windings of each inductor line up (all starts going toward SW pin or all starts going toward the output) to prevent crosstalk or other channel-to-channel interference.

### Input Coupling Capacitor

The input coupling capacitors, C6 and C9, are used to pass only the AC audio signal to the input of the amplifier. In a typical system application, the source input signal is usually centered around the circuit ground, while the MP7782 input is at half the power supply voltage ($V_{DD}/2$). The input coupling capacitor transmits the AC signal from the source to the MP7782 while blocking the DC voltage. This input coupling capacitor creates a low-pass filter with the input resistor of the MP7782. Choose an input coupling capacitor such that the corner frequency ($f_{IN}$) is less than the desired pass-band frequency.

The formula for the corner frequency is:

$$f_{IN} = \frac{1}{2\pi \times R3 \times C6}$$

$$R4 = R3$$

$$C9 = C6$$

Where $f_{IN}$ is the -3dB cutoff frequency, R3 and R6 are the input resistors and C6 and C9 are the input AC coupling capacitors.

### Power Source

For maximum output power, the amplifier circuit requires a regulated external power source to supply power to the amplifier. The higher the power supply voltage provided, the more power that can be delivered to a given load resistance. However, if the power source voltage exceeds the maximum operating voltage of 24V, the MP7782 may sustain damage.

The power supply rejection of the MP7782 is excellent; however, noise at the power supply can get to the output, so care must be taken to minimize power supply noise within the pass-band frequencies. Bypass the power supply pins with a large electrolytic capacitor (typically aluminum electrolytic) along with smaller 1µF ceramic capacitors at the MP7782 $V_{DD}$ supply pins.

**Circuit Layout**

Proper circuit layout is critical for optimum performance and low output distortion and noise. Place the following components as close to the MP7782 as possible:

1. Power Supply Bypass, C3, C8

C3 and C8 carry the transient current for the switching power stage. Place a 1µF power supply bypass capacitor as close to pin 18 (VDD1) and pin 20 (PGND1) as possible. Also place a 1µF power supply bypass capacitor as close to pin 13 (VDD2) and pin 15 (PGND2) as possible.

2. Output Catch Diodes, D3A, D3B, D5A, D5B

D3A, D3B, D5A, and D5B carry the current over the dead-time while the MOSFET switches are off. Place D3A between pin 19 (SW1) and pin 20 (PGND1) to prevent the voltage at SW1 from swinging excessively below ground, and place D3B between SW2 and pin 18 (VDD1) to prevent the voltage at SW1 from swinging excessively above $V_{DD}$. Place D5A and D5B similarly to minimize the overshoot and undershoot of SW2 node.

3. Input Modulator Capacitors, C4

C4 is used to set the amplifier switching frequency. Place C4 as close to the differential inputs, pin 2 and pin 3, as possible to reduce distortion and noise.

4. Electro-Magnetic Interference (EMI)

Due to the switching nature of the Class D amplifier, care must be taken to minimize the effects of electromagnetic interference from the amplifier. However, with proper component selection and careful attention to circuit layout, the effects of EMI due to the amplifier switching can be minimized.

The power inductors are a potential source of radiated emissions. For the best EMI performance use shielded inductors since the magnetic field is well contained inside the core.

On the system printed circuit board, trace loops that carry rapidly changing currents need to be minimized. $V_{DD}$ bypass capacitors (C3 and C8) must be placed as close to the MP7782 as possible.

Nodes that carry rapidly changing voltage, such as SW1 and SW2, must be made as small as possible. If sensitive traces run near SW1 or SW2, place a ground shield between the traces.

**Power Dissipation and Thermal Considerations**

The power dissipation of the MP7782 arises mostly from the conduction loss of the internal main switches. This power loss is estimated to be:

$$P_{LOSS} \cong \frac{P_{OUT}}{R_L} \times 2 \times 0.18\Omega \times 1.3$$

Where 1.3 is a temperature coefficient factor that reflects the increase in the $R_{DS(ON)}$ resistance at elevated temperatures.

For example, for a 6Ω speaker, the max $P_{OUT}$ is 50W:

$$P_{LOSS} \cong \frac{50}{6} \times 2 \times 0.18\Omega \times 1.3 = 3.9W$$

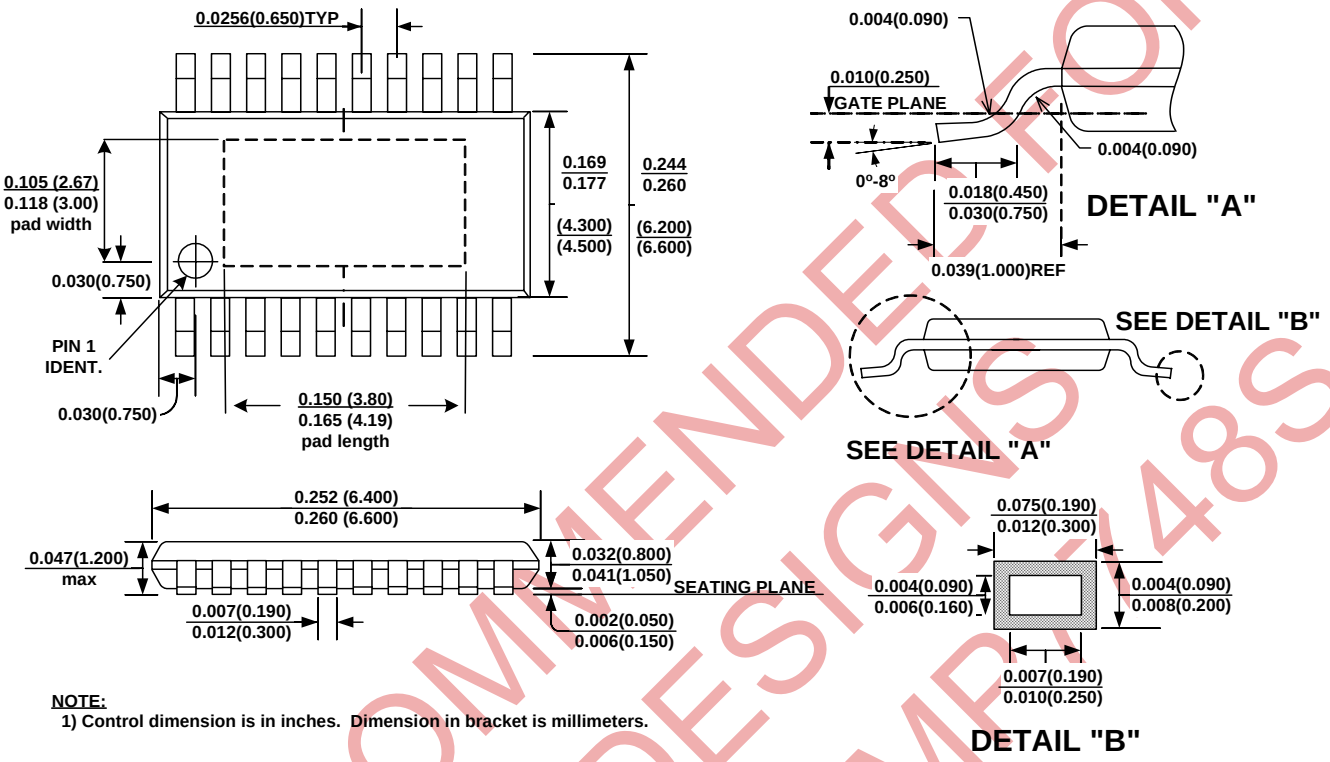
Because the thermal resistance $\theta_{JC}$ is 6°C/W, the resulting temperature rise between junction and case is approximately 24°C.

Therefore, caution must be exercised when using the MP7782 in applications with continuous high output power.

A heat sink is required if the MP7782 is applied at continuous 50W output power.

## PACKAGE INFORMATION

### TSSOP20F (EXPOSED PAD)




**NOTE:**
1) Control dimension is in inches. Dimension in bracket is millimeters.

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