OP470–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (at V_S = ±15 V, T_A = 25°C, unless otherwise noted.)

			OP470A/E			OP470F			OP470G			
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
INPUT OFFSET VOLTAGE	V_{OS}			0.1	0.4		0.2	0.8		0.4	1.0	mV
INPUT OFFSET CURRENT	I_{OS}	V_{CM} = 0 V		3	10		6	20		12	30	nA
INPUT BIAS CURRENT	I_B	V_{CM} = 0 V		6	25		15	50		25	60	nA
INPUT NOISE VOLTAGE	e_{np-p}	0.1 Hz to 10 Hz (Note 1)		80	200		80	200		80	200	nV p-p
INPUT NOISE Voltage Density	e_n	f_O = 10 Hz f_O = 100 Hz f_O = 1 kHz (Note 2)		3.8 3.3 3.2	6.5 5.5 5.0		3.8 3.3 3.2	6.5 5.5 5.0		3.8 3.3 3.2	6.5 5.5 5.0	nV$\sqrt{Hz}$
INPUT NOISE Current Density	i_n	f_O = 10 Hz f_O = 100 Hz f_O = 1 kHz		1.7 0.7 0.4			1.7 0.7 0.4			1.7 0 7 0.4		pA$\sqrt{Hz}$
LARGE-SIGNAL Voltage Gain	A_{VO}	V = ±10 V R_L = 10 kΩ R_L = 2 kΩ	 1000 500	 2300 1200		 800 400	 1700 900		 800 400	 1700 900		V/mV
INPUT VOLTAGE RANGE	IVR	(Note 3)	±11	±12		±11	±12		±11	±12		V
OUTPUT VOLTAGE SWING	V_O	$R_L \geq 2$ kΩ	±12	±13		±12	±13		±12	±13		V
COMMON-MODE REJECTION	CMR	V_{CM} = ±11 V	110	125		100	120		100	120		dB
POWER SUPPLY REJECTION RATIO	PSRR	V_S = ±4.5 V to ±18 V		0.56	1.8		1.0	5.6		1.0	5.6	µV/V
SLEW RATE	SR		1.4	2		1.4	2		1.4	2		V/µs
SUPPLY CURRENT (All Amplifiers)	I_{SY}	No Load		9	11		9	11		9	11	mA
GAIN BANDWIDTH PRODUCT	GBW	A_V = 10		6			6			6		MHz
CHANNEL SEPARATION	CS	V_O = 20 V p-p f_O = 10 Hz (Note 1)	125	155		125	155		125	155		dB
INPUT CAPACITANCE	C_{IN}			2			2			2		pF
INPUT RESISTANCE Differential-Mode	R_{IN}			0.4			0.4			0.4		MΩ
INPUT RESISTANCE Common-Mode	R_{INCM}			11			11			11		GΩ
SETTLING TIME	t_S	A_V = 1 to 0.1% to 0.01 %		 5.5 6.0			 5.5 6.0			 5.5 6.0		µs

NOTES
[1]Guaranteed but not 100% tested
[2]Sample tested
[3]Guaranteed by CMR test

ELECTRICAL CHARACTERISTICS (at V_S = ±15 V, –55°C ≤ T_A ≤ 125°C for OP470A, unless otherwise noted.)

Parameter	Symbol	Conditions	OP470A Min	OP470A Typ	OP470A Max	Unit
INPUT OFFSET VOLTAGE	V_{OS}			0.14	0.6	mV
AVERAGE INPUT Offset Voltage Drift	TCV_{OS}			0.4	2	µV/°C
INPUT OFFSET CURRENT	I_{OS}	V_{CM} = 0 V		5	20	nA
INPUT BIAS CURRENT	I_B	V_{CM} = 0 V		15	20	nA
LARGE-SIGNAL Voltage Gain	A_{VO}	V_O = ±10 V R_L = 10 kΩ R_L = 2 kΩ	 750 400	 1600 800		V/mV
INPUT VOLTAGE RANGE*	IVR		±11	±12		V
OUTPUT VOLTAGE SWING	V_O	R_L ≥ 2 kΩ	±12	±13		V
COMMON-MODE REJECTION	CMR	V_{CM} = ±11 V	100	120		dB
POWER SUPPLY REJECTION RATIO	PSRR	V_S = ±4.5 V to ±18 V		1.0	5.6	µV/V
SUPPLY CURRENT (All Amplifiers)	I_{SY}	No Load	—	9.2	11	mA

*Guaranteed by CMR test

ELECTRICAL CHARACTERISTICS (at V_S = ±15 V, –25°C ≤ T_A ≤ 85°C for OP470E/OP470EF, –40°C ≤ T_A ≤ 85°C for OP470G, unless otherwise noted.)

Parameter	Symbol	Conditions	OP470E Min	OP470E Typ	OP470E Max	OP470F Min	OP470F Typ	OP470F Max	OP470G Min	OP470G Typ	OP470G Max	Unit
INPUT OFFSET VOLTAGE	V_{OS}			0.12	0.5		0.24	1.0		0.5	1.5	mV
AVERAGE INPUT Offset Voltage Drift	TCV_{OS}			0.4	2		0.6	4		2		µV/°C
INPUT OFFSET CURRENT	I_{OS}	V_{CM} = 0 V		4	20		7	40		20	50	nA
INPUT BIAS CURRENT	I_B	V_{CM} = 0 V		11	50		20	70		40	75	nA
LARGE-SIGNAL Voltage Gain	A_{VO}	V_O = ±10 V R_L = 10 kΩ R_L = 2 kΩ	 800 400	 1800 900		 600 300	 1400 700		 600 300	 1500 800		V/mV
INPUT VOLTAGE RANGE*	IVR		±11	±12		±11	±12		±11	±12		V
OUTPUT VOLTAGE SWING	V_O	R_L ≥ 2 kΩ	±12	±13		±12	±13		±12	±13		V
COMMON-MODE REJECTION	CMR	V_{CM} = ±11 V	100	120		90	115		90	110		dB
POWER SUPPLY REJECTION RATIO	PSRR	V_S = ±4.5 V to ±18 V		0.7	5.6		1.8	10		1.8	10	µV/V
SUPPLY CURRENT (All Amplifiers)	I_{SY}	No Load	—	9.2	11	—	9.2	11	—	9.3	11	mA

*Guaranteed by CMR test

OP470–SPECIFICATIONS

WAFER TEST LIMITS (at V_S = ±15 V, 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	OP470GBC Limit	Unit
INPUT OFFSET VOLTAGE	V_{OS}		0.8	mV Max
INPUT OFFSET CURRENT	I_{OS}	V_{CM} = 0 V	20	nA Max
INPUT BIAS CURRENT	I_B	V_{CM} = 0 V	50	nA Min
LARGE-SIGNAL Voltage Gain	A_{VO}	V_O = ±10 V R_L = 10 kΩ R_L = 2 kΩ	 800 400	V/mV Min
INPUT VOLTAGE RANGE*	IVR		±11	V Min
OUTPUT VOLTAGE SWING	V_O	$R_L \geq 2$ kΩ	±12	V Min
COMMON-MODE REJECTION	CMR	V_{CM} = ±11 V	100	dB
POWER SUPPLY REJECTION RATIO	PSRR	V_S = ±4.5 V to ±18 V	5.6	µV/V Max
SUPPLY CURRENT (All Amplifiers)	I_{SY}	No Load	11	mA Max

NOTE
*Guaranteed by CMR test

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Differential Input Voltage[2] . . . . . ±1.0 V
Differential Input Current[2] . . . . . ±25 mA
Input Voltage . . . . . Supply Voltage
Output Short-Circuit Duration . . . . . Continuous
Storage Temperature Range
P, Y Package . . . . . –65°C to +150°C
Lead Temperature Range (Soldering 60 sec) . . . . . 300°C
Junction Temperature (T_j) . . . . . –65°C to +150°C
Operating Temperature Range
OP470A . . . . . –55°C to +125°C
OP470E, OP470F . . . . . –25°C to +85°C
OP470G . . . . . –40°C to +85°C

Package Type	θ_{JA}[3]	θ_{JC}	Unit
14-Lead Hermetic DIP(Y)	94	10	°C/W
14-Lead Plastic DIP(P)	76	33	°C/W
16-Lead SOIC (S)	88	23	°C/W

NOTES
[1]Absolute Maximum Ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]The OP470's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise performance. If differential voltage exceeds ±1.0 V, the input current should be limited to ±25 mA.
[3]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for TO, CerDIP, PDIP, packages; θ_{JA} is specified for device soldered to printed circuit board for SOIC packages.

ORDERING GUIDE

T_A = 25°C V_{OS} max (μV)	Package Options		Operating Temperature Range
	Cerdip 14-Pin	Plastic	
400			MIL
400	OP470AY*		MIL
400	OP470EY		IND
800	OP470FY*		IND
1000		OP470GP	XIND
1000		OP470GS	XIND

*Not for new design; obsolete April 2002.

For military processed devices, please refer to the standard Microcircuit Drawing (SMD) available at www.dscc.dla.mil/programs/milspec/default.asp

SMD Part Number	ADI Equivalent
59628856501CA	OP470AYMDA
596288565012A	OP470ARCMDA
596288565013A*	OP470ATCMDA

*Not for new designs; obsolete April 2002.

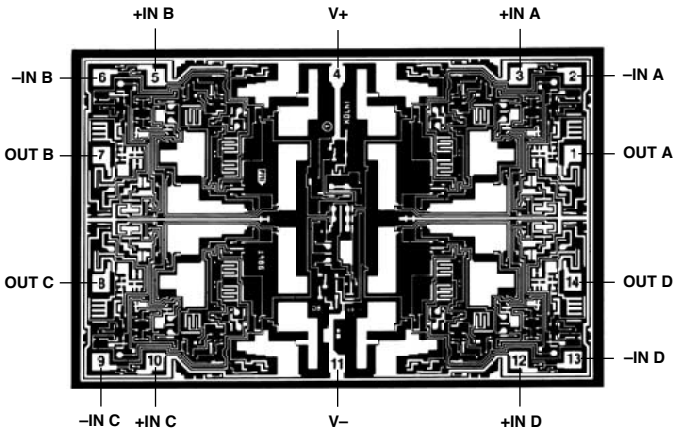
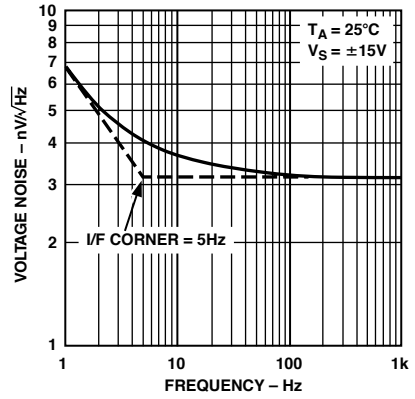


Figure 1. Dice Characteristics

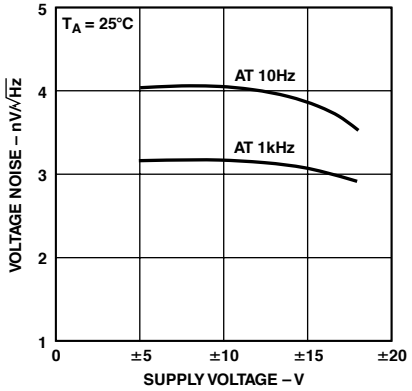
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP470 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

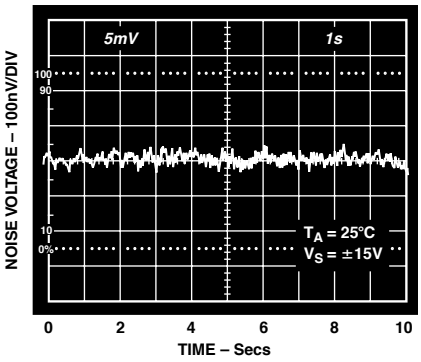
OP470–Typical Performance Characteristics



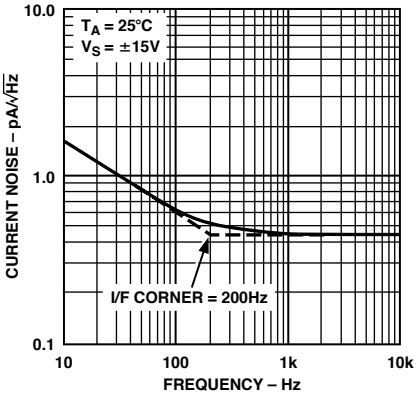
TPC 1. Voltage Noise Density vs. Frequency



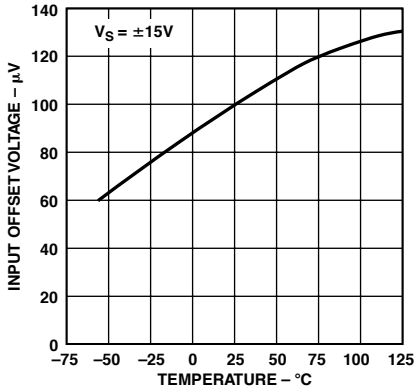
TPC 2. Voltage Noise Density vs. Supply Voltage



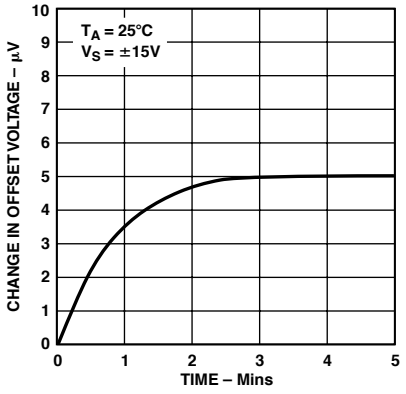
TPC 3. 0.1 Hz to 10 Hz Noise



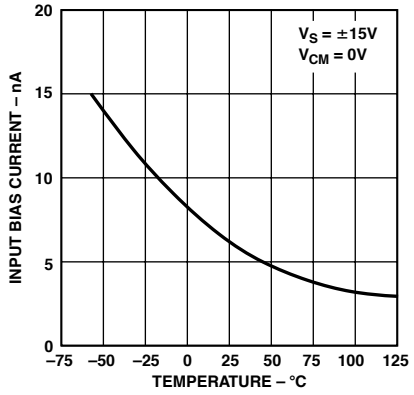
TPC 4. Current Noise Density vs. Frequency



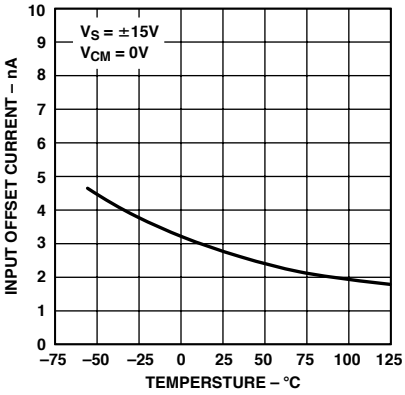
TPC 5. Input Offset Voltage vs. Temperature



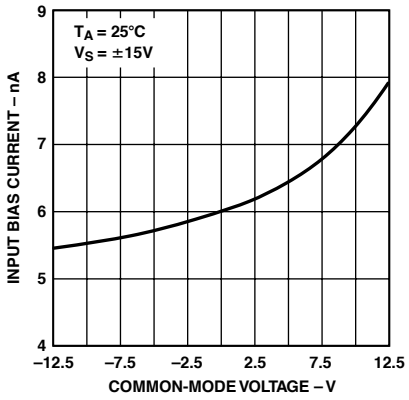
TPC 6. Warm-Up Offset Voltage Drift



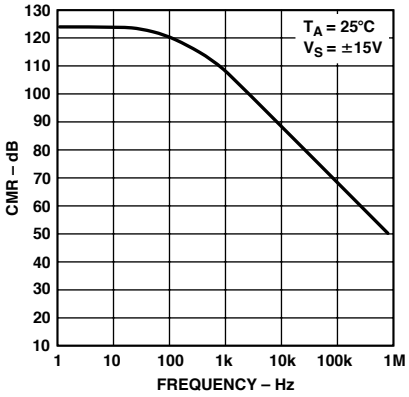
TPC 7. Input Bias Current vs. Temperature



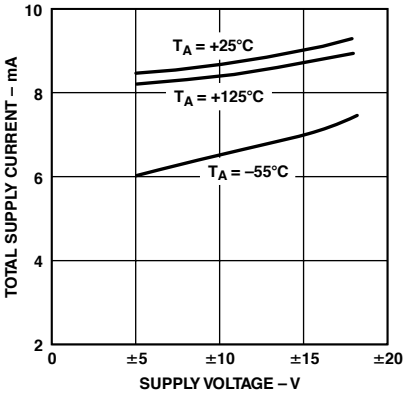
TPC 8. Input Offset Current vs. Temperature



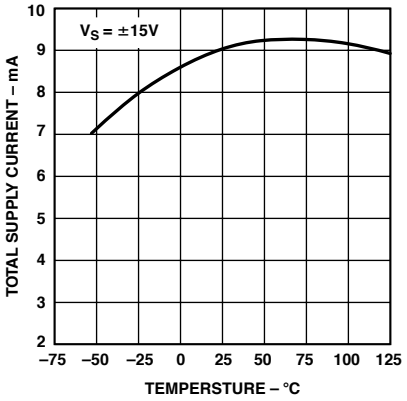
TPC 9. Input Bias Current vs. Common-Mode Voltage



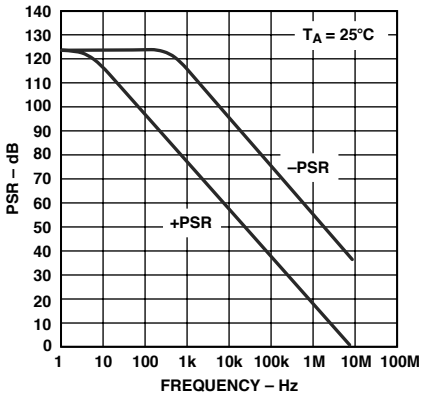
TPC 10. CMR vs. Frequency



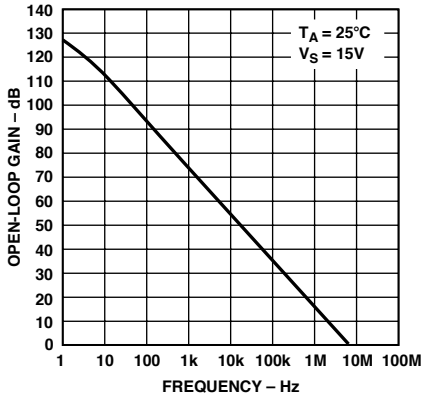
TPC 11. Total Supply Current vs. Supply Voltage



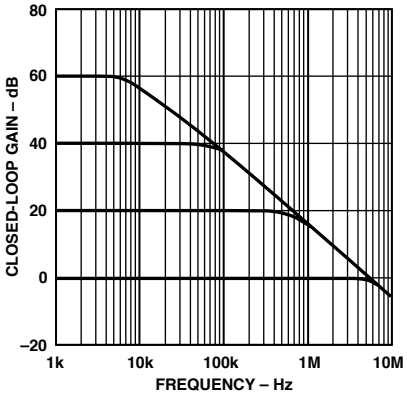
TPC 12. Total Supply Current vs. Supply Voltage



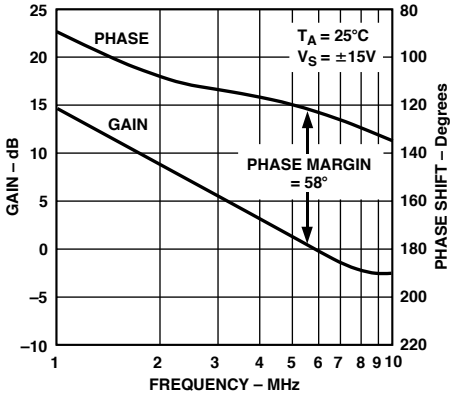
TPC 13. PSR vs. Frequency



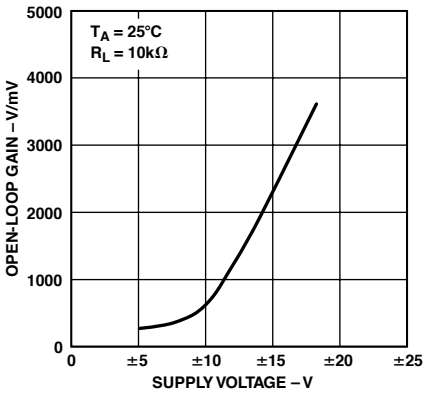
TPC 14. Open-Loop Gain vs. Frequency



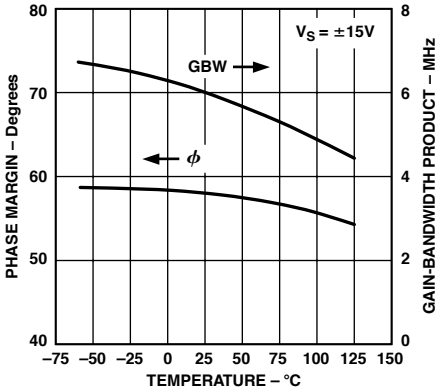
TPC 15. Closed-Loop Gain vs. Frequency



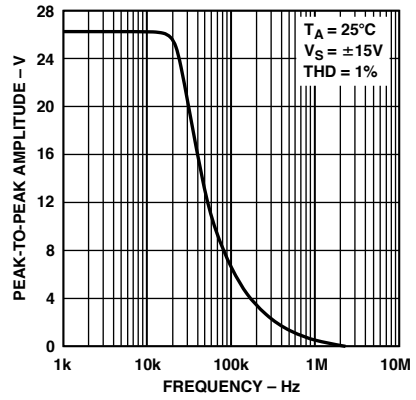
TPC 16. Open-Loop Gain, Phase Shift vs. Frequency



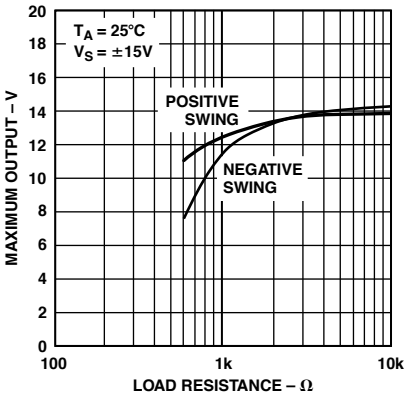
TPC 17. Open-Loop Gain vs. Supply Voltage



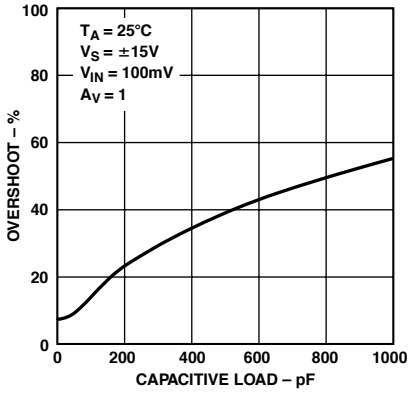
TPC 18. Gain-Bandwidth Product, Phase Margin vs. Temperature



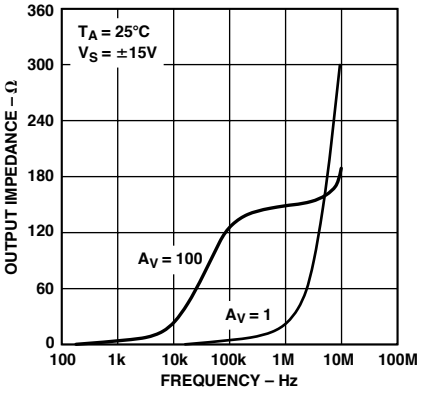
TPC 19. Maximum Output Swing vs. Frequency



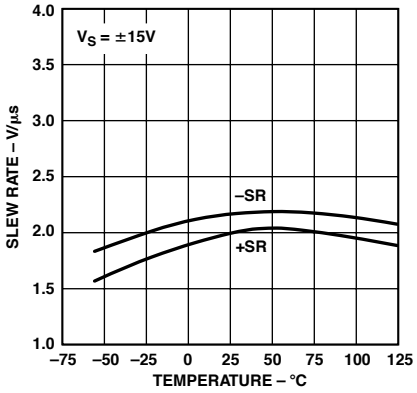
TPC 20. Maximum Output Voltage vs. Load Resistance



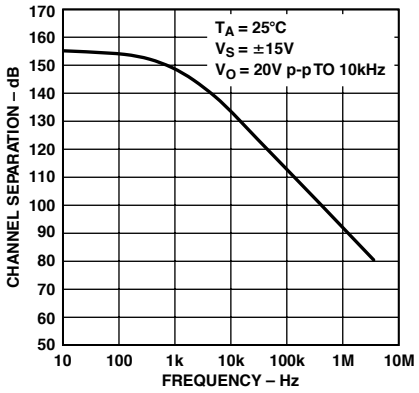
TPC 21. Small-Signal Overshoot vs. Capacitive Load



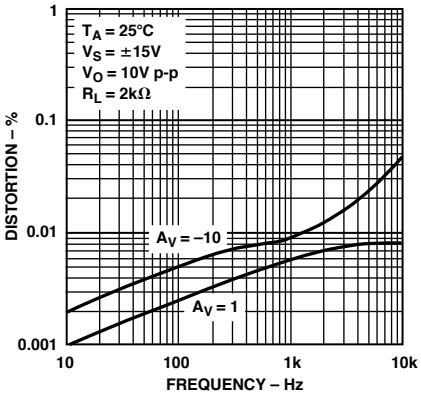
TPC 22. Output Impedance vs. Frequency



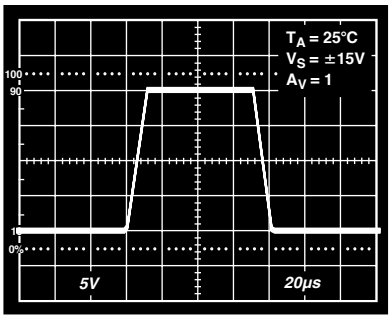
TPC 23. Slew Rate vs. Temperature



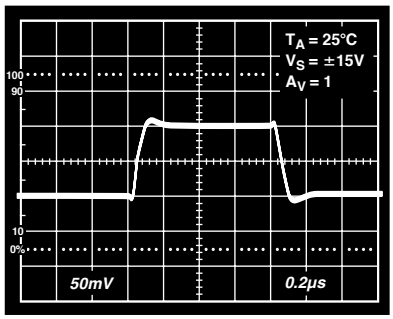
TPC 24. Channel Separation vs. Frequency



TPC 25. Total Harmonic Distortion vs. Frequency



TPC 26. Large-Signal Transient Response



TPC 27. Small-Signal Transient Response

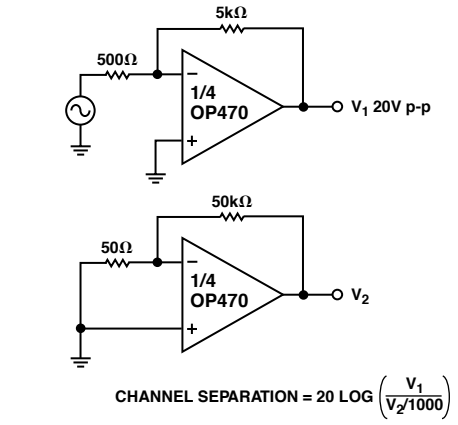


Figure 2. Channel Separation Test Circuit

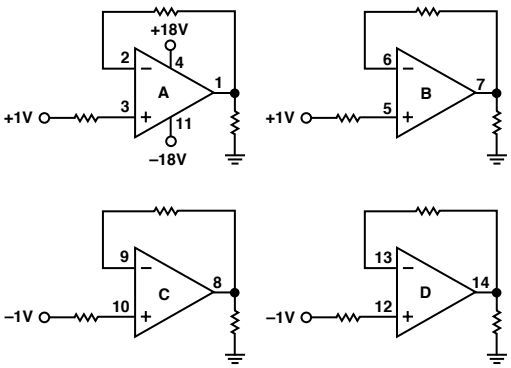


Figure 3. Burn-In Circuit

APPLICATIONS INFORMATION

Voltage and Current Noise

The OP470 is a very low-noise quad op amp, exhibiting a typical voltage noise of only 3.2 nV$\sqrt{\text{Hz}}$ @ 1 kHz. The exceptionally low-noise characteristics of the OP470 are in part achieved by operating the input transistors at high collector currents since the voltage noise is inversely proportional to the square root of the collector current. Current noise, however, is directly proportional to the square root of the collector current. As a result, the outstanding voltage noise performance of the OP470 is gained at the expense of current noise performance, which is typical for low noise amplifiers.

To obtain the best noise performance in a circuit, it is vital to understand the relationship between voltage noise (e_n), current noise (i_n), and resistor noise (e_t).

TOTAL NOISE AND SOURCE RESISTANCE

The total noise of an op amp can be calculated by:

$$E_n = \sqrt{(e_n)^2 + (i_n R_S)^2 + (e_t)^2}$$

where:

E_n = total input referred noise
e_n = up amp voltage noise
i_n = op amp current noise
e_t = source resistance thermal noise
R_S = source resistance

The total noise is referred to the input and at the output would be amplified by the circuit gain. Figure 4 shows the relationship between total noise at 1 kHz and source resistance. For $R_S < 1$ kΩ the total noise is dominated by the voltage noise of the OP470. As R_S rises above 1 kΩ, total noise increases and is dominated by resistor noise rather than by voltage or current noise of the OP470. When R_S exceeds 20 kΩ, current noise of the OP470 becomes the major contributor to total noise.

Figure 5 also shows the relationship between total noise and source resistance, but at 10 Hz. Total noise increases more quickly than shown in Figure 4 because current noise is inversely proportional to the square root of frequency. In Figure 5, current noise of the OP470 dominates the total noise when $R_S > 5$ kΩ.

From Figures 4 and 5 it can be seen that to reduce total noise, source resistance must be kept to a minimum. In applications with a high source resistance, the OP400, with lower current noise than the OP470, will provide lower total noise.

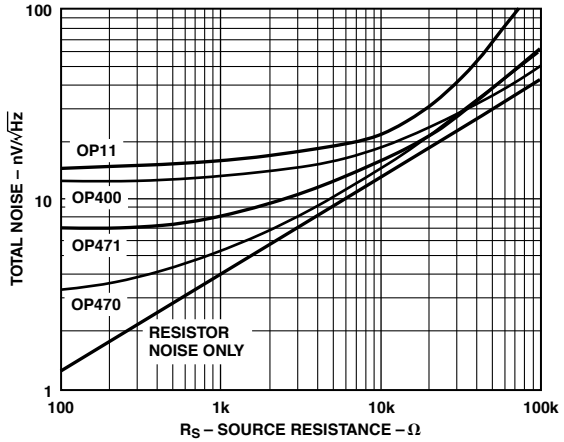


Figure 4. Total Noise vs. Source Resistance (Including Resistor Noise) at 1 kHz

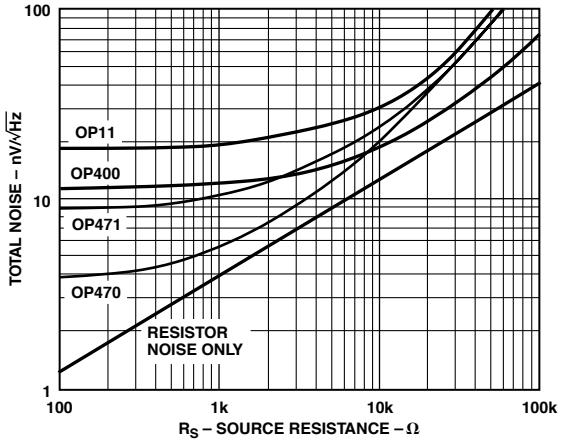


Figure 5. Total Noise vs. Source Resistance (Including Resistor Noise) at 10 Hz

Figure 6 shows peak-to-peak noise versus source resistance over the 0.1 Hz to 10 Hz range. Once again, at low values of R_S, the voltage noise of the OP470 is the major contributor to peak-to-peak noise with current noise the major contributor as R_S increases. The crossover point between the OP470 and the OP400 for peak-to-peak noise is at R_S = 17 kΩ.

The OP471 is a higher speed version of the OP470, with a slew rate of 8 V/μs. Noise of the OP471 is only slightly higher than the OP470. Like the OP470, the OP471 is unity-gain stable.

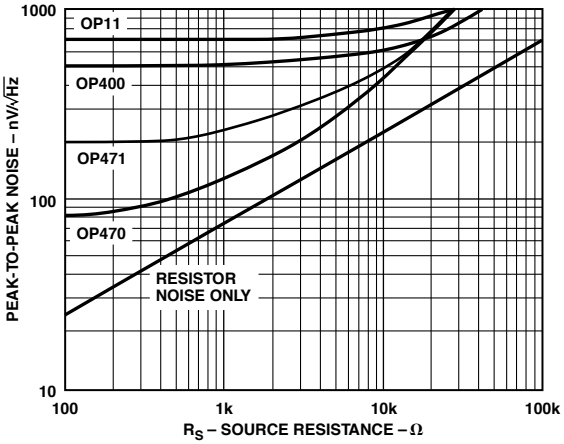


Figure 6. Peak-To-Peak Noise (0.1 Hz to 10 Hz) vs. Source Resistance (Includes Resistor Noise)

For reference, typical source resistances of some signal sources are listed in Table I.

Table I.

Source	Device Impedance	Comments
Strain gage	<500 Ω	Typically used in low frequency applications.
Magnetic tapehead	<1500 Ω	Low I_B very important to reduce self-magnetization problems when direct coupling is used. OP470 I_B can be neglected.
Magnetic phonograph cartridges	<1500 Ω	Similar need for low I_B in direct coupled applications. OP470 will not introduce any self-magnetization problem.
Linear variable differential transformer	<1500 Ω	Used in rugged servo-feedback applications. Bandwidth of interest is 400 Hz to 5 kHz.

For further information regarding noise calculations, see "Minimization of Noise in Op Amp Applications," Application Note AN-15.

NOISE MEASUREMENTS— PEAK-TO-PEAK VOLTAGE NOISE

The circuit of Figure 7 is a test setup for measuring peak-to-peak voltage noise. To measure the 200 nV peak-to-peak noise specification of the OP470 in the 0.1 Hz to 10 Hz range, the following precautions must be observed:

1. The device must be warmed up for at least five minutes. As shown in the warm-up drift curve, the offset voltage typically changes 5 μV due to increasing chip temperature after power-up. In the 10-second measurement interval, these temperature-induced effects can exceed tens of nanovolts.
2. For similar reasons, the device must be well-shielded from air currents. Shielding also minimizes thermocouple effects.
3. Sudden motion in the vicinity of the device can also "feedthrough" to increase the observed noise.

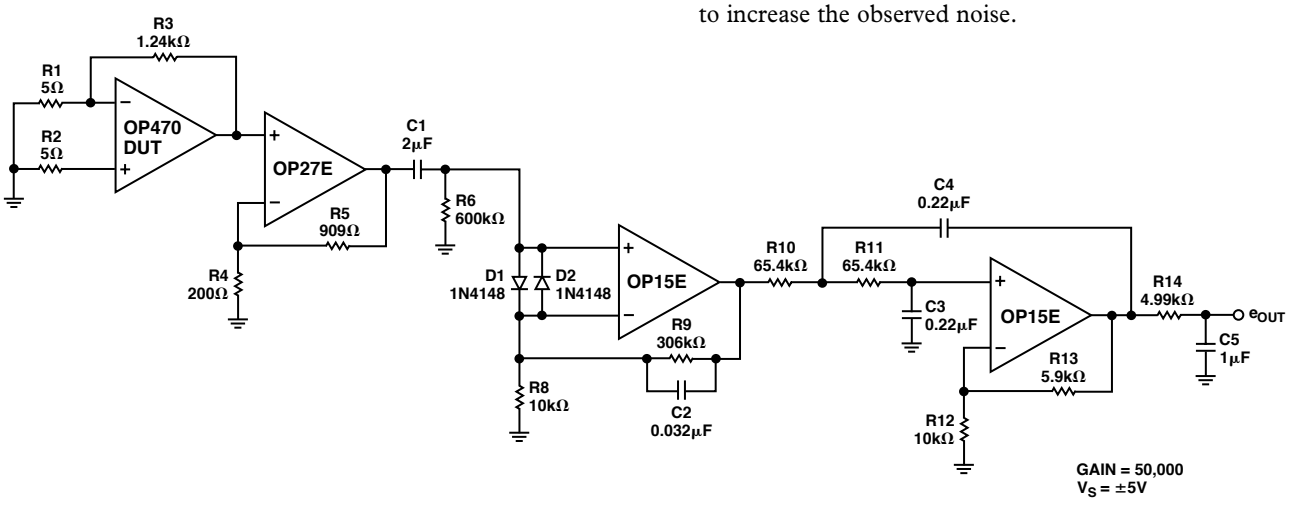


Figure 7. Peak-To-Peak Voltage Noise Test Circuit (0.1 Hz to 10 Hz)

4. The test time to measure 0.1 Hz to 10 Hz noise should not exceed 10 seconds. As shown in the noise-tester frequency-response curve of Figure 8, the 0.1 Hz corner is defined by only one pole. The test time of 10 seconds acts as an additional pole to eliminate noise contribution from the frequency band below 0.1 Hz.
5. A noise-voltage-density test is recommended when measuring noise on a large number of units. A 10 Hz noise voltage-density measurement will correlate well with a 0.1 Hz to 10 Hz peak-to-peak noise reading, since both results are determined by the white noise and the location of the 1/f corner frequency.
6. Power should be supplied to the test circuit by well bypassed low noise supplies, e.g. batteries. These will minimize output noise introduced via the amplifier supply pins.

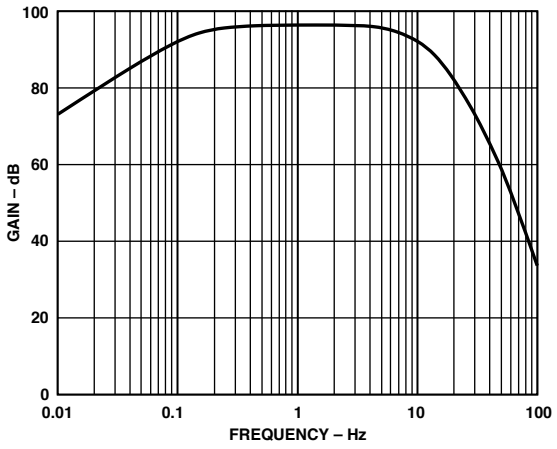


Figure 8. 0.1 Hz to 10 Hz Peak-to-Peak Voltage Noise Test Circuit Frequency Response

NOISE MEASUREMENT—NOISE VOLTAGE DENSITY

The circuit of Figure 9 shows a quick and reliable method of measuring the noise voltage density of quad op amps. Each individual amplifier is series-connected and is in unity-gain, save the final amplifier which is in a noninverting gain of 101. Since the ac noise voltages of each amplifier are uncorrelated, they add in rms fashion to yield:

$$e_{OUT} = 101\left(\sqrt{e_{nA}^{\ 2} + e_{nB}^{\ 2} + e_{nC}^{\ 2} + e_{nD}^{\ 2}}\right)$$

The OP470 is a monolithic device with four identical amplifiers. The noise voltage density of each individual amplifier will match, giving:

$$e_{OUT} = 101\left(\sqrt{4e_n^{\ 2}}\right) = 101\left(2e_n\right)$$

NOISE MEASUREMENT—CURRENT NOISE DENSITY

The test circuit shown in Figure 10 can be used to measure current noise density. The formula relating the voltage output to current noise density is:

$$i_n = \frac{\sqrt{\left(\frac{\theta_{nOUT}}{G}\right)^2 - \left(40nV/\sqrt{Hz}\right)^2}}{R_S}$$

where:

G = gain of 10000
R_S = 100 kΩ source resistance

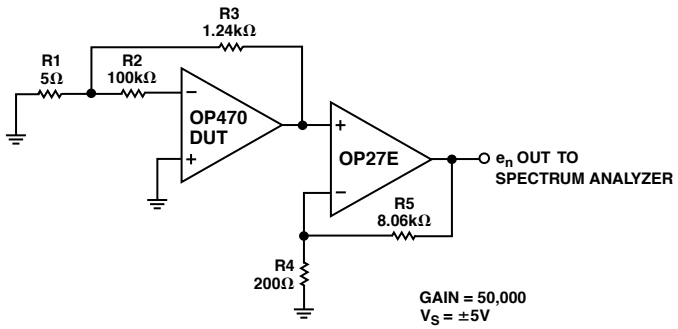


Figure 10. Current Noise Density Test Circuit

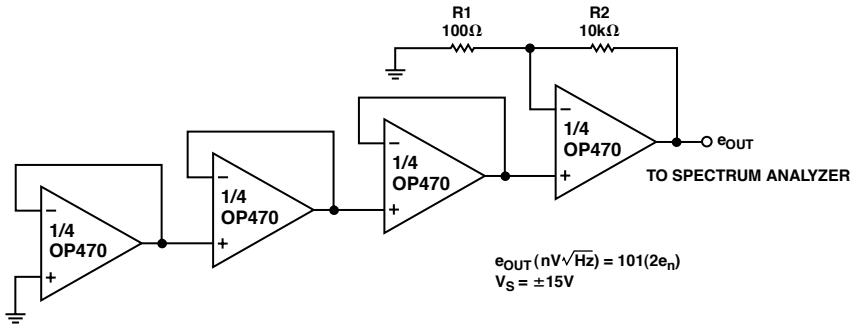


Figure 9. Noise Voltage Density Test Circuit

CAPACITIVE LOAD DRIVING AND POWER SUPPLY CONSIDERATIONS

The OP470 is unity-gain stable and is capable of driving large capacitive loads without oscillating. Nonetheless, good supply bypassing is highly recommended. Proper supply bypassing reduces problems caused by supply line noise and improves the capacitive load driving capability of the OP470.

In the standard feedback amplifier, the op amp's output resistance combines with the load capacitance to form a low pass filter that adds phase shift in the feedback network and reduces stability. A simple circuit to eliminate this effect is shown in Figure 11. The added components, C1 and R3, decouple the amplifier from the load capacitance and provide additional stability. The values of C1 and R3 shown in Figure 11 are for a load capacitance of up to 1000 pF when used with the OP470.

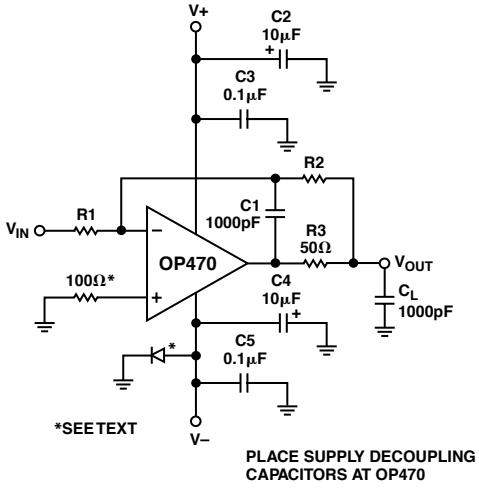


Figure 11. Driving Large Capacitive Loads

In applications where the OP470's inverting or noninverting inputs are driven by a low source impedance (under 100 Ω) or connected to ground, if V+ is applied before V–, or when V is disconnected, excessive parasitic currents will flow. Most applications use dual tracking supplies and with the device supply pins properly bypassed, power-up will not present a problem. A source resistance of at least 100 Ω in series with all inputs (Figure 11) will limit the parasitic currents to a safe level if V– is disconnected. It should be noted that any source resistance, even 100 Ω, adds noise to the circuit. Where noise is required to be kept at a minimum, a germanium or Schottky diode can be used to clamp the V- pin and eliminate the parasitic current flow instead of using series limiting resistors. For most applications, only one diode clamp is required per board or system.

UNITY-GAIN BUFFER APPLICATIONS

When Rf ≤ 100 Ω and the input is driven with a fast, large signal pulse(> 1 V), the output waveform will look as shown in Figure 12.

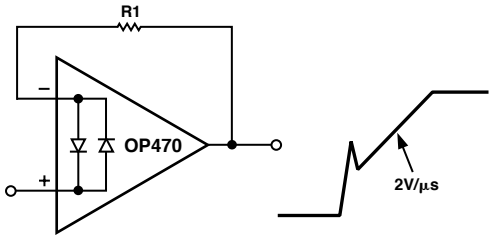


Figure 12. Pulsed Operation

During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input, and a current, limited only by the output short-circuit protection, will be drawn by the signal generator. With Rf ≤ 500 Ω, the output is capable of handling the current requirements (IL < 20 mA at 10 V); the amplifier will stay in its active mode and a smooth transition will occur.

When Rf > 3 kΩ, a pole created by Rf and the amplifier's input capacitance (2 pF) creates additional phase shift and reduces phase margin. A small capacitor (20 pF to 50 pF) in parallel with Rf helps eliminate this problem.

APPLICATIONS

Low Noise Amplifier

A simple method of reducing amplifier noise by paralleling amplifiers is shown in Figure 13. Amplifier noise, depicted in Figure 14, is around 2 nV/√Hz @ 1 kHz (R.T.I.). Gain for each paralleled amplifier and the entire circuit is 1000. The 200 Ω resistors limit circulating currents and provide an effective output resistance of 50 Ω. The amplifier is stable with a 10 nF capacitive load and can supply up to 30 mA of output drive.

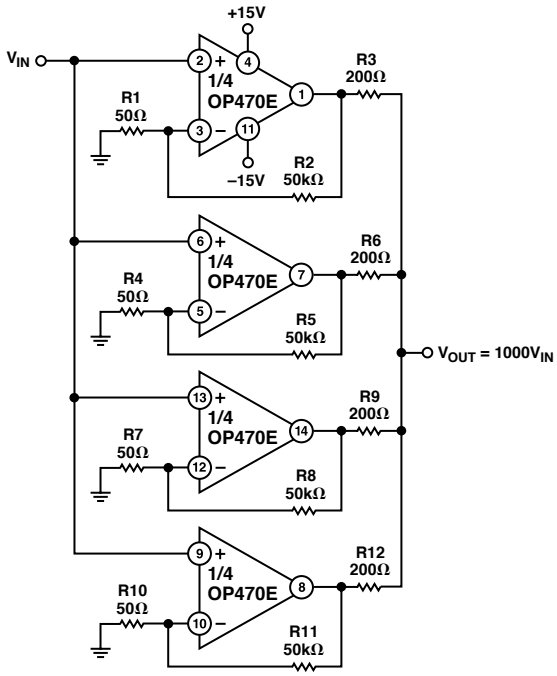


Figure 13. Low Noise Amplifier

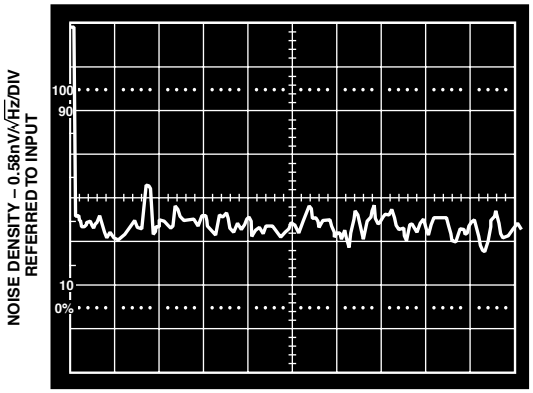


Figure 14. Noise Density of Low Noise Amplifier, G = 1000

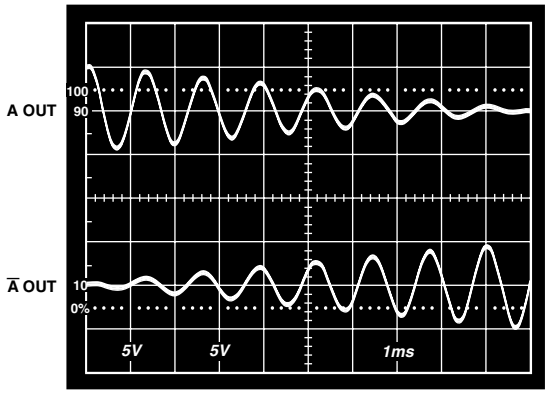


Figure 16. Digital Panning Control Output

DIGITAL PANNING CONTROL

Figure 15 uses a DAC-8408, quad 8-bit DAC to pan a signal between two channels. The complementary DAC current outputs two of the DAC-8408's four DACs drive current-to-voltage converters built from a single quad OP470. The amplifiers have complementary outputs with the amplitudes dependent upon the digital code applied to the DAC. Figure 16 shows the complementary outputs for a 1 kHz input signal and digital ramp applied to the DAC data inputs. Distortion of the digital panning control is less than 0.01%.

Gain error due to the mismatching between the internal DAC ladder resistors and the current-to-voltage feedback resistors is eliminated by using feedback resistors internal to the DAC. Of the four DACs available in the DAC-8408, only two DACs, A and C, actually pass a signal. DACs B and D are used to provide the additional feedback resistors needed in the circuit. If the VREFB and VREFD inputs remain unconnected, the current-to-voltage converters using RFBB and RFBD are unaffected by digital data reaching DACs B and D.

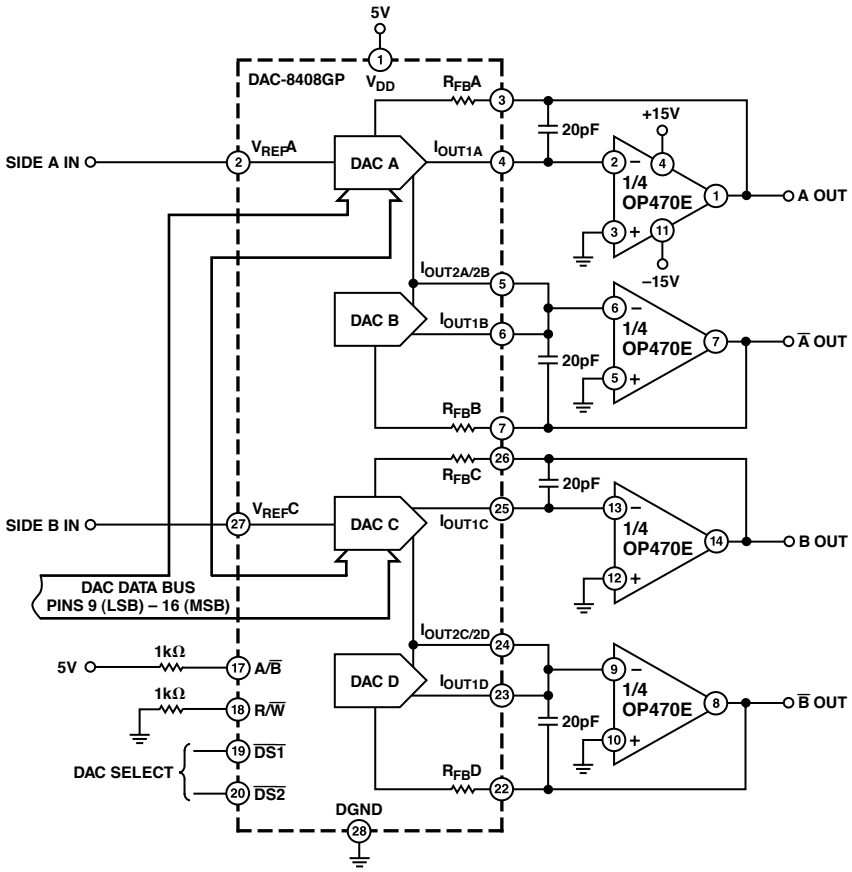


Figure 15. Digital Panning Control Circuit

SQUELCH AMPLIFIER

The circuit of Figure 17 is a simple squelch amplifier that uses a FET switch to cut off the output when the input signal falls below a preset limit.

The input signal is sampled by a peak detector with a time constant set by C1 and R6. When the output of the peak detector (Vp), falls below the threshold voltage, (VTH), set by R8, the comparator formed by op amp C switches from V– to V+. This drives the gate of the N-channel FET high, turning it ON, reducing the gain of the inverting amplifier formed by op amp A to zero.

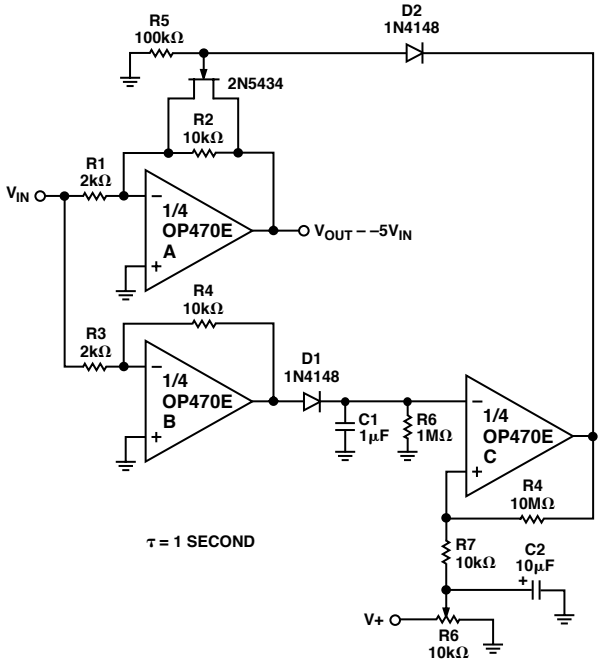


Figure 17. Squelch Amplifier

FIVE-BAND LOW-NOISE STEREO GRAPHIC EQUALIZER

The graphic equalizer circuit shown in Figure 18 provides 15 dB of boost or cut over a 5-band range. Signal-to-noise ratio over a 20 kHz bandwidth is better than 100 dB referred to a 3 V rms input. Larger inductors can be replaced by active inductors but this reduces the signal-to-noise ratio.

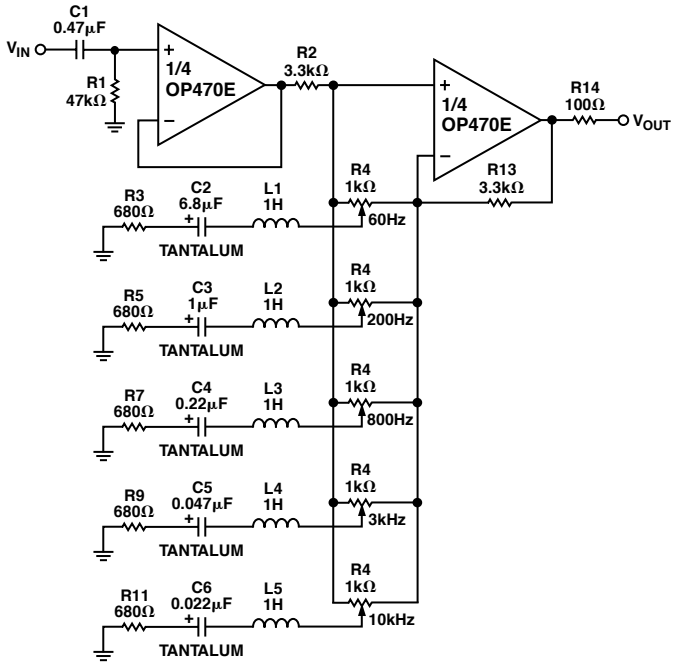
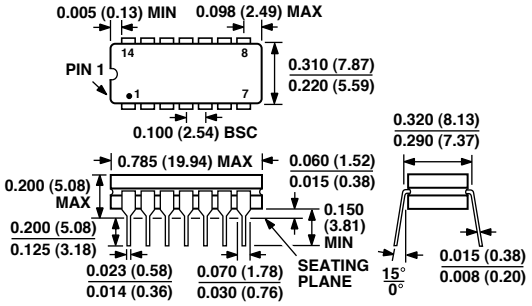


Figure 18. Five-Band Low Noise Graphic Equalizer

OUTLINE DIMENSIONS

14-Lead Ceramic Dip-Glass Hermetic Seal [CERDIP]
(Q-14)

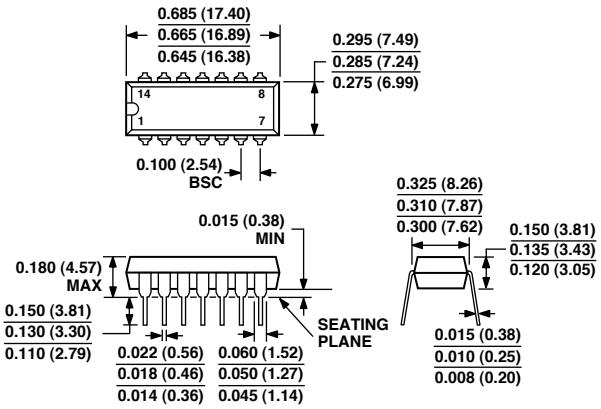
Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETERS DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

14-Lead Plastic Dual-in-Line Package [PDIP]
(N-14)

Dimensions shown in inches and (millimeters)



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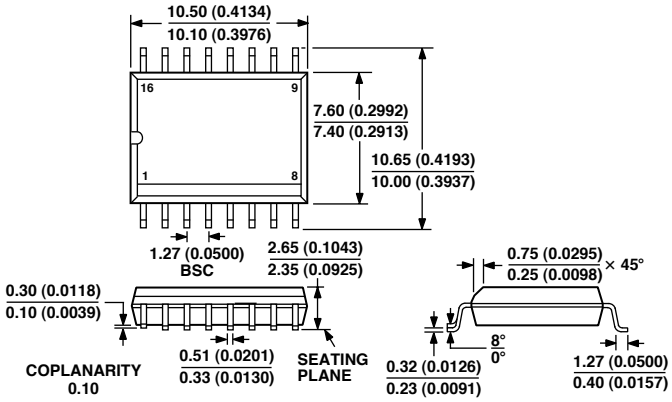
16-Lead Standard Small Outline Package [SOIC]
Wide Body
(RW-16)

Dimensions shown in millimeters and (inches)



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Revision History

Location	Page
10/02—Data Sheet changed from REV. A to REV. B.	
Edits to 16-Lead SOIC	1
Edits to ELECTRICAL CHARACTERISTICS	3
Edits to ABSOLUTE MAXIMUM RATINGS	5
Updated OUTLINE DIMENSIONS	15
4/02—Data Sheet changed from REV. 0 to REV. A.	
28-Lead LCC (RC-Suffix) deleted	1
28-Lead LCC (TC-Suffix) deleted	1
Edits to ABSOLUTE MAXIMUM RATINGS	4
Edits to ORDERING GUIDE	4
Edits to PACKAGE TYPE	4

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