

Chopper-Stabilized Op Amps

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V+ to V-).....18V
 Input Voltage(V+ + 0.3V) to (V- - 0.3V)
 Voltage on Oscillator Control Pins
 (except EXT/CLOCK IN).....V+ to V-
 Voltage on EXT/CLOCK IN(V+ + 0.3V) to (V+ - 6.0V)
 Duration of Output Short CircuitIndefinite
 Current into Any Pin10mA
 Current into Any Pin while Operating (Note 1).....100μA
 Continuous Total Power Dissipation (T_A = +70°C)
 8-Pin SO (derate 5.88mW/°C above +70°C).....471mW
 8-Pin PDIP (derate 6.9mW/°C above +70°C).....552mW
 8-Pin CERDIP (derate 8.0mW/°C above +70°C).....640mW

8-Pin TO-99 (derate 6.7mW/°C above +70°C).....533mW
 14-Pin SO (derate 8.3mW/°C above +70°C).....667mW
 14-Pin PDIP (derate 10.0mW/°C above +70°C).....800mW
 14-Pin CERDIP (derate 9.1mW/°C above +70°C).....727mW
 Operating Temperature Ranges
 ICL765_C_/ICL755_BC_0°C to +70°C
 ICL765_I_/ICL755_BI_-20°C to +85°C
 ICL765_M_/ICL755_BM_-55°C to +125°C
 Storage Temperature Range-65°C to +150°C
 Junction Temperature+150°C
 Lead Temperature (soldering, 10s)+300°C

Note 1: Maxim recommends limiting the input current to 100μA to avoid latchup problems. A value of 1mA is typically safe; however, this is not guaranteed.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—ICL7650B/ICL7653B

(Circuit of Figure 1, V+ = +5V, V- = -5V, T_A = +25°C, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|----------------------------------|--|---------------------|---------------------|------|--------|
| Input Offset Voltage | V _{OS} | T _A = +25°C | | ±0.7 | ±5 | μV |
| | | -55°C < T _A < +85°C | | ±10 | | |
| | | -55°C < T _A < +125°C | | | 5.0 | |
| Average Temperature Coefficient of Input Offset Voltage | $\frac{\Delta V_{OS}}{\Delta T}$ | T _A = +25°C | | 50 | | μV/°C |
| | | -20°C < T _A < +85°C | | 0.01 | 0.05 | |
| Input Bias Current | I _{BIAS} | Doubles every 10° | | | | pA |
| | | | | 1.5 | 10 | |
| | | | | 35 | | |
| Input Offset Current (Note 2) | I _{OS} | T _A = +25°C | | 0.5 | | pA |
| Input Resistance | R _{IN} | | | 10 ¹² | | Ω |
| Large-Signal Voltage Gain | A _{VOL} | R _L = 10kΩ | 1 • 10 ⁵ | 5 • 10 ⁸ | | V/V |
| Output Voltage Swing (Note 3) | V _{OUT} | R _L = 10kΩ | ±4.7 | ±4.85 | | V |
| | | R _L = 100kΩ | | ±4.95 | | |
| Common-Mode Voltage Range | CMVR | | -5.0 | -5.2 to +2.0 | 1.6 | V |
| Common-Mode Rejection Ratio | CMRR | CMVR = -5V to +1.6V | 120 | 130 | | dB |
| Power-Supply Rejection Ratio | PSRR | V+ to V- = ±3V to ±8V | 120 | 130 | | dB |
| Input Noise Voltage | e _{np-p} | R _S = 100Ω, f = 0 to 10Hz | | 2 | | μVp-p |
| Input Noise Current | I _n | f = 10Hz | | 0.01 | | pA/√Hz |
| Unity-Gain Bandwidth | GBW | | | 2.0 | | MHz |
| Slew Rate | SR | C _L = 50pF, R _L = 10kΩ | | 2.5 | | V/μs |
| Rise Time | t _r | | | 0.2 | | μs |
| Overshoot | | | | 20 | | % |
| Operating Supply Range | V+ to V- | | 4.5 | | 16 | V |
| Supply Current | I _{SUPP} | No load | | 2.0 | 3.5 | mA |

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ICL7650/ICL7650B/ICL7653/ICL7653B

ELECTRICAL CHARACTERISTICS—ICL7650B/ICL7653B (continued)

(Circuit of Figure 1, $V_+ = +5V$, $V_- = -5V$, $T_A = +25^\circ C$, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-----------------------------|----------|---------------------------|-----|-----|-----|---------------------------|
| Internal Chopping Frequency | f_{ch} | Pins 12–14 open (DIP) | 120 | 200 | 375 | Hz |
| Clamp On Current (Note 4) | | $R_L = 100k\Omega$ | 25 | 70 | 200 | μA |
| Clamp Off Current (Note 4) | | $-4.0V < V_{OUT} < +4.0V$ | | 1 | | pA |
| Offset Voltage vs. Time | | No load | | 100 | | $\frac{nV}{\sqrt{month}}$ |

Note 2: $I_{OS} = 2 \cdot I_{BIAS}$

Note 3: OUTPUT and CLAMP pins not connected.

Note 4: See *Output Clamp* section for details.

ELECTRICAL CHARACTERISTICS—ICL7650/ICL7653

(Circuit of Figure 1, $V_+ = +5V$, $V_- = -5V$, $T_A = +25^\circ C$, unless otherwise noted.) (Note 5)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|----------------------------------|---|--|------------------|----------------|------------------|
| Input Offset Voltage | V_{OS} | $T_A = +25^\circ C$ | ICL765_ | ± 0.7 | ± 5.0 | μV |
| | | | ICL765_B | ± 1.0 | ± 10 | |
| | | ICL765_ (Note 6) | $0^\circ C \leq T_A \leq +70^\circ C$ | ± 1.0 | ± 10 | |
| | | | $-20^\circ C \leq T_A \leq +85^\circ C$ | ± 1.0 | ± 10 | |
| | | | $-55^\circ C \leq T_A \leq +125^\circ C$ | ± 10 | ± 50 | |
| Average Temperature Coefficient of Input Offset Voltage (Note 6) | $\frac{\Delta V_{OS}}{\Delta T}$ | ICL765_B, $0^\circ C \leq T_A \leq +70^\circ C$ | | 0.01 | 0.05 | $\mu V/^\circ C$ |
| | | ICL765_ | $0^\circ C \leq T_A \leq +70^\circ C$ | 0.01 | 0.1 | |
| | | | $-20^\circ C \leq T_A \leq +85^\circ C$ | 0.01 | 0.05 | |
| | | | $-55^\circ C \leq T_A \leq +85^\circ C$ | 0.01 | 0.05 | |
| | | | $+85^\circ C \leq T_A \leq +125^\circ C$ | 0.25 | 1.5 | |
| Input Bias Current | I_B | $T_A = +25^\circ C$ | ICL765_ | 4 | 10 | pA |
| | | | ICL765_B | 12 | 20 | |
| | | ICL765_ | $0^\circ C \leq T_A \leq +70^\circ C$ | 20 | 100 | |
| | | | $-20^\circ C \leq T_A \leq +85^\circ C$ | 50 | 200 | |
| | | | $-55^\circ C \leq T_A \leq +125^\circ C$ | 0.3 | 10 | |
| Input Resistance | R_{IN} | | | 10^{12} | | Ω |
| Large-Signal Voltage Gain | A_{VOL} | $R_L = 10k\Omega$, $T_A = +25^\circ C$ | | $1 \cdot 10^8$ | $5 \cdot 10^8$ | V/V |
| | | $0^\circ C \leq T_A \leq +70^\circ C$ | | $0.5 \cdot 10^8$ | | |
| | | $-20^\circ C \leq T_A \leq +85^\circ C$ | | $0.5 \cdot 10^8$ | | |
| | | $-55^\circ C \leq T_A \leq +125^\circ C$ | | $0.2 \cdot 10^8$ | | |
| Output Voltage Swing (Note 3) | V_{OUT} | $R_L = 10k\Omega$ | | ± 4.7 | ± 4.85 | V |
| | | $R_L = 100k\Omega$ | | ± 4.95 | | |
| Common-Mode Voltage Range | CMVR | $0^\circ C \leq T_A \leq +70^\circ C$ | | -5.0 | -5.2 to +3.0 | V |
| | | $-20^\circ C \leq T_A \leq +85^\circ C$ | | -5.0 | -5.2 to +3.0 | |
| | | $-55^\circ C \leq T_A \leq +125^\circ C$ | | -4.5 | -4.0 to +3.0 | |

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ELECTRICAL CHARACTERISTICS—ICL7650/ICL7653 (continued)

(Circuit of Figure 1, $V_+ = +5V$, $V_- = -5V$, $T_A = +25^\circ C$, unless otherwise noted.) (Note 5)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|------------------------------|----------------|-------------------------------------|-----|------|-----|---------------------------|
| Common-Mode Rejection Ratio | CMRR | CMVR = -5V to +2.5V | 120 | 130 | | dB |
| Power-Supply Rejection Ratio | PSRR | V_+ to $V_- = \pm 3V$ to $\pm 8V$ | 120 | 130 | | dB |
| Input Noise Voltage | e_{np-p} | $R_S = 100\Omega$, $f = 0$ to 10Hz | | 2 | | μV_{p-p} |
| Input Noise Current | I_n | $f = 10Hz$ | | 0.01 | | pA/\sqrt{Hz} |
| Unity-Gain Bandwidth | GBW | | | 2.0 | | MHz |
| Slew Rate | SR | $C_L = 50pF$, $R_L = 10k\Omega$ | | 2.5 | | $V/\mu s$ |
| Rise Time | t_r | | | 0.2 | | μs |
| Overshoot | | | | 20 | | % |
| Operating Supply Range | V_+ to V_- | | 4.5 | | 16 | V |
| Supply Current | I_{SUPP} | No load | | 1.2 | 2.0 | mA |
| Internal Chopping Frequency | f_{CLKOUT} | Pins 13 and 14 open (DIP) | 120 | 200 | 375 | Hz |
| Clamp On Current (Note 4) | | $R_L = 100k\Omega$ | 25 | 70 | 200 | μA |
| Clamp Off Current (Note 4) | | $-4.0 \leq V_{OUT} \leq +4.0V$ | | 1 | | pA |
| Offset Voltage vs. Time | | | | 100 | | $\frac{nV}{\sqrt{month}}$ |

Note 3: OUTPUT and CLAMP pins not connected.

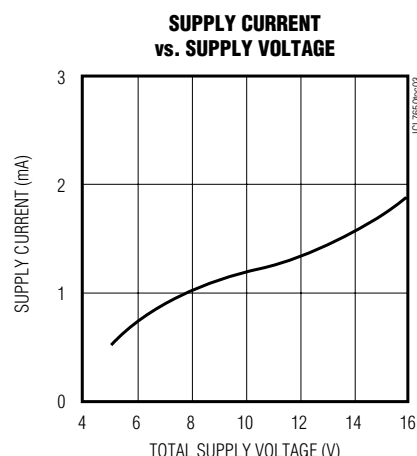
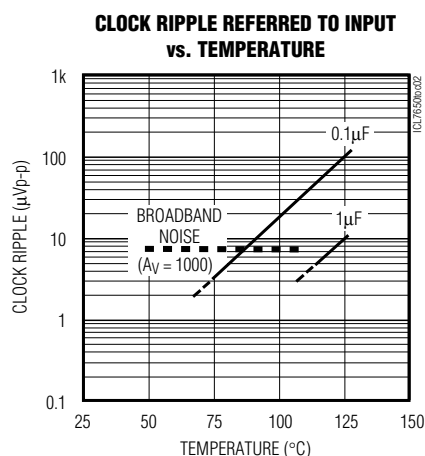
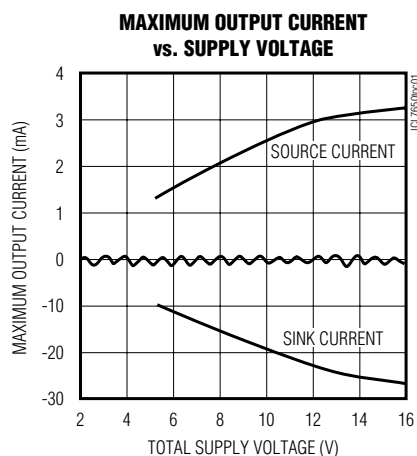
Note 4: See *Output Clamp* section for details.

Note 5: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V (MIL STD 8838 Method 3015.1 test circuit).

Note 6: Sample tested. Limits are not used to calculate outgoing quality level.

Typical Operating Characteristics

(Circuit of Figure 1, $V_+ = +5V$, $V_- = -5V$, $T_A = +25^\circ C$, unless otherwise noted.)

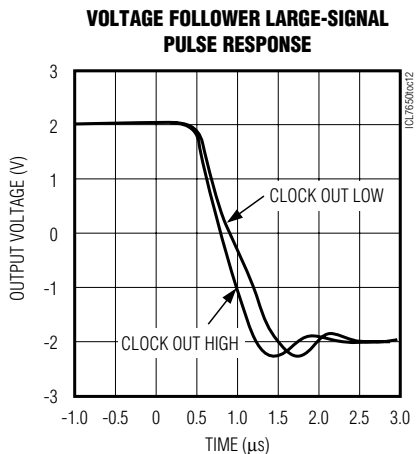
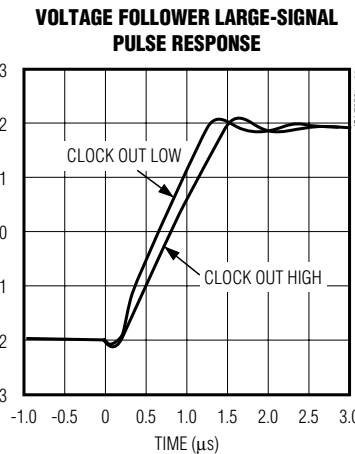
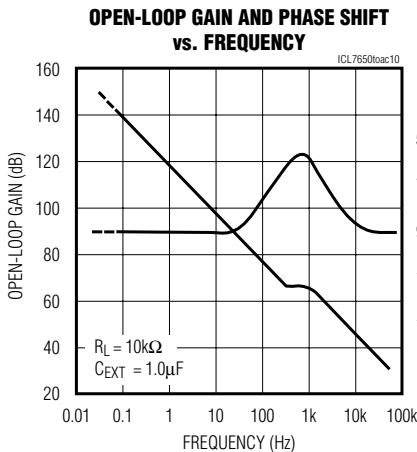
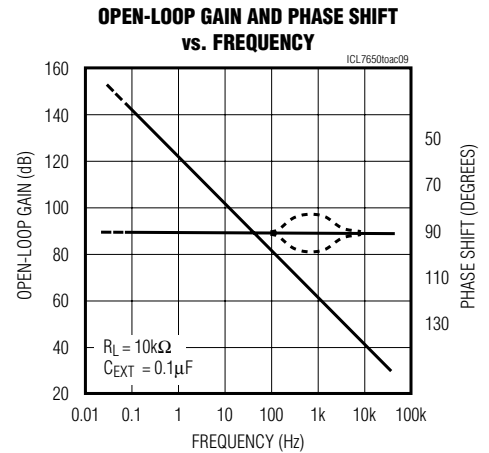
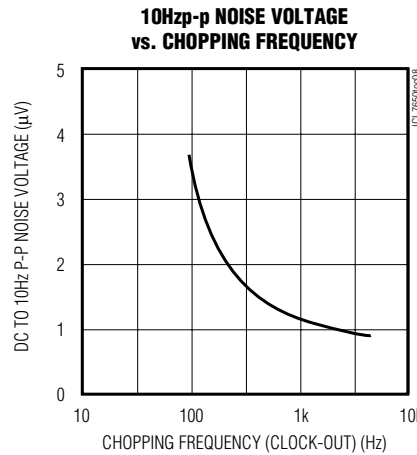
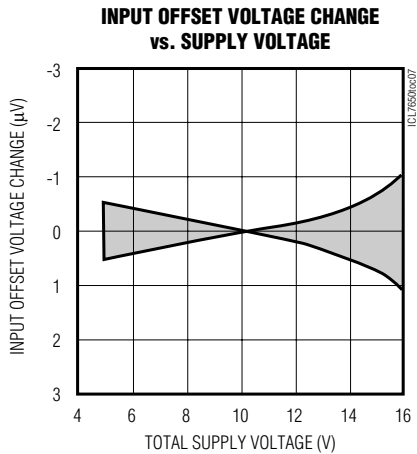
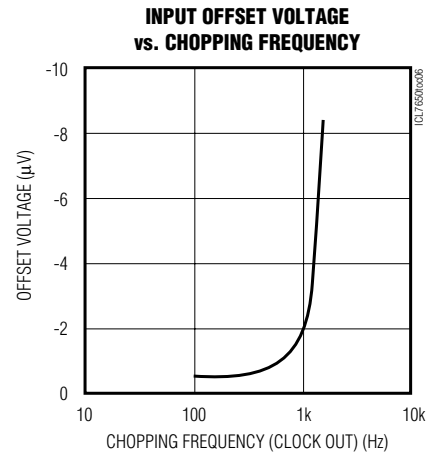
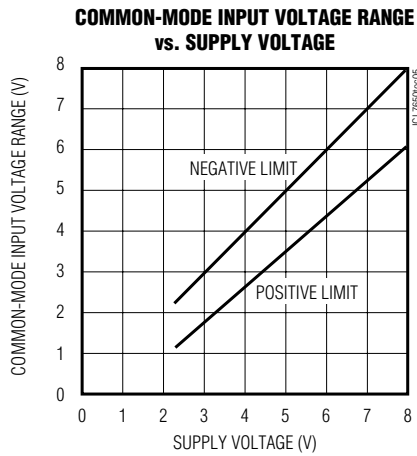
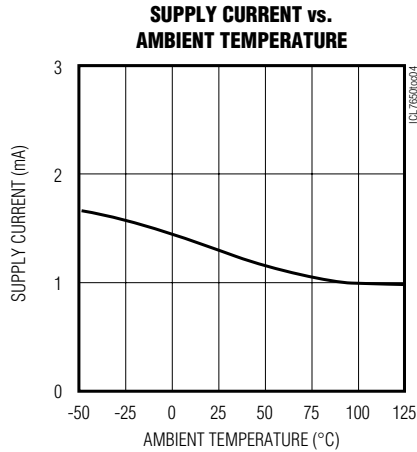


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Typical Operating Characteristics (continued)

(Circuit of Figure 1, $V_+ = +5V$, $V_- = -5V$, $T_A = +25^\circ C$, unless otherwise noted.)

ICL7650/ICL7650B/ICL7653/ICL7653B



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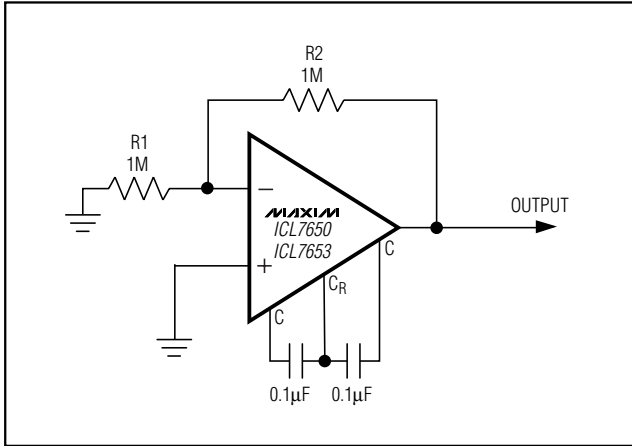


Figure 1. ICL7650 Test Circuit

Detailed Description

Figure 2 shows the major elements of the ICL7650/ICL7653. Two amplifiers are illustrated, the main amplifier and the nulling amplifier, both of which have offset-null capability. The main amplifier is connected full time from the input to the output. The nulling amplifier, under control of the chopper-frequency oscillator and clock circuit, alternately nulls itself and the main amplifier. This nulling arrangement, which is independent of the output level, operates over the full power-supply and common-mode ranges. The ICL7650/ICL7653 exhibit an exceptionally high CMRR, PSRR, and A_{VOL} . Their nulling connections, which are MOSFET back gates, have inherently high impedance. Two external capacitors provide storage for the nulling potentials and the necessary nulling-loop time constants.

The ICL7650/ICL7653 minimize chopper-frequency charge injection at the input terminals by carefully balancing the input switches. Feed-forward injection into the compensation capacitor, the main cause of output spikes in this type of circuit, is also minimized.

Output Clamp (ICL7650 Only)

The output clamp reduces the overload recovery time inherent with chopper-stabilized amplifiers. When tied to the summing junction or inverting input pin, a current path between this point and the output occurs just before the output device saturates. This prevents uncontrolled input differential and the consequent charge build-up on the correction-storage capacitors, while causing only a slight reduction in the output swing.

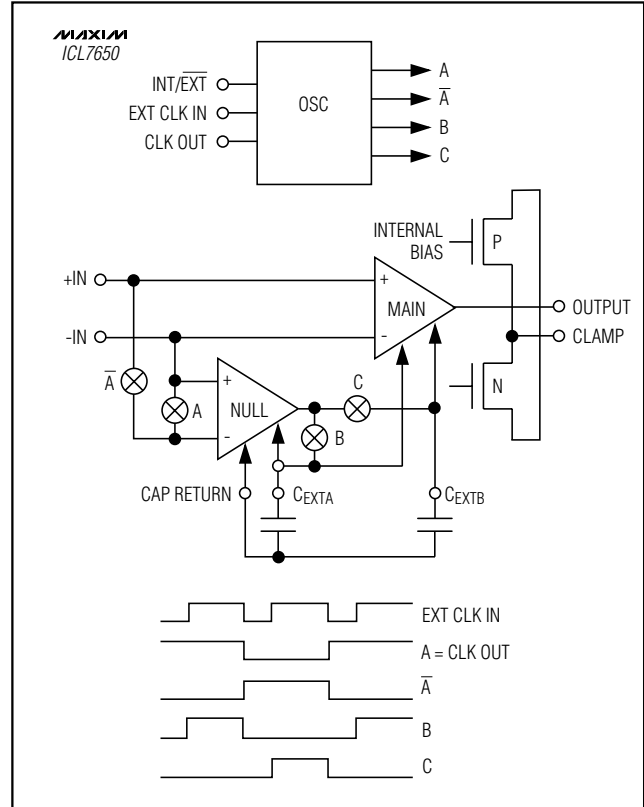


Figure 2. Block Diagram

Intermodulation

Intermodulation effects can cause problems in older chopper-stabilized amplifier modules. Intermodulation occurs since the amplifier has a finite AC gain, and therefore will have a small AC signal at the input. In a chopper-stabilized module, this small AC signal is detected, chopped, and fed into the offset-correction circuit. This results in spurious outputs at the sum and difference frequencies of the chopping and input signal frequencies. Other intermodulation effects in chopper-stabilized modules include gain and phase anomalies near the chopping frequency.

These effects are substantially reduced in the ICL7650/ICL7653, which add to the nulling circuit a dynamic current that compensates for the AC signal on the inputs. Unlike modules, the ICL7650/ICL7653 can precisely compensate for the finite AC gain, since both the AC gain rolloff and the intermodulation compensation current are controlled by internal matched capacitors.

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Nulling Capacitor Connection

Separate pins are provided for C_{RETN} and CLAMP in the ICL7650. If you do not need the clamp feature, order the ICL7653; this device only offers the C_{RETN} pin and will produce slightly lower noise and improved AC common-mode rejection. If you need to use the clamp feature, order the ICL7650 and connect the external capacitors to V-. To prevent load-current IR drops and other extraneous signals from being injected into the capacitors, use a separate PC board trace to connect the capacitor commons directly to the V- pin. The outside foil of the capacitors should be connected to the low-impedance side of the null storage circuit, V- or C_{RETN} . This will act as an ESD voltage shield.

Clock Operation

The ICL7650's internal oscillator generates a 200Hz frequency, which is available at the CLK OUT pin. The device can also be operated with an external clock, if desired. An internal pull-up permits the INT/EXT pin to be left open for normal operation. However, the internal clock must be disabled and INT/EXT must be tied to V- if an external clock is used. An external clock signal may then be applied to the EXT CLK IN pin. The duty cycle of the external clock is not critical at low frequencies. However, a 50% to 80% positive duty cycle is preferred for frequencies above 500Hz, since the capacitors are charged only when EXT CLK IN is high. This ensures that any transients have time to settle before the capacitors are turned off. The external clock should swing between ground and V+ for power supplies up to $\pm 6V$, and between V+ and (V+ - 6V) for higher supply voltages.

To avoid a capacitor imbalance during overload, use a strobe signal. Neither capacitor will be charged if a strobe signal is connected to EXT CLK IN so that it is low while the overload signal is being applied to the amplifier. A typical amplifier will drift less than 10 μV s since the leakage of the capacitor pins is quite low at room temperature. Relatively long measurements may be made with little change in offset.

Applications Information

Device Selection

In applications that require lowest noise, Maxim's ICL7652 may be preferred over the ICL7650/ICL7653. The ICL7650/ICL7653 offer a higher gain-bandwidth product and lower input bias currents, while the ICL7652 reduces noise by using larger input FETs. These larger FETs, however, increase the leakage at the ICL7652's external null pins. Therefore, the ICL7650/ICL7653 can operate to a higher temperature with 0.1 μF capacitors before the clock ripple (due to

leakage at the null capacitor pins) becomes excessive and 1 μF external capacitors are required.

Output Stage/Load Driving

The ICL7650/ICL7653 somewhat resemble a transconductance amplifier whose open-loop gain is proportional to load resistance. This behavior is apparent when loads are less than the high-impedance stage (approximately 18k Ω for one output circuit). The open-loop gain, for example, will be 17dB lower with a 1k Ω load than with a 10k Ω load. This lower gain is of little consequence if the amplifier is used strictly for DC since the DC gain is typically greater than 120dB, even with a 1k Ω load. For wideband applications, however, the best frequency response will be achieved with a load resistor of 10k Ω or higher. The result will be a smooth 6dB per octave response from 0.1Hz to 2MHz, with phase shifts of less than 10° in the transition region where the main amplifier takes over from the null amplifier.

Component Selection

CEXTA and CEXTB, the two required capacitors, have optimum values depending on the clock or chopping frequency. The correct value is 0.1 μF for the preset internal clock. When using an external clock, scale this component value in proportion to the relationship between the chopping frequency and the nulling time constant. A low-leakage ceramic capacitor may prove suitable for many applications; however, a high-quality film-type capacitor (such as mylar) is preferred. For lowest settling time at initial turn-on, use capacitors with low dielectric absorption (such as polypropylene types). With low-dielectric-absorption capacitors, the ICL7650/ICL7653 will settle to 1 μV offset in 100ms, but several seconds may be required if ceramic capacitors are used.

Thermoelectric Effects

Thermoelectric effects developed in thermocouple junctions of dissimilar materials (metals, alloys, silicon, etc.) ultimately limit precision DC measurements. Unless all junctions are at the same temperature, thermoelectric voltages (typically around 10 $\mu V/^{\circ}C$, but up to hundreds of $\mu V/^{\circ}C$ for some materials) will be generated. In order to realize the extremely low offset voltages that the chopper amplifier can provide, take special precautions to avoid temperature gradients. To eliminate air movement, enclose all components (particularly those caused by power-dissipating elements in the system). Minimize power-supply voltages and power dissipation, and use low-thermoelectric-coefficient connections where possible. It is advisable to separate the device surrounding heat-dissipating elements, and to use high-impedance loads.

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Input Guarding

Low-leakage, high-impedance CMOS inputs allow the ICL7650/ICL7653 to measure high-impedance sources. Stray leakage paths can decrease input resistance and increase input currents unless inputs are guarded. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. The board should be coated with epoxy or silicone after cleaning to prevent contamination.

Leakage currents may cause trouble even with properly cleaned and coated boards, particularly since the input pins are adjacent to pins that are at supply potentials. Leakage can be significantly reduced by using guard-

ing to decrease the voltage difference between inputs and adjacent metal runs. Use a 10-lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board to accomplish input guarding of the 8-pin TO-99 package. A conductive ring surrounding the inputs, the "guard," is connected to a low-impedance point that is approximately the same voltage as the inputs. The guard then absorbs the leakage current from the high-voltage pins. Typical guard connections are shown in Figure 3.

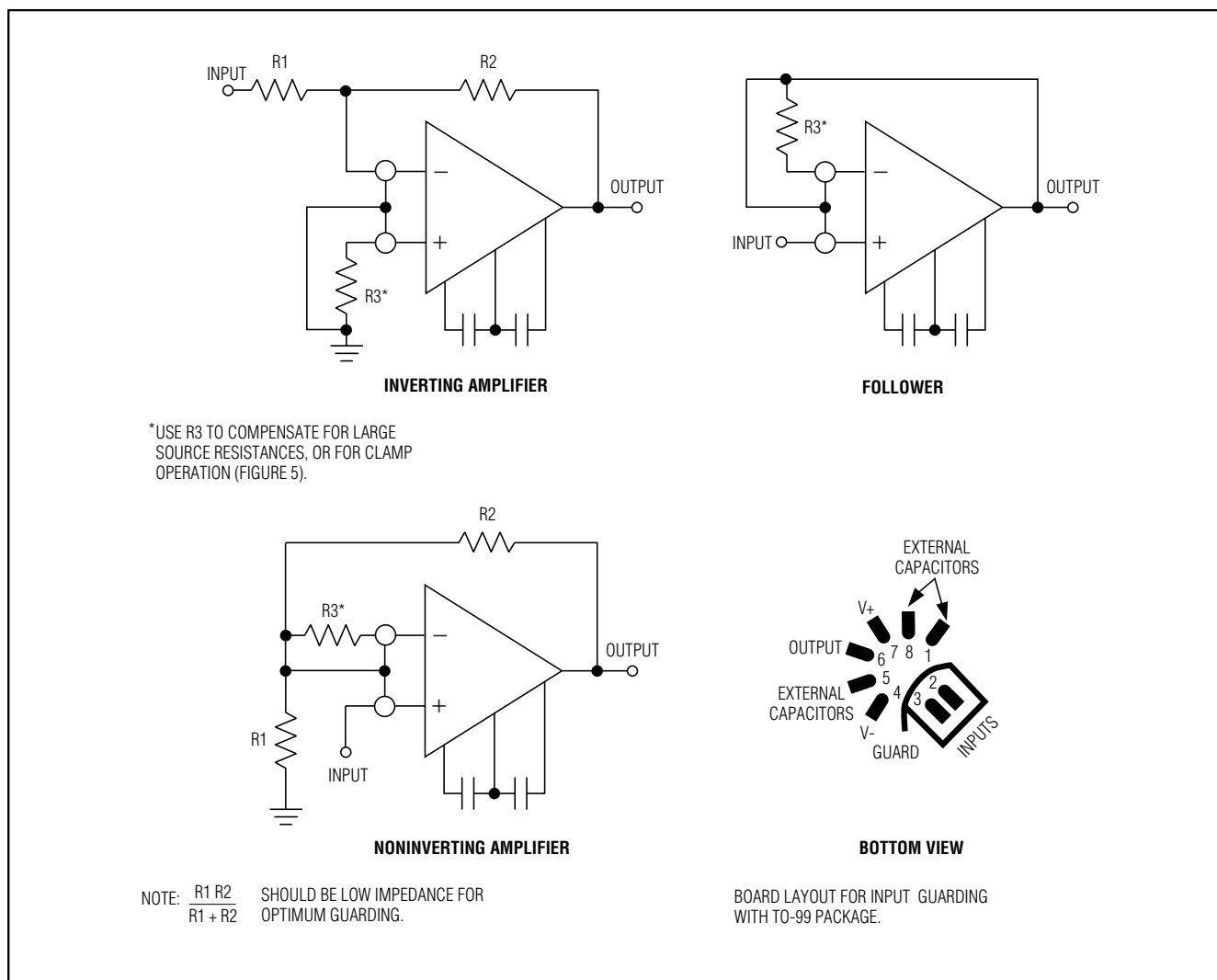


Figure 3. Input Guard Connection

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The 14-pin DIP configuration has been specifically designed to ease input guarding. The pins adjacent to the inputs are not used.

Pin Compatibility

The ICL7653's pinout generally corresponds to that of industry-standard 8-pin devices such as the LM741 or LM101. However, its external null storage capacitors are connected to pins 1 and 8; whereas most op amps leave these pins open or use them for offset null or compensation capacitors.

The OP05 and OP07 op amps can be converted for ICL7650/ICL7653 operation. This can be accomplished by removing the offset null potentiometer, which is connected from pins 1 and 8 to $V+$, and replacing it with two capacitors connected from pins 1 and 8 to $V-$. For LM108 devices, the compensation capacitor is replaced by the external nulling capacitors. Pin 5 is the output clamp connection on the ICL7650/ICL7653. By removing any circuit connections from this pin, the LM101/LM748/LM709 devices can undergo a similar conversion.

Typical Applications

Figure 4 shows the ICL7650/ICL7653 automatically nulling the offset voltage of a high-speed amplifier. The ICL7650/ICL7653 continuously monitor the voltage at

the amplifier's inverting input, integrate the error, and drive the amplifier's noninverting input to correct for the offset voltage detected at the inverting input. The circuit's DC offset characteristics are determined by the ICL7650/ICL7653, and its AC performance is determined by the high-speed amplifier. While this circuit continuously and automatically adjusts the amplifier's offset to less than $5\mu\text{V}$, it does not correct for errors caused by the input bias current, so the value of resistor R_F should be as low as is practical. This technique can be used with any op amp that is configured as an inverting amplifier.

Figures 5 and 6 illustrate basic inverting and noninverting amplifier circuits. Both figures show an output clamping circuit being used to enhance overload recovery performance. Supply voltage ($\pm 8\text{V}$ max) and output drive capability ($10\text{k}\Omega$ load for full swing) are the only limitations to consider when replacing other op amps with the ICL7650/ICL7653. Use a simple booster circuit to overcome these limitations (Figure 7). This enables the full output capabilities of the LM118 (or any other standard device) to be combined with the input capabilities of the ICL7650/ICL7653. Observe the loop gain stability carefully when the feedback network is added, particularly when a slower amplifier such as the LM741 is used.

A lower voltage supply is required when mixing the ICL7650/ICL7653 with circuits that operate at $\pm 15\text{V}$ supplies. One approach is to use a highly efficient voltage divider. This is illustrated in Figure 8, where the ICL7660 voltage converter is used to convert $+15\text{V}$ to $+7.5\text{V}$.

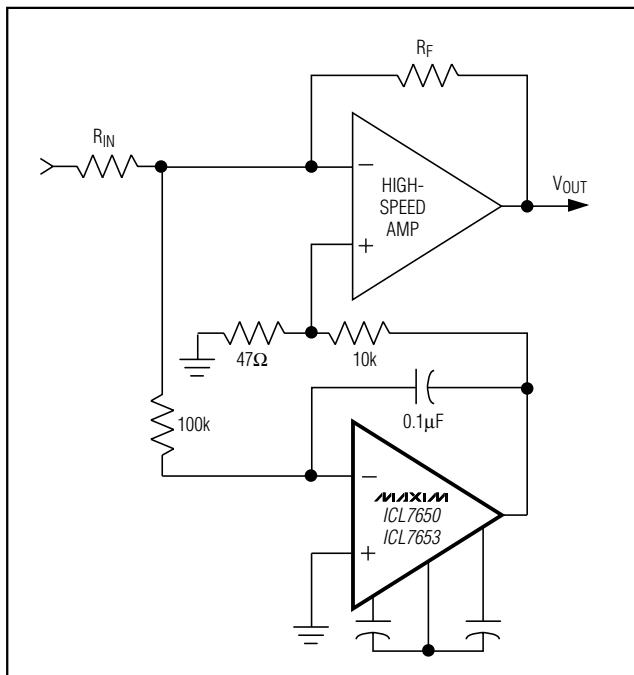


Figure 4. Nulling a High-Speed Amplifier

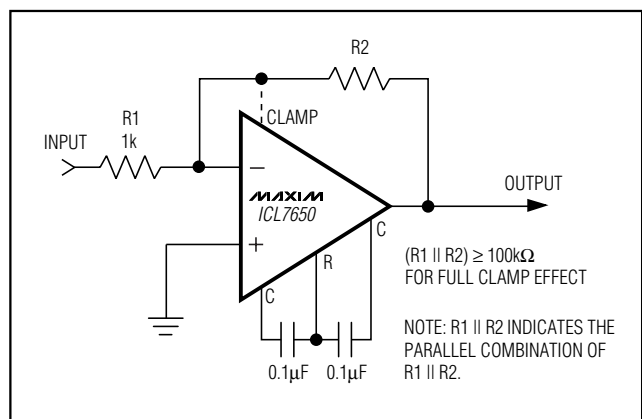


Figure 5. Inverting Amplifier with Optional Clamp

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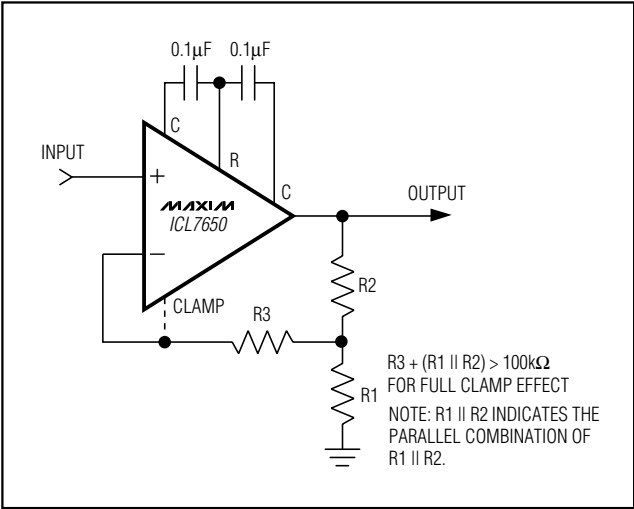


Figure 6. Noninverting Amplifier with Optional Clamp

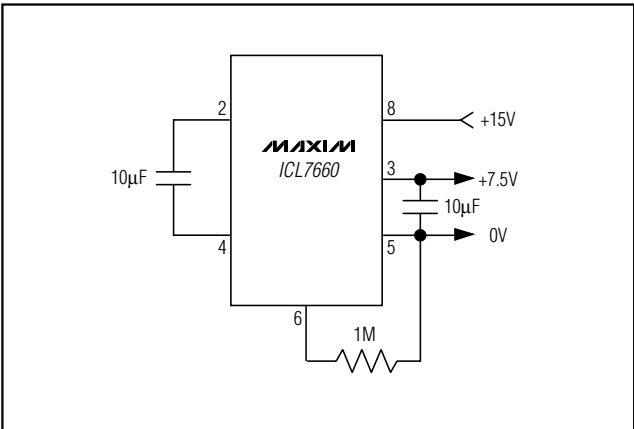


Figure 8. Splitting +15V with an ICL7660, 95% Efficiency (Same for -15V)

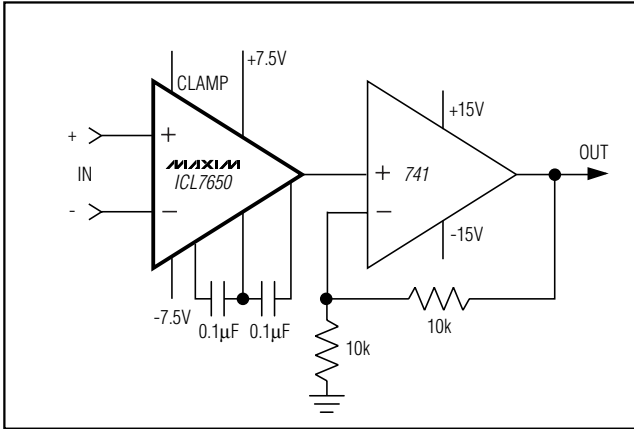
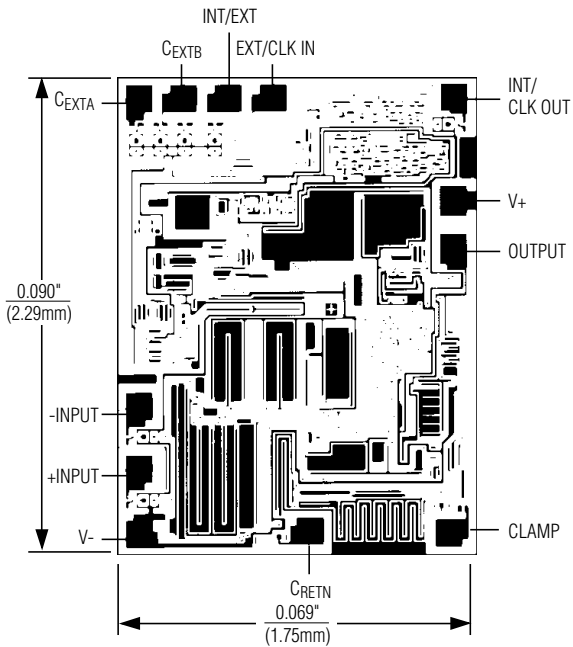


Figure 7. Using an Industry-Standard 741 to Boost Output Drive Capability

Chip Topography

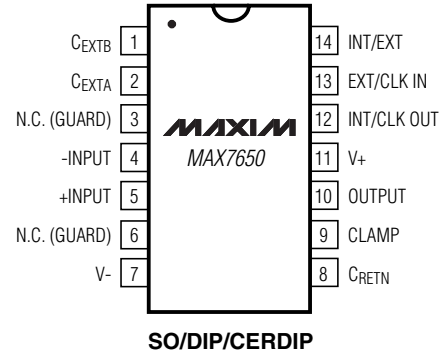


Chopper-Stabilized Op Amps

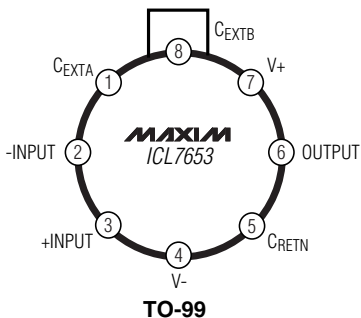
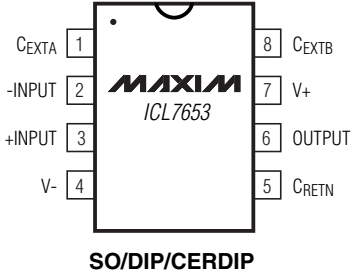
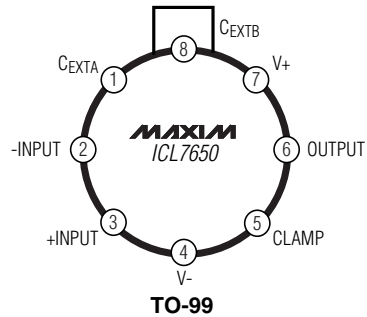
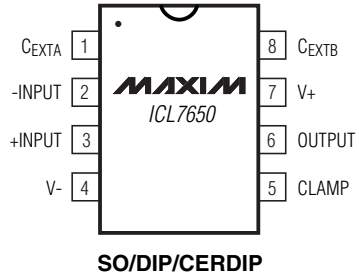
Pin Configurations

ICL7650/ICL7650B/ICL7653/ICL7653B

TOP VIEW



N.C. = NO INTERNAL CONNECTION



Chopper-Stabilized Op Amps

Package Information

SOIC .150

| | INCHES | | MILLIMETERS | |
|----|--------|-------|-------------|------|
| | MIN | MAX | MIN | MAX |
| A | 0.053 | 0.069 | 1.35 | 1.75 |
| A1 | 0.004 | 0.010 | 0.10 | 0.25 |
| B | 0.014 | 0.019 | 0.35 | 0.49 |
| C | 0.007 | 0.010 | 0.19 | 0.25 |
| e | 0.050 | | 1.27 | |
| E | 0.150 | 0.157 | 3.80 | 4.00 |
| H | 0.228 | 0.244 | 5.80 | 6.20 |
| h | 0.010 | 0.020 | 0.25 | 0.50 |
| L | 0.016 | 0.050 | 0.40 | 1.27 |

| | INCHES | | MILLIMETERS | | N | MS012 |
|---|--------|-------|-------------|-------|----|-------|
| | MIN | MAX | MIN | MAX | | |
| D | 0.189 | 0.197 | 4.80 | 5.00 | 8 | A |
| D | 0.337 | 0.344 | 8.55 | 8.75 | 14 | B |
| D | 0.386 | 0.394 | 9.80 | 10.00 | 16 | C |

NOTES:

1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

120 SAN GABRIEL DR. SUNNYVALE, CA 94086 FAX (408) 737-7754
PROPRIETARY INFORMATION

PACKAGE FAMILY OUTLINE: SOIC .150"

1/1

21-0041 A

DOCUMENT CONTROL NUMBER REV

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