PIN CONFIGURATION

VDD_PCI	1	56	PCI0
VSS_PCI	2	55	PCI_STOP#
PCI1	3	54	CPU_STOP#
PCI2	4	53	FSC/TEST_SEL
PCI3	5	52	REF
VSS_PCI	6	51	VSS_REF
VDD_PCI	7	50	XTAL_IN
PCIF0/ITP_EN	8	49	XTAL_OUT
PCIF1	9	48	VDD_REF
VTT_PWRGD#/PD	10	47	SDA
VDD48	11	46	SCL
USB48/FSA	12	45	VSS_CPU
VSS48	13	44	CPU0
DOT96	14	43	CPU0#
DOT96#	15	42	VDD_CPU
FSB/TEST_MODE	16	41	CPU1
SRC0	17	40	CPU1#
SRC0#	18	39	IREF
SRC1	19	38	VSSA
SRC1#	20	37	VDDA
VDD_SRC	21	36	CPU2_ITP/SRC7
SRC2	22	35	CPU2_ITP#/SRC7#
SRC2#	23	34	VDD_SRC
SRC3	24	33	CLKREQA#(1)
SRC3#	25	32	CLKREQB#(1)
SRC4	26	31	SRC5
SRC4#	27	30	SRC5#
VDD_SRC	28	29	VSS_SRC

NOTE:
1. 130K pull-up resistor.

TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Min	Max	Unit
VDDA	3.3V Core Supply Voltage		4.6	V
VDD	3.3V Logic Input Supply Voltage	GND - 0.5	4.6	V
TSTG	Storage Temperature	–65	+150	°C
TAMBIENT	Ambient Operating Temperature	0	+70	°C
TCASE	Case Temperature		+115	°C
ESD Prot	Input ESD Protection Human Body Model	2000		V

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

FREQUENCY SELECTION TABLE

FSC, B, A	CPU	SRC[7:0]	PCI	USB	DOT	REF
101	100	100	33.3	48	96	14.318
001	133	100	33.3	48	96	14.318
011	166	100	33.3	48	96	14.318
010	200	100	33.3	48	96	14.318
000	266	100	33.3	48	96	14.318
100	333	100	33.3	48	96	14.318
110	400	100	33.3	48	96	14.318
111	Reserve	100	33.3	48	96	14.318

PIN DESCRIPTION

Pin Number	Name	Type	Description
1	VDD_PCI	PWR	3.3V
2	VSS_PCI	GND	GND
3	PCI1	OUT	PCI clock
4	PCI2	OUT	PCI clock
5	PCI3	OUT	PCI clock
6	VSS_PCI	GND	GND
7	VDD_PCI	PWR	3.3V
8	PCIF0/ITP_EN	I/O	PCI clock, free running. CPU2 select (sampled on VTT_PWRGD# assertion) HIGH = CPU2.
9	PCIF1	I/O	PCI clock, free running.
10	VTT_PWRGD#/PD	IN	Level-sensitive strobe used to latch the FSA, FSB, FSC/TEST_SEL, and PCIF0/ITP_EN inputs. After VTT_PWRGD# assertion, becomes a real-time input for asserting power down. (Active HIGH)
11	VDD48	PWR	3.3V
12	USB48/FSA	OUT	48MHz clock for CPU frequency selection
13	VSS48	GND	GND
14	DOT96	OUT	96MHz 0.7 current mode differential clock output
15	DOT96#	OUT	96MHz 0.7 current mode differential clock output
16	FSB/TEST_MODE	IN	CPU frequency selection. Selects REF/N or Hi-Z when in test mode, Hi-Z = 1, REF/N = 0.
17	SRC0	OUT	Differential serial reference clock
18	SRC0#	OUT	Differential serial reference clock
19	SRC1	OUT	Differential serial reference clock
20	SRC1#	OUT	Differential serial reference clock
21	VDD_SRC	PWR	3.3V
22	SRC2	OUT	Differential serial reference clock
23	SRC2#	OUT	Differential serial reference clock
24	SRC3	OUT	Differential serial reference clock
25	SRC3#	OUT	Differential serial reference clock
26	SRC4	OUT	Differential serial reference clock
27	SRC4#	OUT	Differential serial reference clock
28	VDD_SRC	PWR	3.3V
29	VSS_SRC	GND	GND
30	SRC5#	OUT	Differential serial reference clock
31	SRC5	OUT	Differential serial reference clock
32	CLKREQB#	IN	SRC clock enable (Active LOW, see Byte 8)
33	CLKREQA#	IN	SRC clock enable (Active LOW, see Byte 8)
34	VDD_SRC	PWR	3.3V
35	CPU2_ITP#/SRC7#	OUT	Selectable CPU or SRC differential clock output. ITP_EN = 0 at VTT_PWRGD# assertion = SRC7#.
36	CPU2_ITP/SRC7	OUT	Selectable CPU or SRC differential clock output. ITP_EN = 0 at VTT_PWRGD# assertion = SRC7.
37	VDDA	PWR	3.3V
38	VSSA	GND	GND
39	IREF	OUT	Reference current for differential output buffer
40	CPU1#	OUT	Host 0.7 current mode differential clock output
41	CPU1	OUT	Host 0.7 current mode differential clock output
42	VDD_CPU	PWR	3.3V

PIN DESCRIPTION (CONT.)

Pin Number	Name	Type	Description
43	CPU0#	OUT	Host 0.7 current mode differential clock output
44	CPU0	OUT	Host 0.7 current mode differential clock output
45	VSS_CPU	GND	GND
46	SCL	IN	SM bus clock
47	SDA	I/O	SM bus data
48	VDD_REF	PWR	3.3V
49	XTAL_OUT	OUT	XTAL output
50	XTAL_IN	IN	XTAL input
51	VSS_REF	GND	GND
52	REF	OUT	14.318 MHz reference clock output
53	FSC/TEST_SEL	IN	CPU frequency selection. Selects test mode if pulled above 2V when VTT_PWRGD# is asserted LOW.
54	CPU_STOP#	IN	Stop all stoppable CPU CLK
55	PCI_STOP#	IN	Stop all stoppable PCI, SRC CLK
56	PCI0	OUT	PCI clock

INDEX BLOCK WRITE PROTOCOL

Bit	# of bits	From	Description
1	1	Master	Start
2-9	8	Master	D2h
10	1	Slave	Ack (Acknowledge)
11-18	8	Master	Register offset byte (starting byte)
19	1	Slave	Ack (Acknowledge)
20-27	8	Master	Byte count, N (0 is not valid)
28	1	Slave	Ack (Acknowledge)
29-36	8	Master	first data byte (Offset data byte)
37	1	Slave	Ack (Acknowledge)
38-45	8	Master	2nd data byte
46	1	Slave	Ack (Acknowledge)
			:
		Master	Nth data byte
		Slave	Acknowledge
		Master	Stop

INDEX BLOCK READ PROTOCOL

Master can stop reading any time by issuing the stop bit without waiting until Nth byte (byte count bit30-37).

Bit	# of bits	From	Description
1	1	Master	Start
2-9	8	Master	D2h
10	1	Slave	Ack (Acknowledge)
11-18	8	Master	Register offset byte (starting byte)
19	1	Slave	Ack (Acknowledge)
20	1	Master	Repeated Start
21-28	8	Master	D3h
29	1	Slave	Ack (Acknowledge)
30-37	8	Slave	Byte count, N (block read back of N bytes), power on is 8
38	1	Master	Ack (Acknowledge)
39-46	8	Slave	first data byte (Offset data byte)
47	1	Master	Ack (Acknowledge)
48-55	8	Slave	2nd data byte
			Ack (Acknowledge)
			:
		Master	Ack (Acknowledge)
		Slave	Nth data byte
			Not acknowledge
		Master	Stop

INDEX BYTE WRITE

Setting bit[11:18] = starting address, bit[20:27] = 01h.

INDEX BYTE READ

Setting bit[11:18] = starting address. After reading back the first data byte, master issues Stop bit.

SSC MAGNITUDE CONTROL FOR CPU, SRC, AND SMC

SMC[2:0]	
000	-0.25
001	-0.5
010	-0.75
011	-1
100	±0.125
101	±0.25
110	±0.375
111	±0.5

RESOLUTION

CPU (MHz)	Resolution	N =
100	0.666667	150
133	0.666667	200
166	1.333333	125
200	1.333333	150
266	1.333333	200
333	2.666667	125
400	2.666667	150

S.E. CLOCK STRENGTH SELECTION (PCI, REF, USB48)

Str[1:0]	Level
00	1
01	0.8
10	0.6
11	1.2

CONTROL REGISTERS

N PROGRAMMING PROCEDURE

- Use Index byte write.
- For N programming, the user only needs to access Byte 12, Byte 13, and Byte 10.

1. Write Byte 12 for CPU PLL N, CPU f = N* Resolution (see resolution table).
2. Write Byte 13 for SRC PLL N, SRC f = N*0.666667, PCI = SRC f /3.
3. Enable N Programming bit, Byte 10 bit 1. Once this bit is enabled, any N value will be changed on the fly.

BYTE 0

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
0	SRC0, SRC0#	Output Enable	Tristate	Enable	RW	1
1	SRC1, SRC1#	Output Enable	Tristate	Enable	RW	1
2	SRC2, SRC2#	Output Enable	Tristate	Enable	RW	1
3	SRC3, SRC3#	Output Enable	Tristate	Enable	RW	1
4	SRC4, SRC4#	Output Enable	Tristate	Enable	RW	1
5	SRC5, SRC5#	Output Enable	Tristate	Enable	RW	1
6	Reserved				RW	1
7	CPU2, CPU2#/ SRC7, SRC7#	Output Enable	Tristate	Enable	RW	1

BYTE 1

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
0	CPU[2:0], SRC[7:0], PCI[5:0], PCIF[1:0]	Spread Spectrum mode enable	Spread off	Spread on	RW	0
1	CPU0, CPU0#	Output Enable	Tristate	Enable	RW	1
2	CPU1, CPU1#	Output Enable	Tristate	Enable	RW	1
3	Reserved				RW	1
4	REF	Output Enable	Tristate	Enable	RW	1
5	USB48	Output Enable	Tristate	Enable	RW	1
6	DOT96	Output Enable	Tristate	Enable	RW	1
7	PCIF0	Output Enable	Tristate	Enable	RW	1

BYTE 2

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
0	PCIF1	Output Enable	Tristate	Enable	RW	1
1	Reserved				RW	1
2	Reserved				RW	1
3	Reserved				RW	1
4	PCI0	Output Enable	Tristate	Enable	RW	1
5	PCI1	Output Enable	Tristate	Enable	RW	1
6	PCI2	Output Enable	Tristate	Enable	RW	1
7	PCI3	Output Enable	Tristate	Enable	RW	1

BYTE 3

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0	SRC0	Allow controlled by PCI_STOP# assertion	Free running, not affected by PCI_STOP#	Stopped with PCI_STOP#	RW	0
1	SRC1				RW	0
2	SRC2				RW	0
3	SRC3				RW	0
4	SRC4				RW	0
5	SRC5				RW	0
6	Reserved				RW	0
7	SRC7	Allow controlled by PCI_STOP# assertion	Free running, not affected by PCI_STOP#	Stopped with PCI_STOP#	RW	0

BYTE 4

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0	CPU0, CPU0#	Allow control of CPU0 with assertion of CPU_STOP#	Not stopped by CPU_STOP#	Stopped with CPU_STOP#	RW	1
1	CPU1, CPU1#	Allow control of CPU1 with assertion of CPU_STOP#	Not stopped by CPU_STOP#	Stopped with CPU_STOP#	RW	1
2	CPU2, CPU2#	Allow control of CPU2 with assertion of CPU_STOP#	Not stopped by CPU_STOP#	Stopped with CPU_STOP#	RW	1
3	PCIF0	Allow controlled by PCI_STOP# assertion	Not stopped by PCI_STOP#	Stopped with PCI_STOP#	RW	0
4	PCIF1				RW	0
5	Reserved				RW	0
6	DOT96	DOT96 power down drive mode	Driven in power down	Tristate	RW	0
7	Reserved				RW	0

BYTE 5

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0	CPU0, CPU0#	CPU0 PD drive mode	Driven in power down	Tristate in power down	RW	0
1	CPU1, CPU1#	CPU1 PD drive mode	Driven in power down	Tristate in power down	RW	0
2	CPU2, CPU2#	CPU2 PD drive mode	Driven in power down	Tristate in power down	RW	0
3	SRCS	SRC PD drive mode	Driven in power down	Tristate in power down	RW	0
4	CPU0	CPU0 CPU_STOP drive mode	Driven in CPU_STOP#	Tristate when stopped	RW	0
5	CPU1	CPU1 CPU_STOP drive mode	Driven in CPU_STOP#	Tristate when stopped	RW	0
6	CPU2	CPU2 CPU_STOP drive mode	Driven in CPU_STOP#	Tristate when stopped	RW	0
7	SRCS	SRC PCI_STOP drive mode	Driven in PCI_STOP	Tristate when stopped	RW	0

BYTE 6

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0	CPU[2:0]	FSA latched value on power up			R	FSA
1	CPU[2:0]	FSB latched value on power up			R	FSB
2	CPU[2:0]	FSC latched value on power up			R	FSC
3	PCI, SRC	Software PCI_STOP control for PCI and SRC CLK	Stop all PCI, PCIF, and SRC which can be stopped by PCI_STOP#	Software STOP Disabled	RW	1
4	REF	REF drive strength	1x drive	2x drive	RW	1
5	Reserved				RW	0
6		Test clock mode entry control	Normal operation	Test mode, controlled by Byte 6, Bit 7	RW	0
7	CPU, SRC, PCI PCIF, REF, USB48, DOT96	Only valid when Byte 6, Bit 7 is HIGH	Hi-Z	REF/N	RW	0

BYTE 7

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0		Vendor ID			R	1
1		Vendor ID			R	0
2		Vendor ID			R	1
3		Vendor ID			R	0
4		Revision ID			R	0
5		Revision ID			R	0
6		Revision ID			R	0
7		Revision ID			R	0

BYTE 8[1,2]

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0	SRC0	Controlled by CLKREQA#. When CLKREQA# is HIGH, output is Hi-Z	Not Controlled	Controlled	RW	0
1	SRC2				RW	0
2	SRC4				RW	1
3	Reserved				RW	0
4	SRC1	Controlled by CLKREQB#. When CLKREQB# is HIGH, output is Hi-Z	Not Controlled	Controlled	RW	0
5	SRC3				RW	0
6	SRC5				RW	1
7	Reserved				RW	0

NOTES:
1. When SRCCLK outputs controlled by CLKREQA# and CLKREQB# are enabled, clock output behavior will follow SMBus control bits (per CK410 spec).
2. Assertion/de-assertion time of CLKREQ# pins will match PCI_STOP# timing of the CK410 spec. This is 15ns from the assertion/de-assertion of CLKREQ# to the drive/tie-state of the respective SRCCLK output.

BYTE 9 (RESERVED)

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
0	Reserved				RW	
1	Reserved				RW	
2	Reserved				RW	
3	Reserved				RW	
4	Reserved				RW	
5	Reserved				RW	
6	Reserved				RW	
7	Reserved				RW	

BYTE 10

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0	Reserved				RW	0
1		N Programming enable	Disable	Enable	RW	0
2	Reserved				RW	0
3	Reserved				RW	0
4		USB PLL power down	Normal	Power Down	RW	0
5		SRC PLL power down	Normal	Power Down	RW	0
6		CPU PLL power down	Normal	PowerDown	RW	0
7	Reserved				RW	0

BYTE 11

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0	SRC SMC0	SRC/PCI SSC control see SMC table			RW	1
1	SRC SMC1				RW	0
2	SRC SMC2				RW	0
3	Reserve				RW	0
4	CPU SMC0	CPU PLL SSC control see SMC table			RW	1
5	CPU SMC1				RW	0
6	CPU SMC2				RW	0
7	Reserve				RW	0

BYTE 12

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0	CPU_N0, LSB	CPU CLK = N* Resolution see Resolution table			RW	0
1	CPU_N1				RW	1
2	CPU_N2				RW	1
3	CPU_N3				RW	0
4	CPU_N4				RW	1
5	CPU_N5				RW	0
6	CPU_N6				RW	0
7	CPU_N7, MSB				RW	1

BYTE 13

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0	SRC_N0, LSB	SRC f = N*SRC Resolution Resolution=0.666667 100MHz N= 150			RW	0
1	SRC_N1				RW	1
2	SRC_N2				RW	1
3	SRC_N3				RW	0
4	SRC_N4				RW	1
5	SRC_N5				RW	0
6	SRC_N6				RW	0
7	SRC_N7, MSB				RW	1

BYTE 14

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0	48MHzStr0				RW	1
1	48MHStr1	USB48MHz strength selection(1)			RW	1
2	REFStr0				RW	0
3	REFStr1	REF strength selection(1)			RW	0
4	PCIStrC0				RW	0
5	PCIStrC1	PCI strength selection(1)			RW	0
6	PCIFStr0				RW	0
7	PCIFStr1	PCIF strength selection(1)			RW	0

NOTE:
1. See S.E. Clock Strength Selection table.

BYTE 15

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0	PCI0	Allow controlled by PCI_STOP# assertion	Free running, not affected by PCI_STOP#	Stopped with PCI_STOP#	RW	1
1	PCI1				RW	1
2	PCI2				RW	1
3	PCI3				RW	1
4	Reserved					0
5	Reserved					0
6	Reserved					0
7	Reserved					0

BYTES 16 - 20 ARE NOT TO BE USED

BYTE 21, BLOCK READ BYTE COUNT(1)

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0						0
1						1
2						1
3						0
4						1
5						0
6						0
7						0

NOTE:
1. The value contained in this register is used for index block read access on SM Bus.

ELECTRICAL CHARACTERISTICS - INPUT / SUPPLY / COMMON OUTPUT PARAMETERS

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IH}	Input HIGH Voltage	3.3V ± 5%	2	—	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage	3.3V ± 5%	V_{SS} - 0.3	—	0.8	V
V_{IH}_FS	LOW Voltage, HIGH Threshold	For FSA.B.C test_mode	0.7	—	V_{DD} + 0.3	V
V_{IL}_FS	LOW Voltage, LOW Threshold	For FSA.B.C test_mode	V_{SS} - 0.3	—	0.35	V
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}	–5	—	5	µA
I_{IL1}	Input LOW Current	V_{IN} = 0V, inputs with no pull-up resistors	–5	—	—	µA
I_{IL2}	Input LOW Current	V_{IN} = 0V, inputs with pull-up resistors	–200	—	—	µA
$I_{DD3.3OP}$	Operating Supply Current	Full active, C_L = full load	—	—	400	mA
$I_{DD3.3PD}$	Powerdown Current	All differential pairs driven	—	—	70	mA
		All differential pairs tri-stated	—	—	12	
F_I	Input Frequency(1)	V_{DD} = 3.3V	—	14.31818	—	MHz
L_{PIN}	Pin Inductance(2)		—	—	7	nH
C_{IN}	Input Capacitance(2)	Logic inputs	—	—	5	pF
C_{OUT}		Output pin capacitance	—	—	6	
C_{INX}		XTAL_IN	—	—	5	
C_{OUTX}		XTAL_OUT	—	—	12	
T_{STAB}	Clock Stabilization(2,3)	From V_{DD} power-up or de-assertion of PD to first clock	—	—	1.8	ms
	Modulation Frequency(2)	Triangular modulation	30	—	33	KHz
	T_{DRIVE}_SRC(2)	SRC output enable after PCI_STOP# de-assertion	—	—	15	ns
	T_{DRIVE}_PD(2)	CPU output enable after PD de-assertion	—	—	300	us
	T_{FALL}_PD(2)	Fall time of PD	—	—	5	ns
	T_{RISE}_PD(2)	Rise time of PD	—	—	5	ns
	T_{DRIVE}_CPU_STOP#(2)	CPU output enable after CPU_STOP# de-assertion	—	—	10	ns
	T_{FALL}_CPU_STOP#(2)	Fall time of CPU_STOP#	—	—	5	ns
	T_{RISE}_CPU_STOP#(2)	Rise time of CPU_STOP#	—	—	5	ns

NOTES:
1. Input frequency should be measured at the REF output pin and tuned to ideal 14.31818MHz to meet ppm frequency accuracy on PLL outputs.
2. This parameter is guaranteed by design, but not 100% production tested.
3. See TIMING DIAGRAMS for timing requirements.

ELECTRICAL CHARACTERISTICS - CPU, SRC, AND DOT96 0.7 CURRENT MODE DIFFERENTIAL PAIR[1]

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%; C_L = 2pF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Z_O	Current Source Output Impedance[2]	$V_O = V_X$	3000	—	—	Ω
V_{OH3}	Output HIGH Voltage	I_{OH} = -1mA	2.4	—	—	V
V_{OL3}	Output LOW Voltage	I_{OL} = 1mA	—	—	0.4	V
V_{HIGH}	Voltage HIGH[2]	Statistical measurement on single-ended signal using oscilloscope math function	660	—	1150	mV
V_{LOW}	Voltage LOW[2]		–300	—	150	
V_{OVS}	Max Voltage[2]	Measurement on single-ended signal using absolute value	—	—	1150	mV
V_{UDS}	Min Voltage[2]		–300	—	—	
$V_{CROSS(ABS)}$	Crossing Voltage (abs)[2]		250	—	550	mV
d - V_{CROSS}	Crossing Voltage (var)[2]	Variation of crossing over all edges	—	—	140	mV
ppm	Static Error[2,3]	See T_{PERIOD} Min. - Max. values	—	—	0	ppm
T_{PERIOD}	Average Period[3]	400MHz nominal / -0.5% spread	2.4993	—	2.5133	ns
		333.33MHz nominal / -0.5% spread	2.9991	—	3.016	
		266.66MHz nominal / -0.5% spread	3.7489	—	3.77	
		200MHz nominal / -0.5% spread	4.9985	—	5.0266	
		166.66MHz nominal / -0.5% spread	5.9982	—	6.032	
		133.33MHz nominal / -0.5% spread	7.4978	—	7.54	
		100MHz nominal / -0.5% spread	9.997	—	10.0533	
		96MHz nominal	10.4135	—	10.4198	
T_{ABSMIN}	Absolute Min Period[2,3]	400MHz nominal / -0.5% spread	2.4143	—	—	ns
		333.33MHz nominal / -0.5% spread	2.9141	—	—	
		266.66MHz nominal / -0.5% spread	3.6639	—	—	
		200MHz nominal / -0.5% spread	4.9135	—	—	
		166.66MHz nominal / -0.5% spread	5.9132	—	—	
		133.33MHz nominal / -0.5% spread	7.4128	—	—	
		100MHz nominal / -0.5% spread	9.912	—	—	
		96MHz nominal	10.1635	—	—	
t_R	Rise Time[2]	V_{OL} = 0.175V, V_{OH} = 0.525V	175	—	700	ps
t_F	Fall Time[2]	V_{OL} = 0.175V, V_{OH} = 0.525V	175	—	700	ps
d-t_R	Rise Time Variation[2]		—	—	125	ps
d-t_F	Fall Time Variation[2]		—	—	125	ps
d_{T3}	Duty Cycle[2]	Measurement from differential waveform	45	—	55	%

NOTES:
1. SRC clock outputs run only at 100MHz.
2. This parameter is guaranteed by design, but not 100% production tested.
3. All long term accuracy and clock period specifications are guaranteed with the assumption that the REF output is at 14.31818MHz.

ELECTRICAL CHARACTERISTICS - CPU, SRC, AND DOT96 0.7 CURRENT MODE DIFFERENTIAL PAIR, CONTINUED[1]

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%; C_L = 2pF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{SK3}	Skew, CPU[1:0][2]	V_T = 50%	—	—	100	ps
	Skew, CPU2[2]		—	—	250	
	Skew, SRC[2]		—	—	250	
$t_{JCYC-CYC}$	Jitter, Cycle to Cycle, CPU[1:0][2]	Measurement from differential waveform	—	—	85	ps
	Jitter, Cycle to Cycle, CPU2[2]		—	—	100	
	Jitter, Cycle to Cycle, SRC[2]		—	—	125	
	Jitter, Cycle to Cycle, DOT96[2]		—	—	250	

NOTES:
1. SRC clock outputs run only at 100MHz.
2. This parameter is guaranteed by design, but not 100% production tested.

ELECTRICAL CHARACTERISTICS - PCICLK / PCICLK_F

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%; C_L = 10 - 30pF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ppm	Static Error[1,2]	See Tperiod Min. - Max. values	—	—	0	ppm
T_{PERIOD}	Clock Period[2]	33.33MHz output nominal	29.991	—	30.009	ns
		33.33MHz output spread	29.991	—	30.1598	
V_{OH}	Output HIGH Voltage	I_{OH} = -1mA	2.4	—	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 1mA	—	—	0.55	V
I_{OH}	Output HIGH Current	V_{OH} at Min. = 1V	-33	—	—	mA
		V_{OH} at Max. = 3.135V	—	—	-33	
I_{OL}	Output LOW Current	V_{OL} at Min. = 1.95V	30	—	—	mA
		V_{OL} at Max. = 0.4V	—	—	38	
	Edge Rate[1]	Rising edge rate	1	—	4	V/ns
	Edge Rate[1]	Falling edge rate	1	—	4	V/ns
t_{R1}	Rise Time[1]	V_{OL} = 0.8V, V_{OH} = 2V	0.3	—	1.2	ns
t_{F1}	Fall Time[1]	V_{OL} = 0.8V, V_{OH} = 2V	0.3	—	1.2	ns
d_{T1}	Duty Cycle[1]	V_T = 1.5V	45	—	55	%
t_{SK1}	Skew[1]	V_T = 1.5V	—	—	500	ps
$t_{JCYC-CYC}$	Jitter, Cycle to Cycle[1]	V_T = 1.5V	—	—	500	ps

NOTES:
1. This parameter is guaranteed by design, but not 100% production tested.
2. All long term accuracy and clock period specifications are guaranteed with the assumption that the REF output is at 14.31818MHz.

ELECTRICAL CHARACTERISTICS, 48MHZ, USB

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%; C_L = 10 - 20pF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ppm	Static Error[1,2]	See Tperiod Min. - Max. values	—	—	0	ppm
T_{PERIOD}	Clock Period[2]	48MHz output nominal	20.8257	—	20.834	ns
V_{OH}	Output HIGH Voltage	I_{OH} = -1mA	2.4	—	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 1mA	—	—	0.55	V
I_{OH}	Output HIGH Current	V_{OH} at Min. = 1V	-29	—	—	mA
		V_{OH} at Max. = 3.135V	—	—	-23	
I_{OL}	Output LOW Current	V_{OL} at Min. = 1.95V	29	—	—	mA
		V_{OL} at Max. = 0.4V	—	—	27	
	Edge Rate[1]	Rising edge rate	1	—	2	V/ns
	Edge Rate[1]	Falling edge rate	1	—	2	V/ns
t_{R1}	Rise Time[1]	V_{OL} = 0.8V, V_{OH} = 2V	0.5	—	1.2	ns
t_{F1}	Fall Time[1]	V_{OL} = 0.8V, V_{OH} = 2V	0.5	—	1.2	ns
d_{T1}	Duty Cycle[1]	V_T = 1.5V	45	—	55	%
$t_{JCYC\text{-}CYC}$	Jitter, Cycle to Cycle		—	—	350	ps

NOTES:
1. This parameter is guaranteed by design, but not 100% production tested.
2. All long term accuracy and clock period specifications are guaranteed with the assumption that the REF output is at 14.31818MHz.

ELECTRICAL CHARACTERISTICS - REF-14.318MHZ

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%; C_L = 10 - 20pF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ppm	Long Accuracy[1]	See Tperiod Min. - Max. values	—	—	0	ppm
T_{PERIOD}	Clock Period	14.318MHz output nominal	69.827	—	69.855	ns
V_{OH}	Output HIGH Voltage[1]	I_{OH} = -1mA	2.4	—	—	V
V_{OL}	Output LOW Voltage[1]	I_{OL} = 1mA	—	—	0.4	V
I_{OH}	Output HIGH Current	V_{OH} at Min. = 1V	-33	—	—	mA
		V_{OH} at Max. = 3.135V	—	—	-33	
I_{OL}	Output LOW Current	V_{OL} at Min. = 1.95V	30	—	—	mA
		V_{OL} at Max. = 0.4V	—	—	38	
	Edge Rate[1]	Rising edge rate	1	—	4	V/ns
	Edge Rate[1]	Falling edge rate	1	—	4	V/ns
t_{R1}	Rise Time[1]	V_{OL} = 0.8V, V_{OH} = 2V	0.3	—	1.2	ns
t_{F1}	Fall Time[1]	V_{OL} = 0.8V, V_{OH} = 2V	0.3	—	1.2	ns
d_{T1}	Duty Cycle[1]	V_T = 1.5V	45	—	55	%
$t_{JCYC\text{-}CYC}$	Jitter, Cycle to Cycle[1]	V_T = 1.5V	—	—	1000	ps

NOTE:
1. This parameter is guaranteed by design, but not 100% production tested.

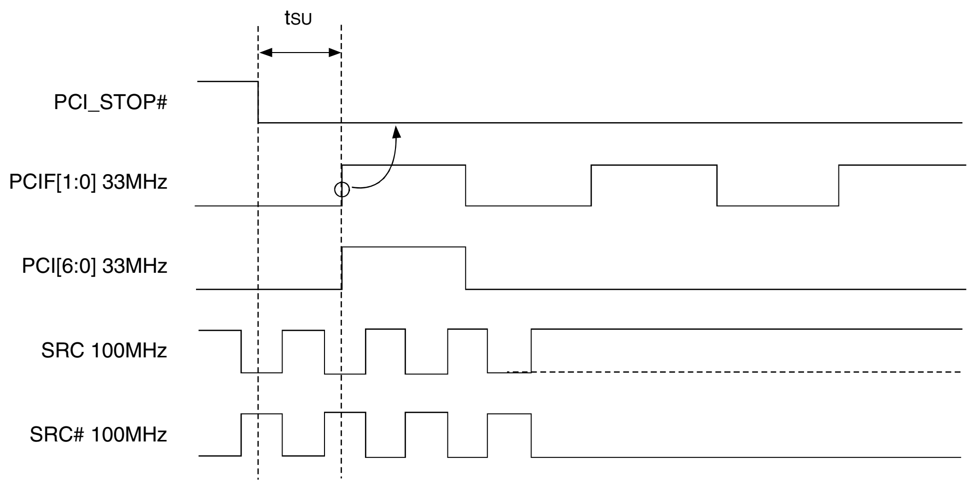
PCI STOP FUNCTIONALITY

The PCI_STOP# signal is on an active low input controlling PCI and SRC outputs. If PCIF[1:0] and SRC clocks can be set to be free-running through SMBus programming, they will ignore both the PCI_STOP# pin and the PCI_STOP register bit.

PCI_STOP#	CPU	CPU#	SRC	SRC#	PCIF/PCI	USB	DOT96	DOT96#	REF
1	Normal	Normal	Normal	Normal	33MHz	48MHz	Normal	Normal	14.318MHz
0	Normal	Normal	I_{REF} * 6 or float	Low	Low	48MHz	Normal	Normal	14.318MHz

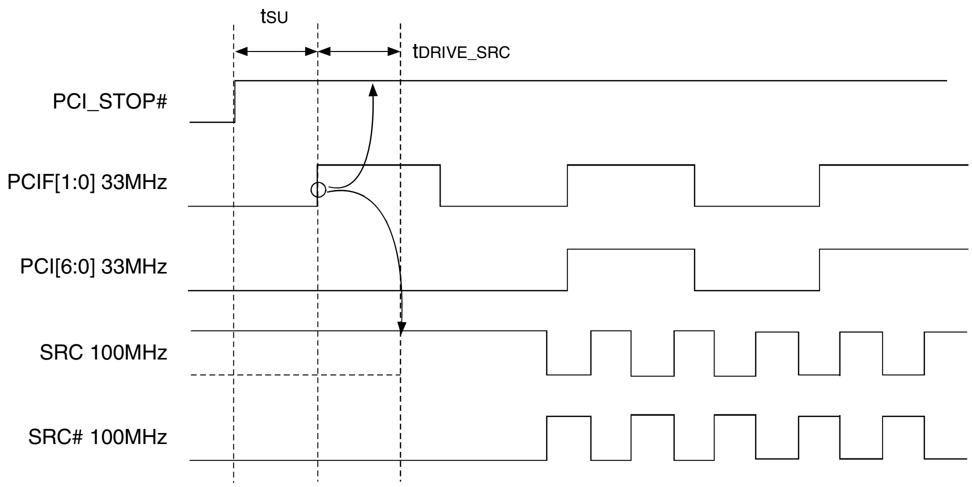
PCI_STOP# ASSERTION (TRANSITION FROM '1' TO '0')

The clock samples the PCI_STOP# signal on a rising edge of PCIF clock. After detecting the PCI_STOP# assertion low, all PCI[6:0] and stoppable PCIF[1:0] clocks will latch low on their next high to low transition. After the PCI clocks are latched low, the SRC clock, (if set to stoppable) will latch high at I_{REF} * 6 (or tristate if Byte 2 Bit 6 = 1) upon its next low to high transition and the SRC# will latch low as shown below.



PCI_STOP# - DE-ASSERTION

The de-assertion of the PCI_STOP# signal is to be sampled on the rising edge of the PCIF free running clock domain. After detecting PCI_STOP# de-assertion, all PCI[6:0], stoppable PCIF[1:0] and stoppable SRC clocks will resume in a glitch free manner.



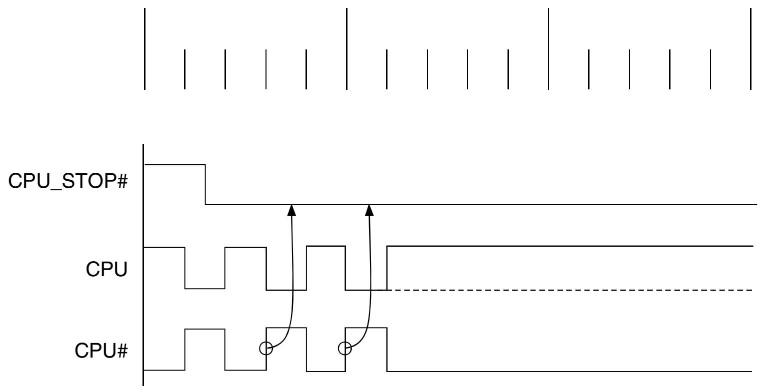
CPU STOP FUNCTIONALITY

The CPU_STOP# signal is an active low input controlling the CPU outputs. This signal can be asserted asynchronously.

CPU_STOP#	CPU	CPU#	SRC	SRC#	PCIF/PCI	USB	DOT96	DOT96#	REF
1	Normal	Normal	Normal	Normal	33MHz	48MHz	Normal	Normal	14.318MHz
0	IREF * 6 or float	Low	Normal	Normal	33MHz	48MHz	Normal	Normal	14.318MHz

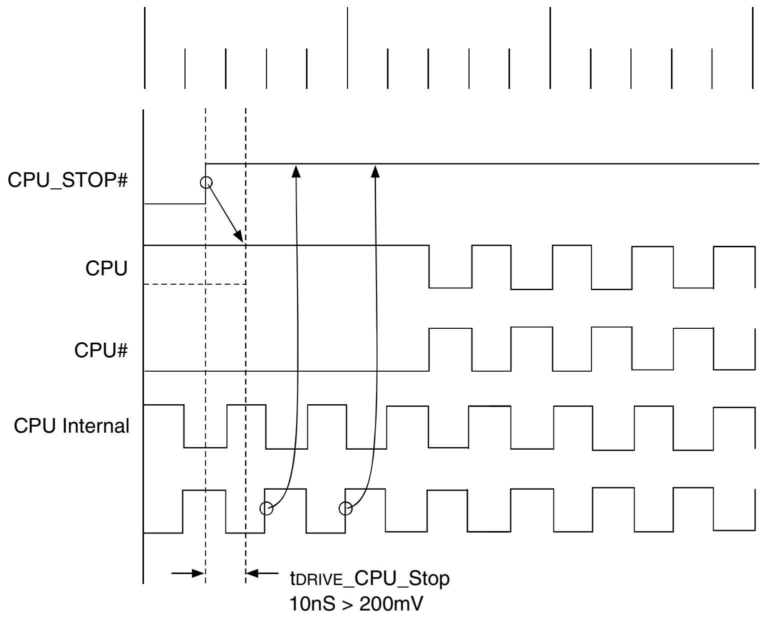
CPU_STOP# ASSERTION (TRANSITION FROM '1' TO '0')

Asserting CPU_STOP# pin stops all CPU outputs that are set to be stoppable after their next transition. When the SMBus CPU_STOP tri-state bit corresponding to the CPU output of interest is programmed to a '0', CPU output will stop CPU_True = High and CPU_Complement = Low. When the SMBus CPU_STOP# tri-state bit corresponding to the CPU output of interest is programmed to a '1', CPU outputs will be tri-stated.



CPU_STOP# - DE-ASSERTION (TRANSITION FROM '0' TO '1')

With the de-assertion of CPU_STOP# all stopped CPU outputs will resume without a glitch. The maximum latency from the de-assertion to active outputs is two to six CPU clock periods. If the control register tristate bit corresponding to the output of interest is programmed to '1', then the stopped CPU outputs will be driven High within 10nS of CPU_STOP# de-assertion to a voltage greater than 200mV.

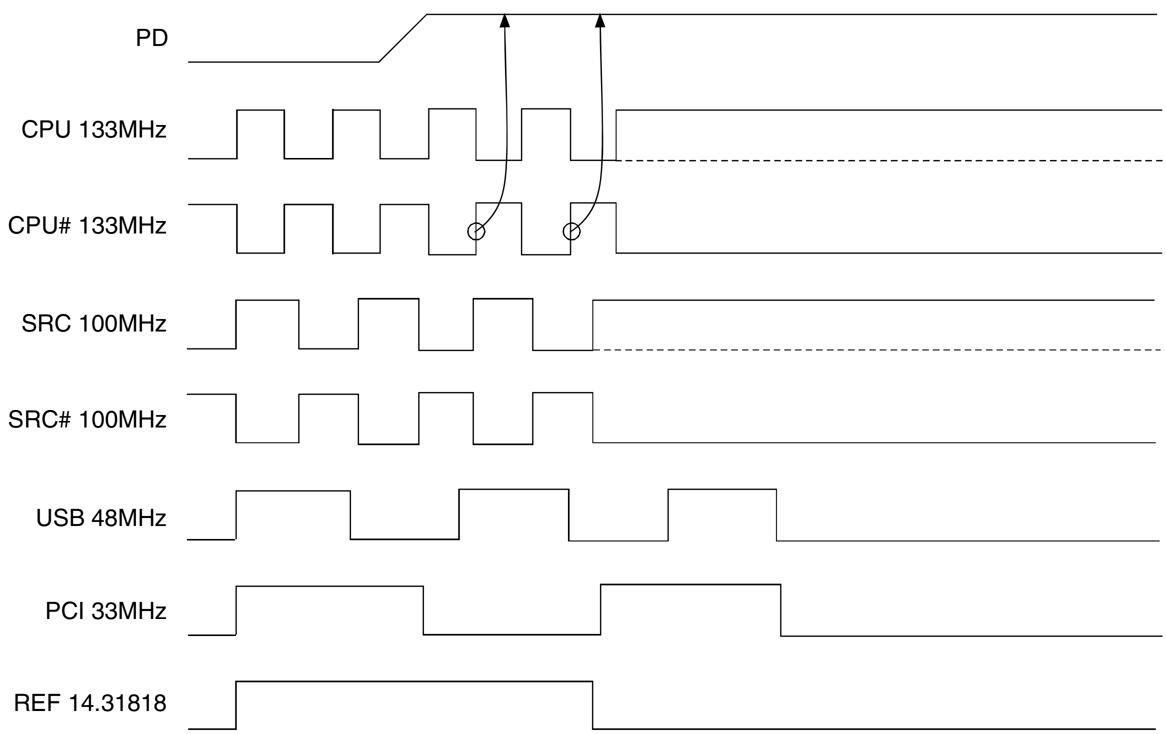


PD, POWER DOWN

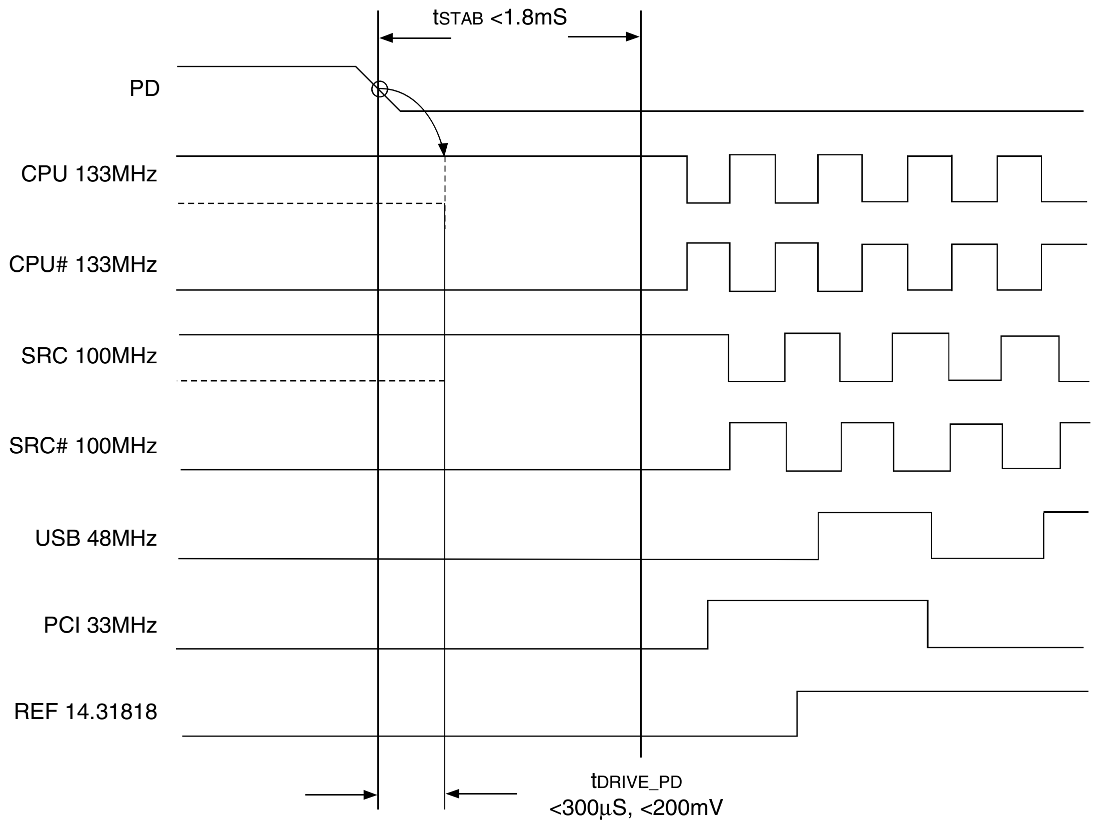
PD is an asynchronous active high input used to shut off all clocks cleanly prior to clock power. When PD is asserted high, all single-ended clocks will be driven low, and CPU# and SRC# will be left floating, before turning off the VCO. In PD de-assertion all clocks will start without glitches.

PD	CPU	CPU#	SRC	SRC#	PCIF/PCI	USB	DOT96	DOT96#	REF
0	Normal	Normal	Normal	Normal	33MHz	48MHz	Normal	Normal	14.318MHz
1	IREF * 2 or float	Float	IREF * 2 or float	Float	Low	Low	IREF * 2 or float	Float	Low

PD ASSERTION



PD DE-ASSERTION



DIFFERENTIAL CLOCK TRISTATE

To minimize power consumption, CPU[2:0] clock outputs are individually configurable through SMBus to be driven or tristated during PD and CPU_STOP# mode and the SRC clock is configurable to be driven or tristated during PCI_STOP# and PD mode. Each differential clock (SRC, CPU[2:0]) output can be disabled by setting the corresponding output's register OE bit to "0" (disable). Disabled outputs are to be tristated regardless of "CPU_STOP", "SRC_STOP" and "PD" register bit settings.

Signal	Pin PD	Pin CPU_STOP#	CPU_STOPTristate Bit	PD Tristate Bit	Non-Stoppable Outputs	Stoppable Outputs
CPU	0	1	X	X	Running	Running
CPU	0	0	0	X	Running	Driven at IREF x 6
CPU	0	0	1	X	Running	Tristate
CPU	1	X	X	0	Driven at IREF x 2	Driven at IREF x 2
CPU	1	X	X	1	Tristate	Tristate

NOTES:
1. Each output has four corresponding control register bits; OE, PD, CPU_STOP, and "Free Running".
2. IREF x 6 and IREF x 2 is the output current in the corresponding mode.
3. See CONTROL REGISTERS section for bit address.

Signal	Pin PD	Pin PCI_STOP#	PCI_STOPTristate Bit	PD Tristate Bit	Non-Stoppable Outputs	Stoppable Outputs
SRC	0	1	X	X	Running	Running
SRC	0	0	0	X	Running	Driven at IREF x 6
SRC	0	0	1	X	Running	Tristate
SRC	1	X	X	0	Driven at IREF x 2	Driven at IREF x 2
SRC	1	X	X	1	Tristate	Tristate

NOTES:
1. SRC output has four corresponding control register bits; OE, PD, SRC_STOP, and "Free Running".
2. IREF x 6 and IREF x 2 is the output current in the corresponding mode.
3. See CONTROL REGISTERS section for bit address.

TRISTATE DOT96 CLOCK CONTROL

Signal	Pin PD	PD Tristate Bit	Output
DOT96	0	X	Running
DOT96	1	0	Driven at IREF x 2
DOT96	1	1	Tristate

NOTES:
1. DOT output has two corresponding control register bits; OE and PD.
2. IREF x 6 and IREF x 2 is the output current in the corresponding mode.
3. See CONTROL REGISTERS section for bit address.

ORDERING INFORMATION

IDTCV XXX XX X

Device Type Package Grade

Grade	Blank	Commercial Temperature Range (0°C to +70°C)
Package	PA	Thin Small Shrink Outline Package
	PAG	TSSOP - Green
Device Type	142	Programmable FlexPC Clock for P4 Processor

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
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