PIN DESCRIPTION

PIN	NAME	FUNCTION
1	A7	Address Input
2	A6	
3	A5	
4	A4	
5	A3	
6	A2	
7	A1	
8	A0	
19	A10	
22	A9	
23	A8	
9	DQ0	Data Input/Output
10	DQ1	
11	DQ2	
13	DQ3	
14	DQ4	
15	DQ5	
16	DQ6	
17	DQ7	
12	GND	Ground
18	CE	Active-Low Chip-Enable Input
20	OE	Active-Low Output-Enable Input
21	WE	Active-Low Write-Enable Input
24	V_{CC}	Power-Supply Input

DESCRIPTION

The DS1742 is a full-function, year 2000-compliant (Y2KC), real-time clock/calendar (RTC) and 2k x 8 nonvolatile static RAM. User access to all registers within the DS1742 is accomplished with a bytewide interface as shown in Figure 1. The RTC information and control bits reside in the eight uppermost RAM locations. The RTC registers contain century, year, month, date, day, hours, minutes, and seconds data in 24-hour BCD format. Corrections for the day of the month and leap year are made automatically.

The RTC clock registers are double-buffered to avoid access of incorrect data that can occur during clock update cycles. The double-buffered system also prevents time loss as the timekeeping countdown continues unabated by access to time register data. The DS1742 also contains its own power-fail circuitry, which deselects the device when the V_{CC} supply is in an out-of-tolerance condition. This feature prevents loss of data from unpredictable system operation brought on by low V_{CC} as errant access and update cycles are avoided.

CLOCK OPERATIONS—READING THE CLOCK

While the double-buffered register structure reduces the chance of reading incorrect data, internal updates to the DS1742 clock registers should be halted before clock data is read to prevent reading of data in transition. However, halting the internal clock register updating process does not affect clock accuracy. Updating is halted when a 1 is written into the read bit, bit 6 of the century register, see Table 2. As long as a 1 remains in that position, updating is halted. After a halt is issued, the registers reflect the count, that is day, date, and time that was current at the moment the halt command was issued. However, the internal clock registers of the double-buffered system continue to update so that the clock accuracy is not affected by the access of data. All of the DS1742 registers are updated simultaneously after the internal clock register updating process has been re-enabled. Updating is within a second after the read bit is written to 0. The READ bit must be a zero for a minimum of 500μs to ensure the external registers will be updated.

Figure 1. DS1742 BLOCK DIAGRAM

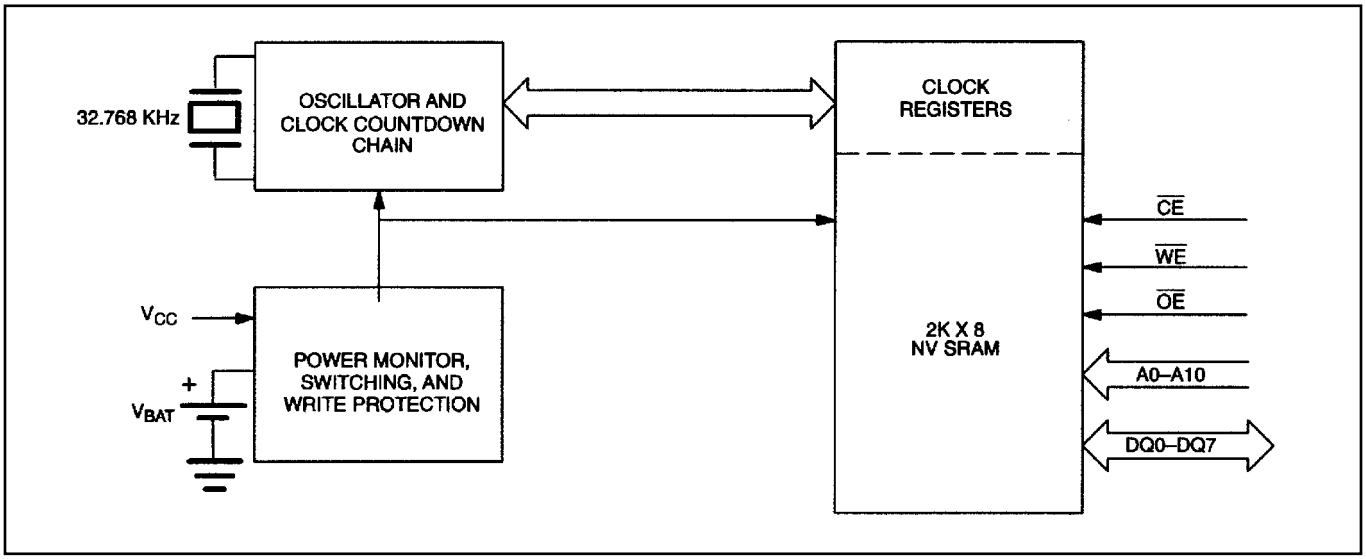


Table 1. TRUTH TABLE

V_{CC}	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	MODE	DQ	POWER
$V_{CC} > V_{PF}$	V_{IH}	X	X	Deselect	High-Z	Standby
	V_{IL}	X	V_{IL}	Write	Data In	Active
	V_{IL}	V_{IL}	V_{IH}	Read	Data Out	Active
	V_{IL}	V_{IH}	V_{IH}	Read	High-Z	Active
$V_{SO} < V_{CC} < V_{PF}$	X	X	X	Deselect	High-Z	CMOS Standby
$V_{CC} < V_{SO} < V_{PF}$	X	X	X	Deselect	High-Z	Data Retention Mode

SETTING THE CLOCK

As shown in Table 2, bit 7 of the Control register is the W (write) bit. Setting the W bit to 1 halts updates to the DS1742 registers. The user can subsequently load correct date and time values into all eight registers, followed by a write cycle of 00h to the Control register to clear the W bit and transfer those new settings into the clock, allowing timekeeping operations to resume from the new set point.

Again referring to Table 2, bit 6 of the Control register is the R (read) bit. Setting the R bit to 1 halts updates to the DS1742 registers. The user can subsequently read the date and time values from the eight registers without those contents possibly changing during those I/O operations. A subsequent write cycle of 00h to the Control register to clear the R bit allows timekeeping operations to resume from the previous set-point.

The pre-existing contents of the Control register bits 0:5 (Century value) are ignored/unmodified by a write cycle to Control if either the W or R bits are being set to 1 in that write operation.

The pre-existing contents of the Control register bits 0:5 (Century value) will be modified by a write cycle to Control if the W bit is being cleared to 0 in that write operation.

The pre-existing contents of the Control register bits 0:5 (Century value) will not be modified by a write cycle to Control if the R bit is being cleared to 0 in that write operation.

STOPPING AND STARTING THE CLOCK OSCILLATOR

The clock oscillator may be stopped at any time. To increase the shelf life, the oscillator can be turned off to minimize current drain from the battery. The $\overline{\text{OSC}}$ bit is the MSB (bit 7) of the seconds registers, see Table 2. Setting it to a 1 stops the oscillator.

FREQUENCY TEST BIT

As shown in Table 2, bit 6 of the day byte is the frequency test bit. When the frequency test bit is set to logic 1 and the oscillator is running, the LSB of the seconds register will toggle at 512 Hz. When the seconds register is being read, the DQ0 line will toggle at the 512 Hz frequency as long as conditions for access remain valid (i.e., $\overline{\text{CE}}$ low, $\overline{\text{OE}}$ low, $\overline{\text{WE}}$ high, and address for seconds register remain valid and stable).

CLOCK ACCURACY

The DS1742 is guaranteed to keep time accuracy to within ±1 minute per month at 25°C. Dallas Semiconductor calibrates the RTC at the factory using nonvolatile tuning elements. The DS1742 does not require additional calibration. For this reason, methods of field clock calibration are not available and not necessary. Clock accuracy is also affected by the electrical environment and caution should be taken to place the RTC in the lowest level EMI section of the PCB layout. For additional information, refer to Application Note 58.

Table 2. REGISTER MAP

ADDRESS	DATA								FUNCTION	RANGE
	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
7FF	10 Year				Year				Year	00–99
7FE	X	X	X	10 Month	Month				Month	01–12
7FD	X	X	10 Date		Date				Date	01–31
7FC	BF	FT	X	X	X	Day			Day	01–07
7FB	X	X	10 Hour		Hour				Hour	00–23
7FA	X	10 Minutes			Minutes				Minutes	00–59
7F9	$\overline{OSC}$	10 Seconds			Seconds				Seconds	00–59
7F8	W	R	10 Century		Century				Control	00–39

OSC = STOP BIT R = READ BIT FT = FREQUENCY TEST

W = WRITE BIT X = SEE NOTE BELOW BF = BATTERY FLAG

Note: *All indicated "X" bits are not used but must be set to "0" during write cycle to ensure proper clock operation.*

RETRIEVING DATA FROM RAM OR CLOCK

The DS1742 is in the read mode whenever $\overline{OE}$ (output enable) is low, $\overline{WE}$ (write enable) is high, and $\overline{CE}$ (chip enable) is low. The device architecture allows ripple-through access to any of the address locations in the NV SRAM. Valid data will be available at the DQ pins within t_{AA} after the last address input is stable, providing that the $\overline{CE}$ and $\overline{OE}$ access times and states are satisfied. If $\overline{CE}$ or $\overline{OE}$ access times and states are not met, valid data will be available at the latter of chip enable access (t_{CEA}) or at output enable access time (t_{OEA}). The state of the data input/output pins (DQ) is controlled by $\overline{CE}$, and $\overline{OE}$. If the outputs are activated before t_{AA}, the data lines are driven to an intermediate state until t_{AA}. If the address inputs are changed while $\overline{CE}$ and $\overline{OE}$ remain valid, output data will remain valid for output data hold time (t_{OH}) but will then go indeterminate until the next address access.

WRITING DATA TO RAM OR CLOCK

The DS1742 is in the write mode whenever $\overline{WE}$ and $\overline{CE}$ are in their active state. The start of a write is referenced to the latter occurring transition of $\overline{WE}$ on $\overline{CE}$. The addresses must be held valid throughout the cycle. $\overline{CE}$ or $\overline{WE}$ must return inactive for a minimum of t_{WR} prior to the initiation of another read or write cycle. Data in must be valid t_{DS} prior to the end of write and remain valid for t_{DH} afterward. In a typical application, the $\overline{OE}$ signal will be high during a write cycle. However, $\overline{OE}$ can be active provided that care is taken with the data bus to avoid bus contention. If $\overline{OE}$ is low prior to $\overline{WE}$ transitioning low the data bus can become active with read data defined by the address inputs. A low transition on $\overline{WE}$ will then disable the outputs t_{WEZ} after $\overline{WE}$ goes active.

DATA RETENTION MODE

The 5V device is fully accessible and data can be written or read only when V_{CC} is greater than V_{PF}. However, when V_{CC} is below the power fail point, V_{PF}, (point at which write protection occurs) the internal clock registers and SRAM are blocked from any access. When V_{CC} falls below the battery switch point V_{SO} (battery supply level), device power is switched from the V_{CC} pin to the backup battery. RTC operation and SRAM data are maintained from the battery until V_{CC} is returned to nominal levels. The 3.3V device is fully accessible and data can be written or read only when V_{CC} is greater than V_{PF}. When V_{CC} falls below the power fail point, V_{PF}, access to the device is inhibited. If V_{PF} is less than Vso, the device power is switched from V_{CC} to the backup supply (V_{BAT}) when V_{CC} drops below V_{PF}. If V_{PF} is greater than Vso, the device power is switched from V_{CC} to the backup supply (V_{BAT}) when V_{CC} drops below Vso. RTC operation and SRAM data are maintained from the battery until V_{CC} is returned to nominal levels.

BATTERY LONGEVITY

The DS1742 has a lithium power source that is designed to provide energy for clock activity, and clock and RAM data retention when the V_{CC} supply is not present. The capability of this internal power supply is sufficient to power the DS1742 continuously for the life of the equipment in which it is installed. For specification purposes, the life expectancy is 10 years at 25°C with the internal clock oscillator running in the absence of V_{CC} power. Each DS1742 is shipped from Dallas Semiconductor with its lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is first applied at a level greater than V_{PF}, the lithium energy source is enabled for battery backup operation. Actual life expectancy of the DS1742 will be much longer than 10 years since no lithium battery energy is consumed when V_{CC} is present.

BATTERY MONITOR

The DS1742 constantly monitors the battery voltage of the internal battery. The Battery Flag bit (bit 7) of the day register is used to indicate the voltage level range of the battery. This bit is not writable and should always be a 1 when read. If a 0 is ever present, an exhausted lithium energy source is indicated and both the contents of the RTC and RAM are questionable.

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……..-0.3V to +6.0V
Storage Temperature Range……...-40°C to +85°C
Soldering Temperature (EDIP, leads)..……..+260°C for 10 seconds (See Note 7)

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Commercial	0°C to +70°C (noncondensing)	3.3V ±10% or 5V ±10%
Industrial	-40°C to +85°C (noncondensing)	3.3V ±10% or 5V ±10%

RECOMMENDED DC OPERATING CONDITIONS

(Over the operating range)

PARAMETER		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1 Voltage (All Inputs)	V_{CC} = 5V ±10%	V_{IH}	2.2		V_{CC} + 0.3V	V	1
	V_{CC} = 3.3V ±10%	V_{IH}	2.0		V_{CC} + 0.3V	V	1
Logic 0 Voltage (All Inputs)	V_{CC} = 5V ±10%	V_{IL}	-0.3		+0.8	V	1
	V_{CC} = 3.3V ±10%	V_{IL}	-0.3		+0.6	V	1

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, Over the operating range.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Active Supply Current	I_{CC}		15	50	mA	2, 3
TTL Standby Current ($\overline{CE}$ = V_{IH})	I_{CC1}		1	3	mA	2, 3
CMOS Standby Current ($\overline{CE}$ ≥V_{CC} - 0.2V)	I_{CC2}		1	3	mA	2, 3
Input Leakage Current (Any Input)	I_{IL}	-1		+1	µA	
Output Leakage Current (Any Output)	I_{OL}	-1		+1	µA	
Output Logic 1 Voltage (I_{OUT} = -1.0mA)	V_{OH}	2.4				1
Output Logic 0 Voltage (I_{OUT} = +2.1mA)	V_{OL}			0.4		1
Write Protection Voltage	V_{PF}	4.25		4.50	V	1
Battery Switchover Voltage	V_{SO}		V_{BAT}			1, 4

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.3V ±10%, Over the operating range.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Active Supply Current	I_{CC}		10	30	mA	2, 3
TTL Standby Current ($\overline{CE}$ = V_{IH})	I_{CC1}		0.7	2	mA	2, 3
CMOS Standby Current ($\overline{CE}$ ≥V_{CC} - 0.2V)	I_{CC2}		0.7	2	mA	2, 3
Input Leakage Current (any input)	I_{IL}	-1		+1	µA	
Output Leakage Current (Any Output)	I_{OL}	-1		+1	µA	
Output Logic 1 Voltage (I_{OUT} = -1.0mA)	V_{OH}	2.4				1
Output Logic 0 Voltage (I_{OUT} =2.1mA)	V_{OL}			0.4		1
Write Protection Voltage	V_{PF}	2.80		2.97	V	1
Battery Switchover Voltage	V_{SO}		V_{BAT} or V_{PF}		V	1, 4

AC CHARACTERISTICS—READ CYCLE (5V)

(V_{CC} = 5.0V ±10%, Over the operating range.)

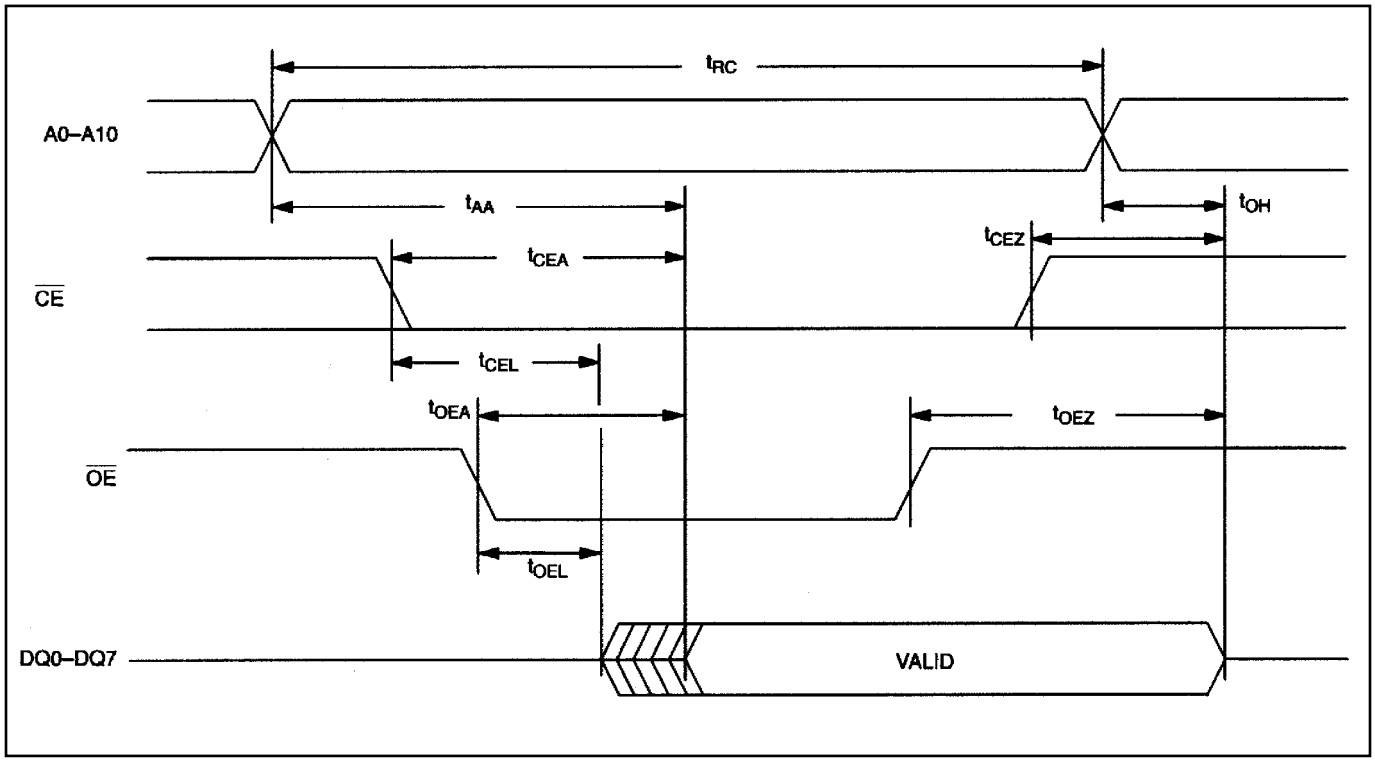
PARAMETER	SYMBOL	85ns ACCESS		100ns ACCESS		UNITS
		MIN	MAX	MIN	MAX	
Read Cycle Time	t_{RC}	85		100		ns
Address Access Time	t_{AA}		85		100	ns
$\overline{CE}$ to DQ Low-Z	t_{CEL}	5		5		ns
$\overline{CE}$ Access Time	t_{CEA}		85		100	ns
$\overline{CE}$ Data Off time	t_{CEZ}		30		35	ns
$\overline{OE}$ to DQ Low-Z	t_{OEL}	5		5		ns
$\overline{OE}$ Access Time	t_{OEA}		45		55	ns
$\overline{OE}$ Data Off Time	t_{OEZ}		30		35	ns
Output Hold from Address	t_{OH}	5		5		ns

AC CHARACTERISTICS—READ CYCLE (3.3V)

(V_{CC} = 3.3V ±10%, Over the operating range.)

PARAMETER	SYMBOL	120ns ACCESS		150ns ACCESS		UNITS
		MIN	MAX	MIN	MAX	
Read Cycle Time	t_{RC}	120		150		ns
Address Access Time	t_{AA}		120		150	ns
$\overline{CE}$ to DQ Low-Z	t_{CEL}	5		5		ns
$\overline{CE}$ Access Time	t_{CEA}		120		150	ns
$\overline{CE}$ Data Off time	t_{CEZ}		40		50	ns
$\overline{OE}$ to DQ Low-Z	t_{OEL}	5		5		ns
$\overline{OE}$ Access Time	t_{OEA}		100		130	ns
$\overline{OE}$ Data Off Time	t_{OEZ}		35		35	ns
Output Hold from Address	t_{OH}	5		5		ns

READ CYCLE TIMING DIAGRAM



AC CHARACTERISTICS—WRITE CYCLE (5V)

(V_{CC} = 5.0V ±10%, Over the operating range.)

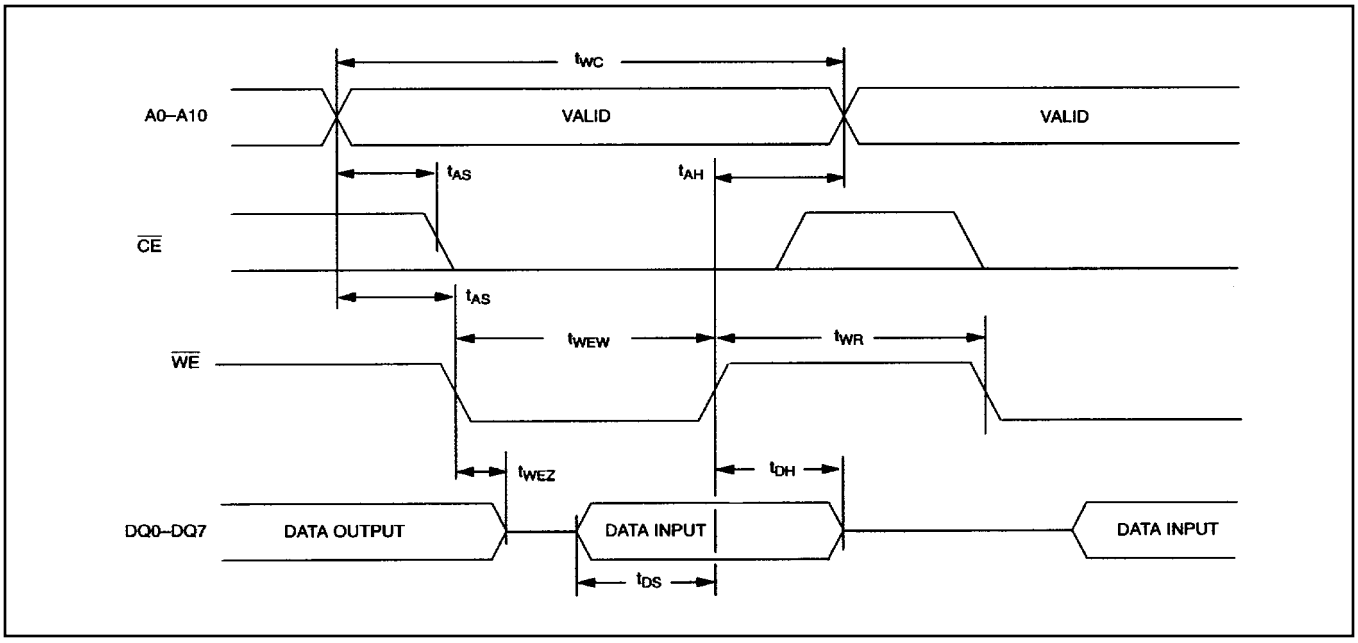
PARAMETER	SYMBOL	85ns ACCESS		100ns ACCESS		UNITS
		MIN	MAX	MIN	MAX	
Write Cycle Time	t_{WC}	85		100		ns
Address Access Time	t_{AS}	0		0		ns
$\overline{WE}$ Pulse Width	t_{WEW}	65		70		ns
$\overline{CE}$ Pulse Width	t_{CEW}	70		75		ns
Data Setup Time	t_{DS}	35		40		ns
Data Hold time	t_{DH}	0		0		ns
Address Hold Time	t_{AH}	5		5		ns
$\overline{WE}$ Data Off Time	t_{WEZ}		30		35	ns
Write Recovery Time	t_{WR}	5		5		ns

AC CHARACTERISTICS—WRITE CYCLE (3.3V)

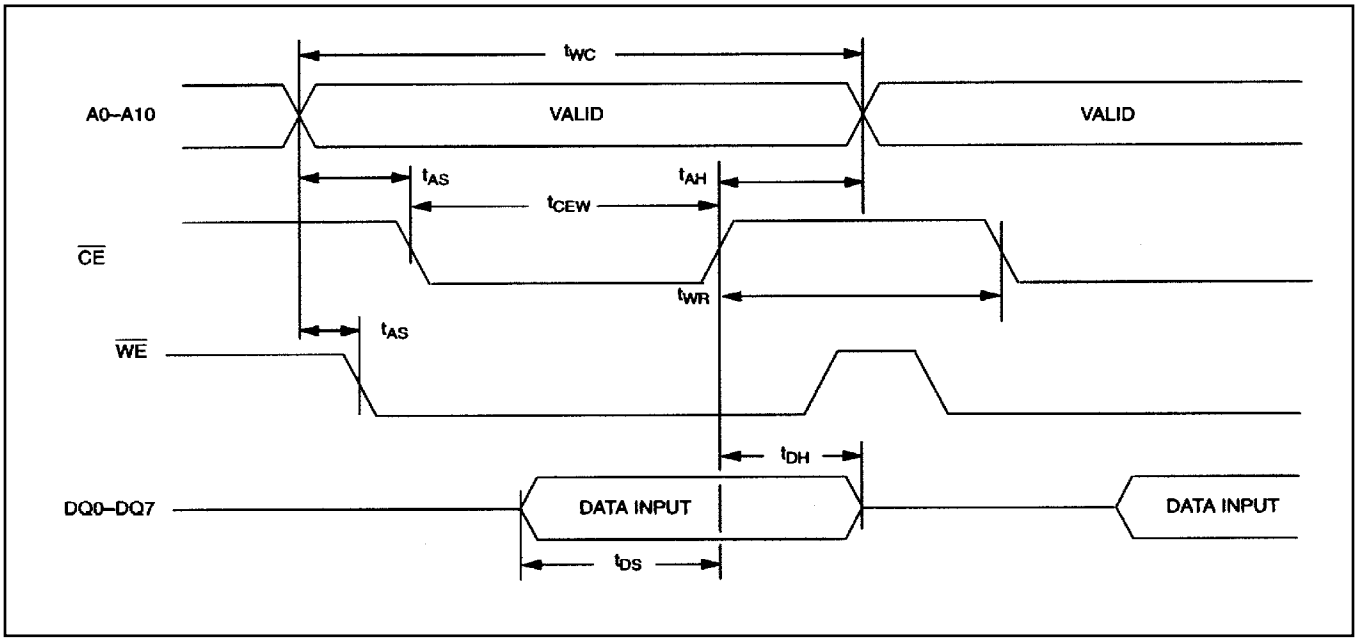
(V_{CC} = 3.3V ±10%, Over the operating range.)

PARAMETER	SYMBOL	120ns ACCESS		150ns ACCESS		UNITS
		MIN	MAX	MIN	MAX	
Write Cycle Time	t_{WC}	120		150		ns
Address Setup Time	t_{AS}	0		0		ns
$\overline{WE}$ Pulse Width	t_{WEW}	100		130		ns
$\overline{CE}$ Pulse Width	t_{CEW}	110		140		ns
Data Setup Time	t_{DS}	80		90		ns
Data Hold Time	t_{DH}	0		0		ns
Address Hold Time	t_{AH}	0		0		ns
$\overline{WE}$ Data Off Time	t_{WEZ}		40		50	ns
Write Recovery Time	t_{WR}	10		10		ns

WRITE CYCLE TIMING DIAGRAM—WRITE-ENABLE CONTROLLED



WRITE CYCLE TIMING DIAGRAM—CHIP-ENABLE CONTROLLED

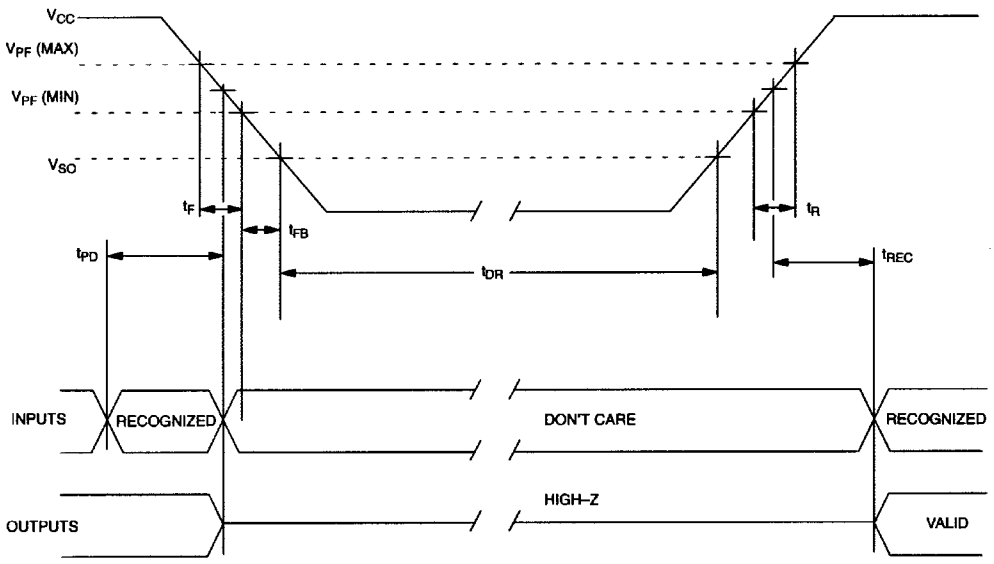


POWER-UP/POWER-DOWN CHARACTERISTICS (5V)

(V_{CC} = 5.0V ±10%, Over the operating range.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ or $\overline{WE}$ at V_{IH}, Before Power-Down	t_{PD}	0			µs	
V_{CC} Fall Time: $V_{PF(MAX)}$ to $V_{PF(MIN)}$	t_F	300			µs	
V_{CC} Fall Time: $V_{PF(MIN)}$ to V_{SO}	t_{FB}	10			µs	
V_{CC} Rise Time: $V_{PF(MIN)}$ to $V_{PF(MAX)}$	t_R	0			µs	
Power-Up Recover Time	t_{REC}			35	ms	
Expected Data Retention Time (Oscillator On)	t_{DR}	10			years	5, 6

POWER-UP/POWER-DOWN WAVEFORM TIMING (5V DEVICE)

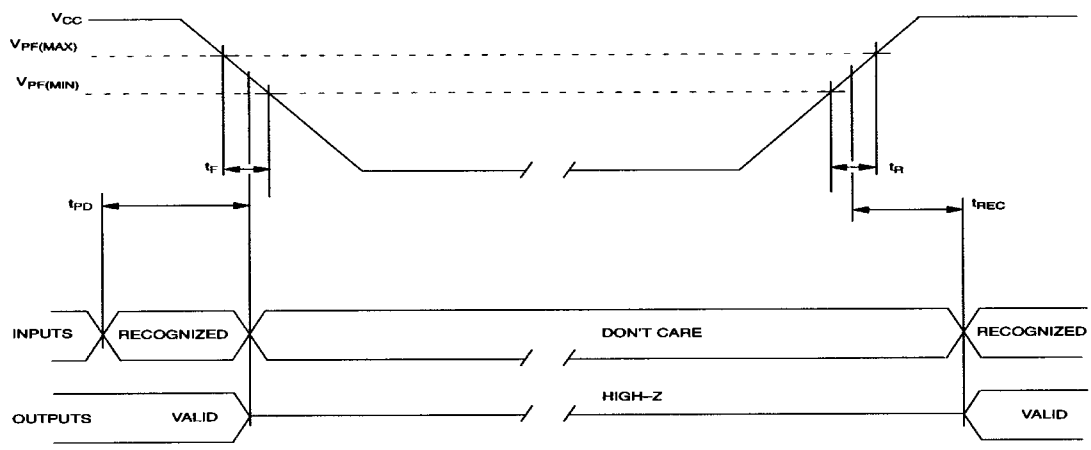


POWER-UP/POWER-DOWN CHARACTERISTICS (3.3V)

(V_{CC} = 3.3V ±10%, Over the operating range.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ or $\overline{WE}$ at V_{IH}, Before Power-Down	t_{PD}	0			µs	
V_{CC} Fall Time: $V_{PF(MAX)}$ to $V_{PF(MIN)}$	t_F	300			µs	
V_{CC} Rise Time: $V_{PF(MIN)}$ to $V_{PF(MAX)}$	t_R	0			µs	
Power-Up Recovery Time	t_{REC}			35	ms	
Expected Data Retention Time (Oscillator On)	t_{DR}	10			years	5, 6

POWER-UP/POWER-DOWN WAVEFORM TIMING (3.3V DEVICE)



CAPACITANCE

(T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Capacitance on All Input Pins	C_{IN}			7	pF	
Capacitance on All Output Pins	C_O			10	pF	

AC TEST CONDITIONS

Output Load: 100pF + 1TTL Gate
Input Pulse Levels: 0.0 to 3.0V
Timing Measurement Reference Levels:
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

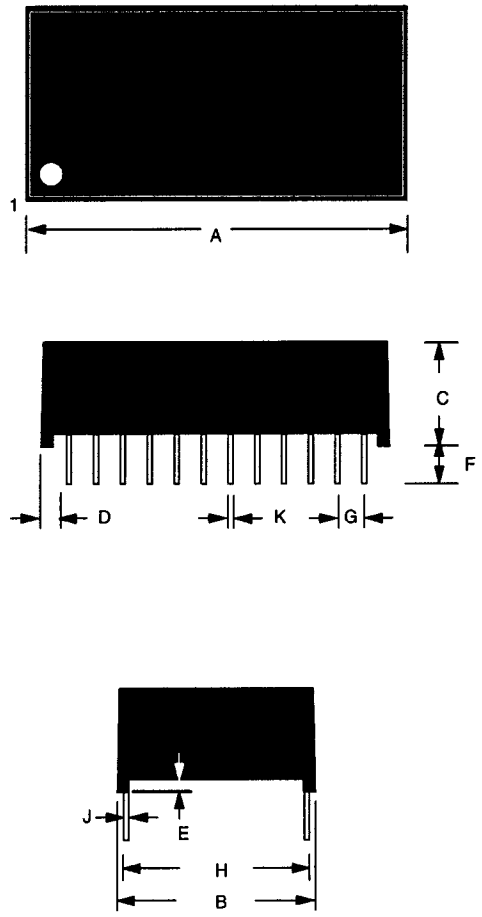
NOTES:

1) Voltage referenced to ground.
2) Typical values are at +25°C and nominal supplies.
3) Outputs are open.
4) Battery switchover occurs at the lower of either the battery voltage or V_{PF}.
5) Data retention time is at +25°C.
6) Each DS1742 has a built-in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as a cumulative time in the absence of V_{CC} starting from the time power is first applied by the user.
7) Real-time clock modules can be successfully processed through conventional wave-soldering techniques as long as temperature exposure to the lithium energy source contained within does not exceed +85°C. Post-solder cleaning with water washing techniques is acceptable, provided that ultrasonic vibration is not used to prevent damage to the crystal.

PACKAGE INFORMATION

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages.** Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
24 EDIP	MDF24+1	21-0245	—



PKG	24–PIN	
DIM	MIN	MAX
A IN.	1.270	1.290
MM	37.34	37.85
B IN.	0.675	0.700
MM	17.15	17.78
C IN.	0.315	0.335
MM	8.00	8.51
D IN.	0.075	0.105
MM	1.91	2.67
E IN.	0.015	0.030
MM	0.38	0.76
F IN.	0.140	0.180
MM	3.56	4.57
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.010	0.018
MM	0.25	0.45
K IN.	0.015	0.025
MM	0.43	0.58

REVISION HISTORY

REVISION DATE	DESCRIPTION	PAGES CHANGED
041305	Added “UL Recognized” bullet to *Features* and new *Ordering Information* table	1
	Added new *Pin Description* table	2
	Updated note for Table 2	4
	updated Operating Temperature Range for *Absolute Maximum Ratings*	7
071905	Corrected 24-pin to 28-pin package and top mark items in *Ordering Information* table	1
060706	Removed reference to J-STD-020 and indicated the lead soldering temperature of +260°C for 10 seconds max	7
022207	Added DS1742-85, DS1742-85+ to the *Ordering Information* table; removed DS1742P-100+ (PowerCap) package	1
102808	Removed the –70 ordering numbers from the *Ordering Information* table	1
6/13	Updated the *Ordering Information* table and the *Setting the Clock* section	1, 4

Maxim Integrated 160 Rio Robles, San Jose, CA 95134 USA 1-408-601-1000

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