8th-Order, Lowpass, Elliptic, Switched-Capacitor Filters

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND
  MAX7400/MAX7403 .....-0.3V to +6V
  MAX7404/MAX7407 .....-0.3V to +4V
IN, OUT, COM, OS, CLK .....-0.3V to (V_{DD} + 0.3V)
$\overline{SHDN}$.....-0.3V to +6V
OUT Short-Circuit Duration.....1sec

Continuous Power Dissipation (T_A = +70°C)
  SO (derate 5.88mW/°C above +70°C).....471mW
  DIP (derate 9.1mW/°C above +70°C).....727mW
Operating Temperature Ranges
  MAX740_C_A .....0°C to +70°C
  MAX740_E_A .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX7400/MAX7403

(V_{DD} = +5V, filter output measured at OUT, 10kΩ || 50pF load to GND at OUT, $\overline{SHDN}$ = V_{DD}, OS = COM, 0.1µF from COM to GND, f_{CLK} = 100kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
FILTER CHARACTERISTICS							
Corner Frequency	f_C	(Note 1)			0.001 to 10		kHz
Clock-to-Corner Ratio	f_{CLK}/f_C				100:1		
Clock-to-Corner Tempco					10		ppm/°C
Output Voltage Range				0.25		V_{DD} - 0.25	V
Output Offset Voltage	V_{OFFSET}	V_{IN} = V_{COM} = V_{DD} / 2			±5	±25	mV
DC Insertion Gain with Output Offset Removed		V_{COM} = V_{DD} / 2 (Note 2)		-0.1	0.15	0.3	dB
Total Harmonic Distortion plus Noise	THD+N	f_{IN} = 200Hz, V_{IN} = 4Vp-p, measurement bandwidth = 22kHz	MAX7400		-82		dB
			MAX7403		-80		
OS Voltage Gain to OUT	A_{OS}				1		V/V
Input Voltage Range at OS	V_{OS}				V_{COM} ±0.1		V
COM Voltage Range	V_{COM}	Input, COM externally driven		V_{DD} / 2 - 0.5	V_{DD} / 2	V_{DD} / 2 + 0.5	V
		Output, COM internally biased		V_{DD} / 2 - 0.2	V_{DD} / 2	V_{DD} / 2 + 0.2	
Input Resistance at COM	R_{COM}			75	125		kΩ
Clock Feedthrough					10		mVp-p
Resistive Output Load Drive	R_L			10	1		kΩ
Maximum Capacitive Load at OUT	C_L			50	500		pF
Input Leakage Current at COM		$\overline{SHDN}$ = GND, V_{COM} = 0 to V_{DD}			±0.1	±10	µA
Input Leakage Current at OS		V_{OS} = 0 to (V_{DD} - 1V) (Note 3)			±0.1	±10	µA
CLOCK							
Internal Oscillator Frequency	f_{OSC}	C_{OSC} = 1000pF (Note 4)		29	38	48	kHz
Clock Input Current	I_{CLK}	V_{CLK} = 0 or 5V			±15	±30	µA
Clock Input High	V_{IH}			V_{DD} - 0.5			V
Clock Input Low	V_{IL}					0.5	V

ELECTRICAL CHARACTERISTICS—MAX7400/MAX7403 (continued)

(V_{DD} = +5V, filter output measured at OUT, 10kΩ || 50pF load to GND at OUT, $\overline{SHDN}$ = V_{DD}, OS = COM, 0.1µF from COM to GND, f_{CLK} = 100kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER REQUIREMENTS						
Supply Voltage	V_{DD}		4.5		5.5	V
Supply Current	I_{DD}	Operating mode, no load, IN = OS = COM		2	3.5	mA
Shutdown Current	$I_{\overline{SHDN}}$	$\overline{SHDN}$ = GND, CLK driven from 0 to V_{DD}		0.2	1	µA
Power-Supply Rejection Ratio	PSRR	Measured at DC		60		dB
SHUTDOWN						
$\overline{SHDN}$ Input High	V_{SDH}		V_{DD} - 0.5			V
$\overline{SHDN}$ Input Low	V_{SDL}				0.5	V
$\overline{SHDN}$ Input Leakage Current		$V_{\overline{SHDN}}$ = 0 to V_{DD}		±0.1	±10	µA

ELECTRICAL CHARACTERISTICS—MAX7404/MAX7407

(V_{DD} = +3V, filter output measured at OUT, 10kΩ || 50pF load to GND at OUT, $\overline{SHDN}$ = V_{DD}, OS = COM, 0.1µF from COM to GND, f_{CLK} = 100kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
FILTER CHARACTERISTICS							
Corner Frequency	f_C	(Note 1)			0.001 to 10		kHz
Clock-to-Corner Ratio	f_{CLK}/f_C				100:1		
Clock-to-Corner Tempco					10		ppm/°C
Output Voltage Range				0.25		V_{DD} - 0.25	V
Output Offset Voltage	V_{OFFSET}	V_{IN} = V_{COM} = V_{DD} / 2			±5	±25	mV
DC Insertion Gain with Output Offset Removed		V_{COM} = V_{DD} / 2 (Note 2)		-0.1	0.1	0.3	dB
Total Harmonic Distortion plus Noise	THD+N	f_{IN} = 200Hz, V_{IN} = 2.5Vp-p, measurement bandwidth = 22kHz	MAX7404		-79		dB
			MAX7407		-77		
OS Voltage Gain to OUT	A_{OS}				1		V/V
Input Voltage Range at OS	V_{OS}				V_{COM} ±0.1		V
COM Voltage Range	V_{COM}	COM internally biased or externally driven		V_{DD} / 2 - 0.1	V_{DD} / 2	V_{DD} / 2 + 0.1	V
Input Resistance at COM	R_{COM}			75	125		kΩ
Clock Feedthrough					10		mVp-p
Resistive Output Load Drive	R_L			10	1		kΩ
Maximum Capacitive Load at OUT	C_L			50	500		pF
Input Leakage Current at COM		$\overline{SHDN}$ = GND, V_{COM} = 0 to V_{DD}			±0.1	±10	µA
Input Leakage Current at OS		V_{OS} = 0 to (V_{DD} - 1V) (Note 3)			±0.1	±10	µA

ELECTRICAL CHARACTERISTICS—MAX7404/MAX7407 (continued)

(V_{DD} = +3V, filter output measured at OUT, 10kΩ || 50pF load to GND at OUT, $\overline{SHDN}$ = V_{DD}, OS = COM, 0.1µF from COM to GND, f_{CLK} = 100kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLOCK						
Internal Oscillator Frequency	f_{OSC}	C_{OSC} = 1000pF (Note 4)	26	34	43	kHz
Clock Input Current	I_{CLK}	V_{CLK} = 0 or 3V		±15	±30	µA
Clock Input High	V_{IH}		V_{DD} - 0.5			V
Clock Input Low	V_{IL}				0.5	V
POWER REQUIREMENTS						
Supply Voltage	V_{DD}		2.7		3.6	V
Supply Current	I_{DD}	Operating mode, no load, IN = OS = COM		2	3.5	mA
Shutdown Current	$I_{\overline{SHDN}}$	$\overline{SHDN}$ = GND, CLK driven from 0 to V_{DD}		0.2	1	µA
Power-Supply Rejection Ratio	PSRR	Measured at DC		60		dB
SHUTDOWN						
$\overline{SHDN}$ Input High	V_{SDH}		V_{DD} - 0.5			V
$\overline{SHDN}$ Input Low	V_{SDL}				0.5	V
$\overline{SHDN}$ Input Leakage Current		$V_{\overline{SHDN}}$ = 0 to V_{DD}		±0.1	±10	µA

ELLIPTIC (r = 1.5) FILTER CHARACTERISTICS—MAX7400/MAX7404

(V_{DD} = +5V for MAX7400, V_{DD} = +3V for MAX7404; filter output measured at OUT; 10kΩ || 50pF load to GND at OUT; $\overline{SHDN}$ = V_{DD}; V_{COM} = V_{OS} = V_{DD} / 2; f_{CLK} = 100kHz; T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Insertion Gain Relative to DC Gain (Note 5)	f_{IN} = 0.371f_C	-0.20	-0.10	0.20	dB
	f_{IN} = 0.587f_C	-0.20	0.02	0.20	
	f_{IN} = 0.737f_C	-0.20	-0.08	0.20	
	f_{IN} = 0.868f_C	-0.20	0.06	0.20	
	f_{IN} = 0.940f_C	-0.20	-0.03	0.20	
	f_{IN} = 0.988f_C	-0.20	0.09	0.25	
	f_{IN} = 1.000f_C	-0.20	0.02	0.25	
	f_{IN} = 1.500f_C		-82	-75	
	f_{IN} = 1.601f_C		-84	-78	
	f_{IN} = 2.020f_C		-83	-78	
	f_{IN} = 4.020f_C		-85	-78	

ELLIPTIC (r = 1.2) FILTER CHARACTERISTICS—MAX7403/MAX7407

(V_{DD} = +5V for MAX7403, V_{DD} = +3V for MAX7407; filter output measured at OUT; 10kΩ ‖ 50pF load to GND at OUT; $\overline{SHDN}$ = V_{DD}; V_{COM} = V_{OS} = V_{DD} / 2; f_{CLK} = 100kHz; T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Insertion Gain Relative to DC Gain (Note 5)	f_{IN} = 0.408f_C	-0.20	-0.11	0.20	dB
	f_{IN} = 0.640f_C	-0.20	0.02	0.20	
	f_{IN} = 0.784f_C	-0.20	-0.06	0.20	
	f_{IN} = 0.902f_C	-0.20	0.10	0.20	
	f_{IN} = 0.956f_C	-0.20	0.02	0.20	
	f_{IN} = 0.992f_C	-0.20	0.14	0.30	
	f_{IN} = 1.000f_C	-0.20	0.09	0.30	
	f_{IN} = 1.200f_C		-58	-50	
	f_{IN} = 1.261f_C		-59	-54	
	f_{IN} = 1.533f_C		-60	-54	
	f_{IN} = 2.875f_C		-60	-54	

Note 1: The maximum f_C is defined as the clock frequency, f_{CLK} = 100 • f_C, at which the peak SINAD drops to 68dB with a sinusoidal input at 0.2f_C.

Note 2: DC insertion gain is defined as ΔV_{OUT} / ΔV_{IN}.

Note 3: OS voltages above V_{DD} - 1V saturate the input and result in a 75µA typical input leakage current.

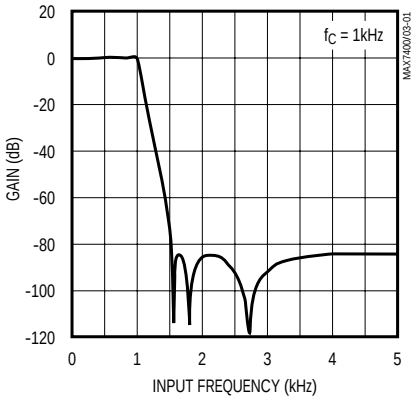
Note 4: For MAX7400/MAX7403, f_{OSC} (kHz) ≅ 38 • 10^3 / C_{OSC} (pF). For MAX7404/MAX7407, f_{OSC} (kHz) ≅ 34 • 10^3 / C_{OSC} (pF).

Note 5: The input frequencies, f_{IN}, are selected at the peaks and troughs of the frequency responses.

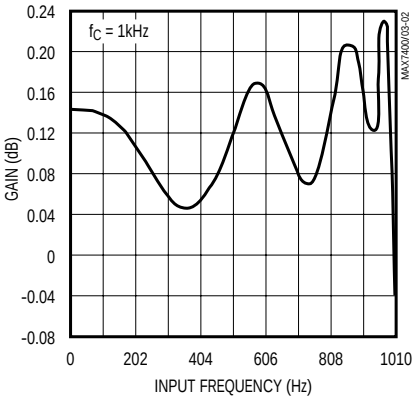
Typical Operating Characteristics

(V_{DD} = +5V for MAX7400/MAX7403, V_{DD} = +3V for MAX7404/MAX7407; V_{COM} = V_{OS} = V_{DD} / 2; $\overline{SHDN}$ = V_{DD}; f_{CLK} = 100kHz; T_A = +25°C; unless otherwise noted.)

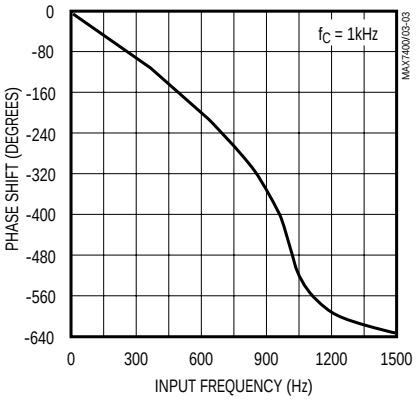
MAX7400/MAX7404 (r = 1.5)
FREQUENCY RESPONSE



MAX7400/MAX7404 (r = 1.5)
PASSBAND FREQUENCY RESPONSE



MAX7400/MAX7404 (r = 1.5)
PHASE RESPONSE

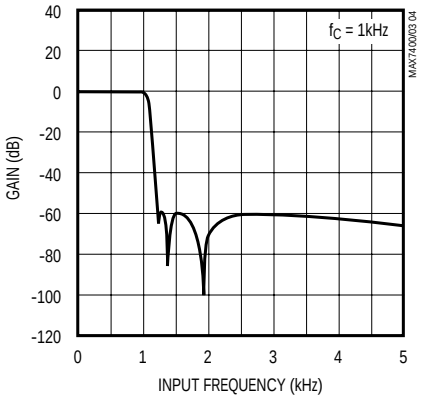


8th-Order, Lowpass, Elliptic, Switched-Capacitor Filters

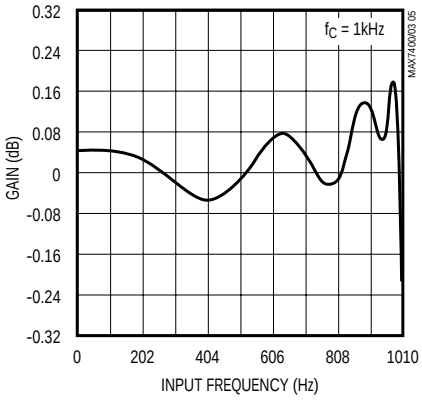
Typical Operating Characteristics (continued)

(V_{DD} = +5V for MAX7400/MAX7403, V_{DD} = +3V for MAX7404/MAX7407; V_{COM} = V_{OS} = V_{DD} / 2; $\overline{SHDN}$ = V_{DD}; f_{CLK} = 100kHz; T_A = +25°C; unless otherwise noted.)

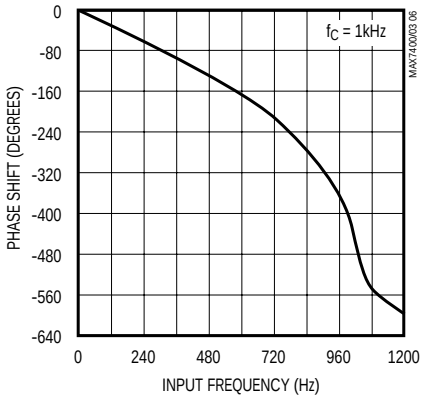
MAX7403/MAX7407 (r = 1.2)
FREQUENCY RESPONSE



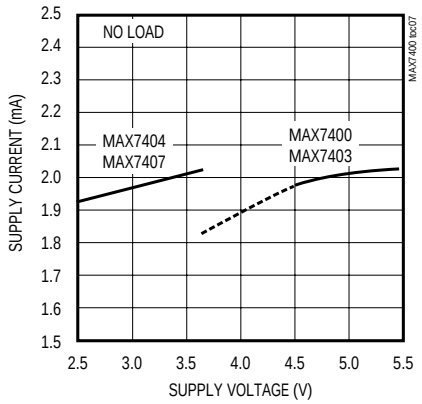
MAX7403/MAX7407 (r = 1.2)
PASSBAND FREQUENCY RESPONSE



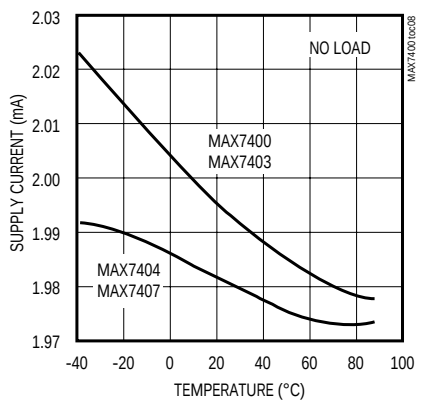
MAX7403/MAX7407 (r = 1.2)
PHASE RESPONSE



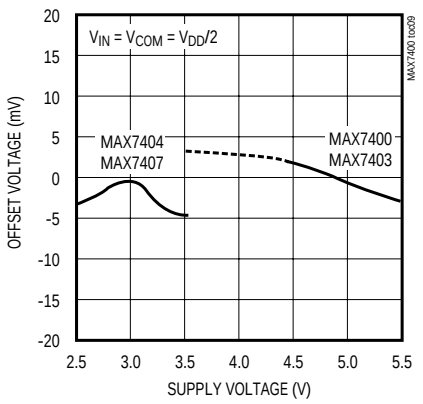
SUPPLY CURRENT
vs. SUPPLY VOLTAGE



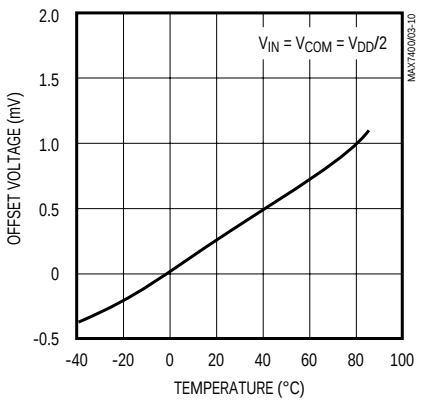
SUPPLY CURRENT
vs. TEMPERATURE



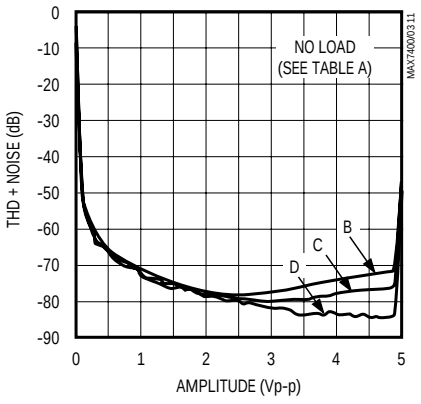
OFFSET VOLTAGE
vs. SUPPLY VOLTAGE



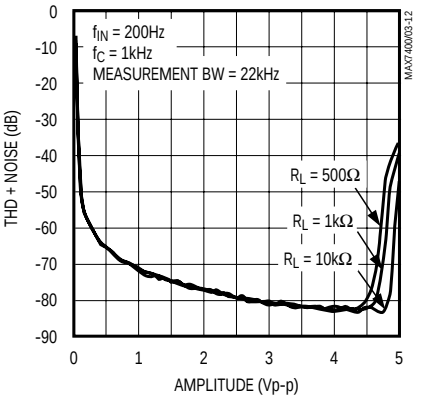
OFFSET VOLTAGE vs. TEMPERATURE



THD PLUS NOISE vs. INPUT SIGNAL
AMPLITUDE (MAX7400)



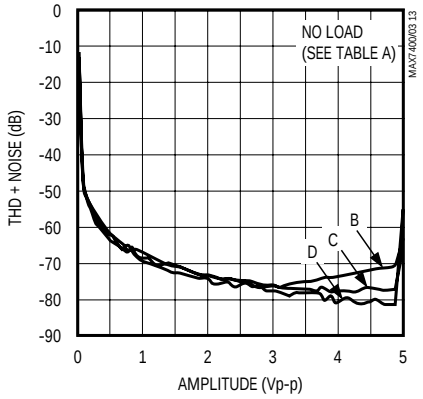
THD PLUS NOISE vs. INPUT SIGNAL
AMPLITUDE AND RESISTIVE LOAD (MAX7400)



Typical Operating Characteristics (continued)

(V_{DD} = +5V for MAX7400/MAX7403, V_{DD} = +3V for MAX7404/MAX7407; V_{COM} = V_{OS} = V_{DD} / 2; $\overline{SHDN}$ = V_{DD}; f_{CLK} = 100kHz; T_A = +25°C; unless otherwise noted.)

THD PLUS NOISE vs. INPUT SIGNAL AMPLITUDE (MAX7403)



THD PLUS NOISE vs. INPUT SIGNAL AMPLITUDE AND RESISTIVE LOAD (MAX7403)

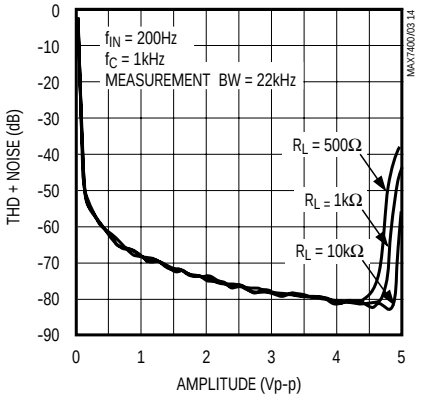
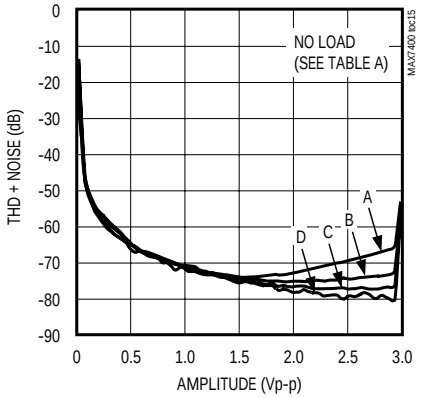


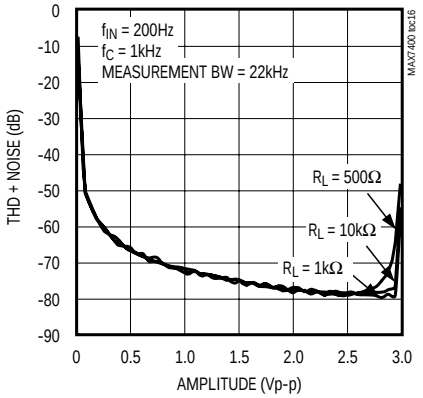
TABLE A. THD PLUS NOISE vs. INPUT SIGNAL AMPLITUDE TEST CONDITIONS

TRACE	f_{IN} (Hz)	f_C (kHz)	f_{CLK} (kHz)	MEASUREMENT BANDWIDTH (kHz)
A	2800	14	1400	80
B	2000	10	1000	80
C	1000	5	500	80
D	200	1	100	22

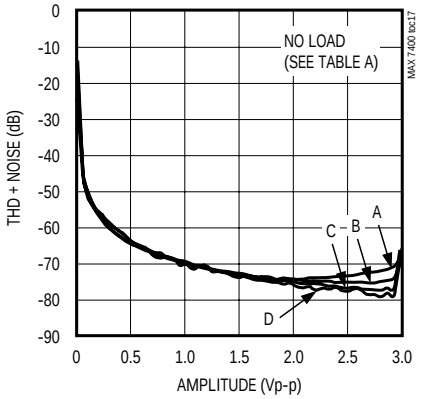
THD PLUS NOISE vs. INPUT SIGNAL AMPLITUDE (MAX7404)



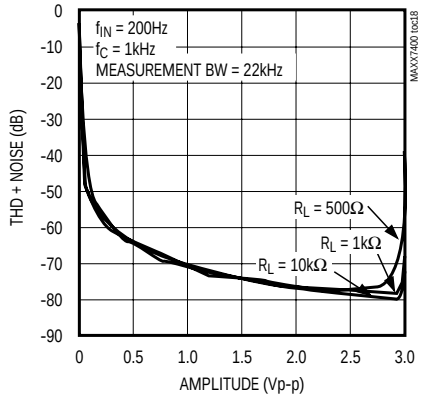
THD PLUS NOISE vs. INPUT SIGNAL AMPLITUDE AND RESISTIVE LOAD (MAX7404)



THD PLUS NOISE vs. INPUT SIGNAL AMPLITUDE (MAX7407)



THD PLUS NOISE vs. INPUT SIGNAL AMPLITUDE AND RESISTIVE LOAD (MAX7407)

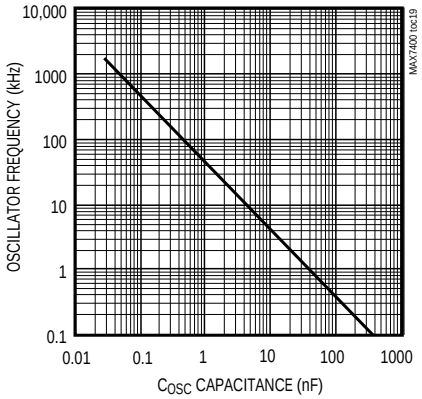


8th-Order, Lowpass, Elliptic, Switched-Capacitor Filters

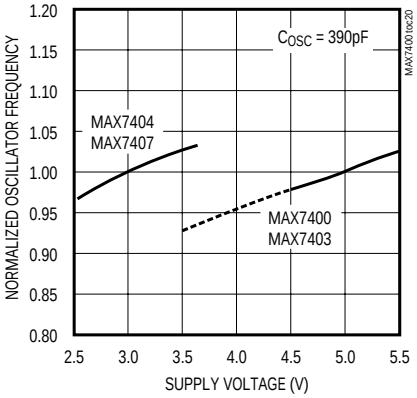
Typical Operating Characteristics (continued)

(V_{DD} = +5V for MAX7400/MAX7403, V_{DD} = +3V for MAX7404/MAX7407; V_{COM} = V_{OS} = V_{DD} / 2; $\overline{SHDN}$ = V_{DD}; f_{CLK} = 100kHz; T_A = +25°C; unless otherwise noted.)

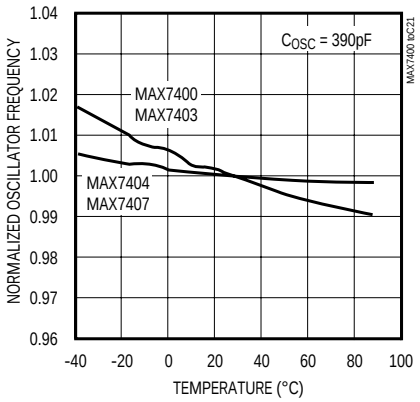
INTERNAL OSCILLATOR FREQUENCY vs. C_{OSC} CAPACITANCE



NORMALIZED OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE



NORMALIZED OSCILLATOR FREQUENCY vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1	COM	Common Input. Biased internally at midsupply. Bypass externally to GND with a 0.1µF capacitor. To override internal biasing, drive with an external supply.
2	IN	Filter Input
3	GND	Ground
4	V_{DD}	Positive Supply Input: +5V for MAX7400/MAX7403, +3V for MAX7404/MAX7407
5	OUT	Filter Output
6	OS	Offset Adjust Input. To adjust output offset, bias OS externally. Connect OS to COM if no offset adjustment is needed. Refer to *Offset and Common-Mode Input Adjustment* section.
7	$\overline{SHDN}$	Shutdown Input. Drive low to enable shutdown mode; drive high or connect to V_{DD} for normal operation.
8	CLK	Clock Input. To override the internal oscillator, connect to an external clock; otherwise, connect an external capacitor (C_{OSC}) from CLK to GND to set the internal oscillator frequency.

Detailed Description

The MAX7400/MAX7403/MAX7404/MAX7407 family of 8th-order, lowpass filters provides sharp rolloff with good stopband rejection. All parts operate with a 100:1 clock-to-corner frequency ratio and a 10kHz maximum corner frequency. These devices accept a single +5V (MAX7400/MAX7403) or +3V (MAX7404/MAX7407) supply. Figure 1 shows the functional diagram.

Most switched-capacitor filters (SFCs) are designed with biquadratic sections. Each section implements two filtering poles, and the sections can be cascaded to produce higher-order filters. The advantage of this approach is ease of design. However, this type of design is highly sensitive to component variations if any section's Q is high. The MAX7400 family uses an alternative approach, which is to emulate a passive network using switched-capacitor integrators with summing and scaling. The passive network can be synthesized using CAD programs or can be found in many filter books. Figure 2 shows a basic 8th-order ladder elliptic filter structure.

A switched-capacitor filter that emulates a passive ladder filter retains many of the same advantages. The component sensitivity of a passive ladder filter is low when compared to a cascaded biquadratic design, because each component affects the entire filter shape rather than a single pole-zero pair. In other words, a mismatched component in a biquadratic design has a concentrated error on its respective poles, while the same mismatch in a ladder filter design spreads its error over all poles.

Elliptic Characteristics

Lowpass, elliptic filters such as the MAX7400/MAX7403/MAX7404/MAX7407 provide the steepest possible rolloff with frequency of the four most common filter types (Butterworth, Bessel, Chebyshev, and Elliptic). Figure 3 shows the 8th-order elliptic filter response. The high Q value of the poles near the passband edge combined with the stopband zeros allows for the sharp attenuation characteristic of elliptic filters, making these devices ideal for anti-aliasing and post-DAC filtering in single-supply systems (see the *Anti-Aliasing and Post-DAC Filtering* section).

In the frequency domain, the first transmission zero causes the filter's amplitude to drop to a minimum level. Beyond this zero, the response rises as the frequency increases until the next transmission zero. The stopband begins at the stopband frequency, f_S. At frequencies above f_S, the filter's gain does not exceed the gain at f_S.

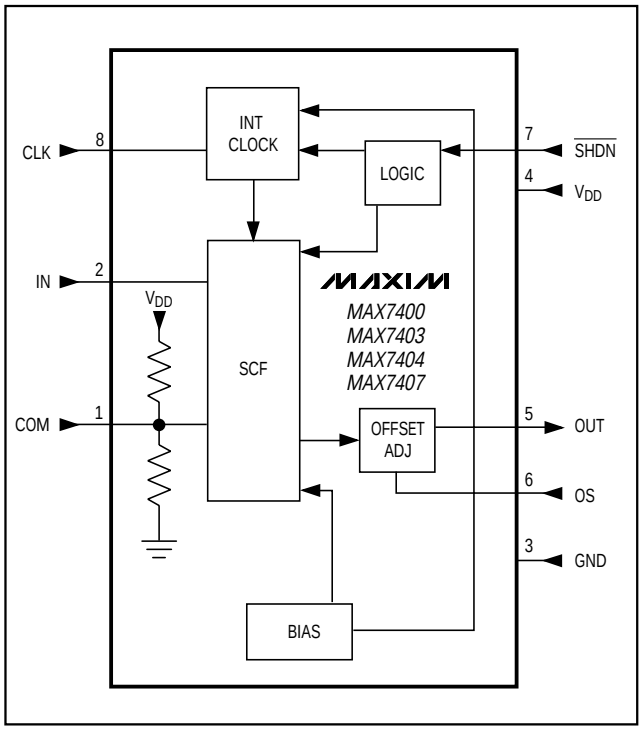


Figure 1. Functional Diagram

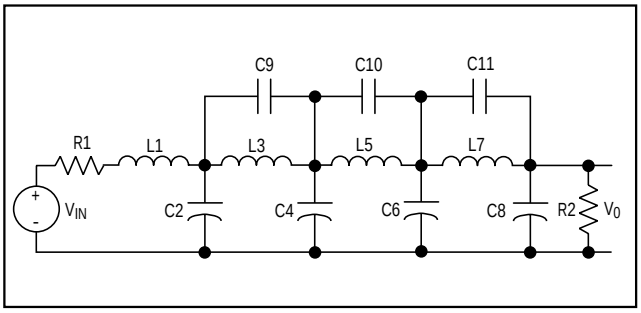


Figure 2. 8th-Order Ladder Filter Network

The corner frequency, f_C, is defined as the point where the filter output attenuation falls just below the passband ripple. The transition ratio is defined as the ratio of the stopband frequency to the corner frequency:

$$r = f_S / f_C$$

The MAX7400/MAX7404 have a transition ratio of 1.5 and a typical stopband rejection of 82dB. The MAX7403/MAX7407 have a transition ratio of 1.2 (providing the steepest rolloff) and a typical stopband rejection of 60dB.

8th-Order, Lowpass, Elliptic, Switched-Capacitor Filters

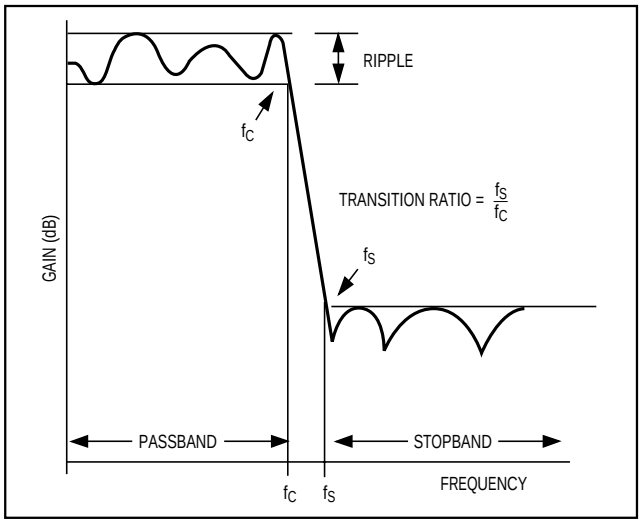


Figure 3. Elliptic Filter Response

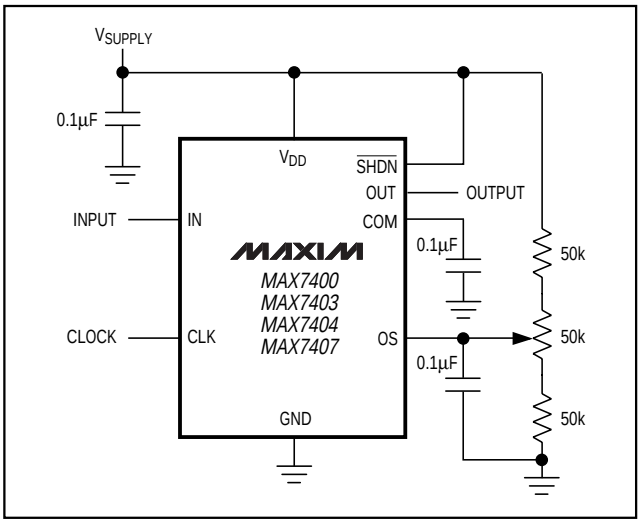


Figure 4. Offset Adjustment Circuit

Clock Signal

External Clock

The MAX7400/MAX7403/MAX7404/MAX7407 SCFs were designed for use with external clocks that have a 40% to 60% duty cycle. When using an external clock, drive CLK with a CMOS gate powered from 0 to V_{DD}. Varying the rate of the external clock adjusts the filter corner frequency:

$$f_C = f_{CLK} / 100$$

Internal Clock

When using the internal oscillator, the capacitance (C_{OSC}) on the CLK pin determines the oscillator frequency:

$$f_{OSC}(kHz) = \frac{K \cdot 10^3}{C_{OSC}};\ C_{OSC} \text{ in pF}$$

where K = 38 for the MAX7400/MAX7403, and K = 34 for the MAX7404/MAX7407. Since the capacitor value is in picofarads, minimize the stray capacitance at CLK so that it does not affect the internal oscillator frequency. Varying the rate of the internal oscillator adjusts the filter's corner frequency by a 100:1 clock-to-corner frequency ratio. For example, an internal oscillator frequency of 100kHz produces a nominal corner frequency of 1kHz.

Input Impedance vs. Clock Frequencies

The MAX7400/MAX7403/MAX7404/MAX7407's input impedance is effectively that of a switched-capacitor resistor and is inversely proportional to frequency. The input impedance determined by the following equation represents the average input impedance, since the input current is not continuous. As a rule, use a driver with an output source impedance less than 10% of the filter's input impedance. Estimate the input impedance of the filter using the following formula:

$$Z_{IN}(\Omega) = \frac{1}{(f_{CLK} \cdot C_{IN})}$$

where f_{CLK} = clock frequency and C_{IN} = 0.85pF.

Low-Power Shutdown Mode

These devices feature a shutdown mode that is activated by driving $\overline{SHDN}$ low. Placing the filter in shutdown mode reduces the supply current to 0.2µA (typ) and places the output of the filter into a high-impedance state. For normal operation, drive $\overline{SHDN}$ high or connect to V_{DD}.

Applications Information

Offset and Common-Mode Input Adjustment

The voltage at COM sets the common-mode input voltage and is internally biased at midsupply by a resistor-divider. Bypass COM with a 0.1µF capacitor and connect OS to COM. For applications requiring offset adjustment or DC level shifting, apply an external bias voltage through a resistor-divider network to OS, as shown in Figure 4. (Note: Do not leave OS unconnected.) The output voltage is represented by the following equation:

$$V_{OUT} = (V_{IN} - V_{COM}) + V_{OS}$$

with V_{COM} = V_{DD} / 2 (typical), and where (V_{IN} - V_{COM}) is lowpass filtered by the SCF, and V_{OS} is added at the output stage. See the *Electrical Characteristics* for COM and OS input voltage ranges. Changing the voltage on COM or OS significantly from midsupply reduces the filter's dynamic range.

Power Supplies

The MAX7400/MAX7403 operate from a single +5V supply. The MAX7404/MAX7407 operate from a single +3V supply. Bypass V_{DD} to GND with a 0.1µF capacitor. If dual supplies are required, connect COM to the system ground and GND to the negative supply. Figure 5 shows an example of dual-supply operation. Single-supply and dual-supply performance are equivalent. For single-supply or dual-supply operation, drive CLK and $\overline{SHDN}$ from GND (V- in dual-supply operation) to V_{DD}. For a ±2.5V supply, use the MAX7400 or MAX7403; for a ±1.5V supply, use MAX7404 or MAX7407. For ±5V dual-supply applications, use the MAX291–MAX297.

Input Signal Amplitude Range

The ideal input signal range is determined by observing the voltage level at which the total harmonic distortion plus noise (THD+N) is minimized for a given corner frequency. The *Typical Operating Characteristics* show THD+N response as the input signal's peak-to-peak amplitude is varied. These measurements are made with OS and COM biased at midsupply.

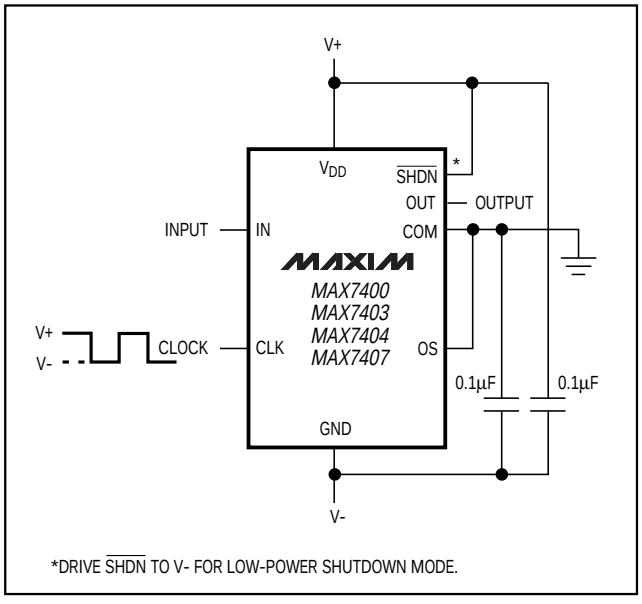


Figure 5. Dual-Supply Operation

Anti-Aliasing and Post-DAC Filtering

When using the MAX7400/MAX7403/MAX7404/MAX7407 for anti-aliasing or post-DAC filtering, synchronize the DAC and the filter clocks. If the clocks are not synchronized, beat frequencies may alias into the passband.

The high clock-to-corner frequency ratio (100:1) also eases the requirements of pre- and post-SCF filtering. At the input, a lowpass filter prevents the aliasing of frequencies around the clock frequency into the passband. At the output, a lowpass filter attenuates the clock feedthrough.

A high clock-to-corner frequency ratio allows a simple RC lowpass filter, with the cutoff frequency set above the SCF corner frequency, to provide input anti-aliasing and reasonable output clock attenuation.

Harmonic Distortion

Harmonic distortion arises from nonlinearities within the filter. Such nonlinearities generate harmonics when a pure sine wave is applied to the filter input. Table 1 lists typical harmonic distortion values with a 10kΩ load and an input signal of 4Vp-p (MAX7400/MAX7403) or 2Vp-p (MAX7404/MAX7407), at T_A = +25°C.

Table 1. Typical Harmonic Distortion

FILTER	f_{CLK} (kHz)	f_C (kHz)	f_{IN} (Hz)	V_{IN} (Vp-p)	TYPICAL HARMONIC DISTORTION (dB)			
					2nd	3rd	4th	5th
MAX7400	100	1	200	4	-89	-82	-89	-86
	500	5	1000		-89	-77	-93	-88
MAX7403	100	1	200	4	-88	-81	-91	-87
	500	5	1000		-84	-80	-90	-91
MAX7404	100	1	200	2	-85	-82	-85	-86
	500	5	1000		-85	-81	-86	-84
MAX7407	100	1	200	2	-85	-82	-85	-86
	500	5	1000		-86	-84	-85	-86

8th-Order, Lowpass, Elliptic, Switched-Capacitor Filters

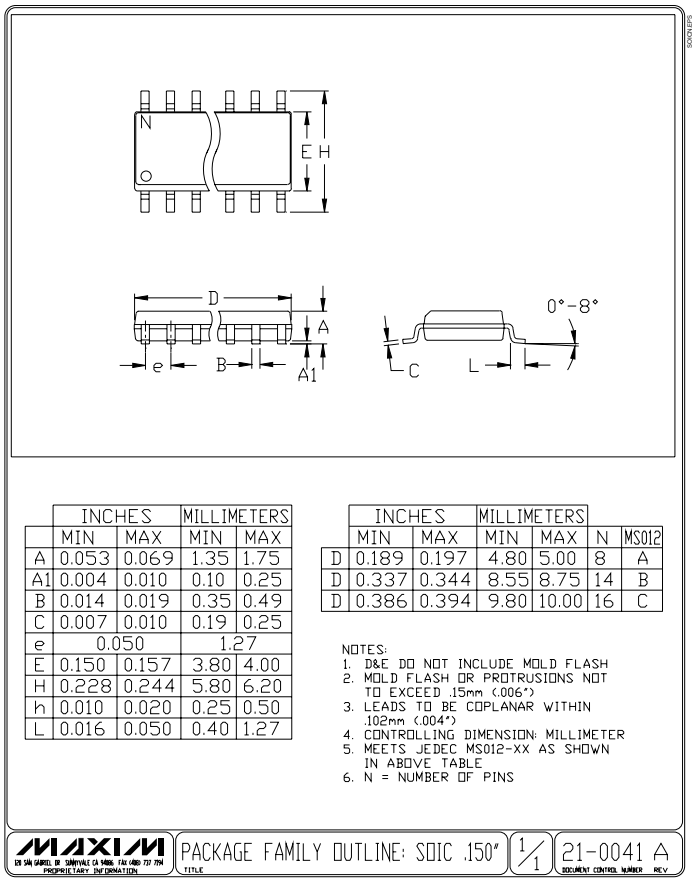
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX7403CSA	0°C to +70°C	8 SO
MAX7403CPA	0°C to +70°C	8 Plastic DIP
MAX7403ESA	-40°C to +85°C	8 SO
MAX7403EPA	-40°C to +85°C	8 Plastic DIP
MAX7404CSA	0°C to +70°C	8 SO
MAX7404CPA	0°C to +70°C	8 Plastic DIP
MAX7404ESA	-40°C to +85°C	8 SO
MAX7404EPA	-40°C to +85°C	8 Plastic DIP
MAX7407CSA	0°C to +70°C	8 SO
MAX7407CPA	0°C to +70°C	8 Plastic DIP
MAX7407ESA	-40°C to +85°C	8 SO
MAX7407EPA	-40°C to +85°C	8 Plastic DIP

Chip Information

TRANSISTOR COUNT: 1116

Package Information



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	A
D	0.337	0.344	8.55	8.75	14	B
D	0.386	0.394	9.80	10.00	16	C

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

MAXIM | PACKAGE FAMILY OUTLINE: SOIC .150" | 1/1 | 21-0041 A

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Maxim Integrated:

MAX7400CSA+ MAX7403CSA+ MAX7403ESA+T MAX7404CPA+ MAX7404CSA+ MAX7404CSA+T MAX7404EPA+ MAX7404ESA+ MAX7404ESA+T MAX7407CPA+ MAX7407CSA+ MAX7407CSA+T MAX7407EPA+ MAX7407ESA+ MAX7407ESA+T MAX7400ESA+ MAX7403ESA+ MAX7400CPA+ MAX7400CSA+T MAX7400EPA+ MAX7400ESA+T MAX7403CPA+ MAX7403CSA+T MAX7403EPA+