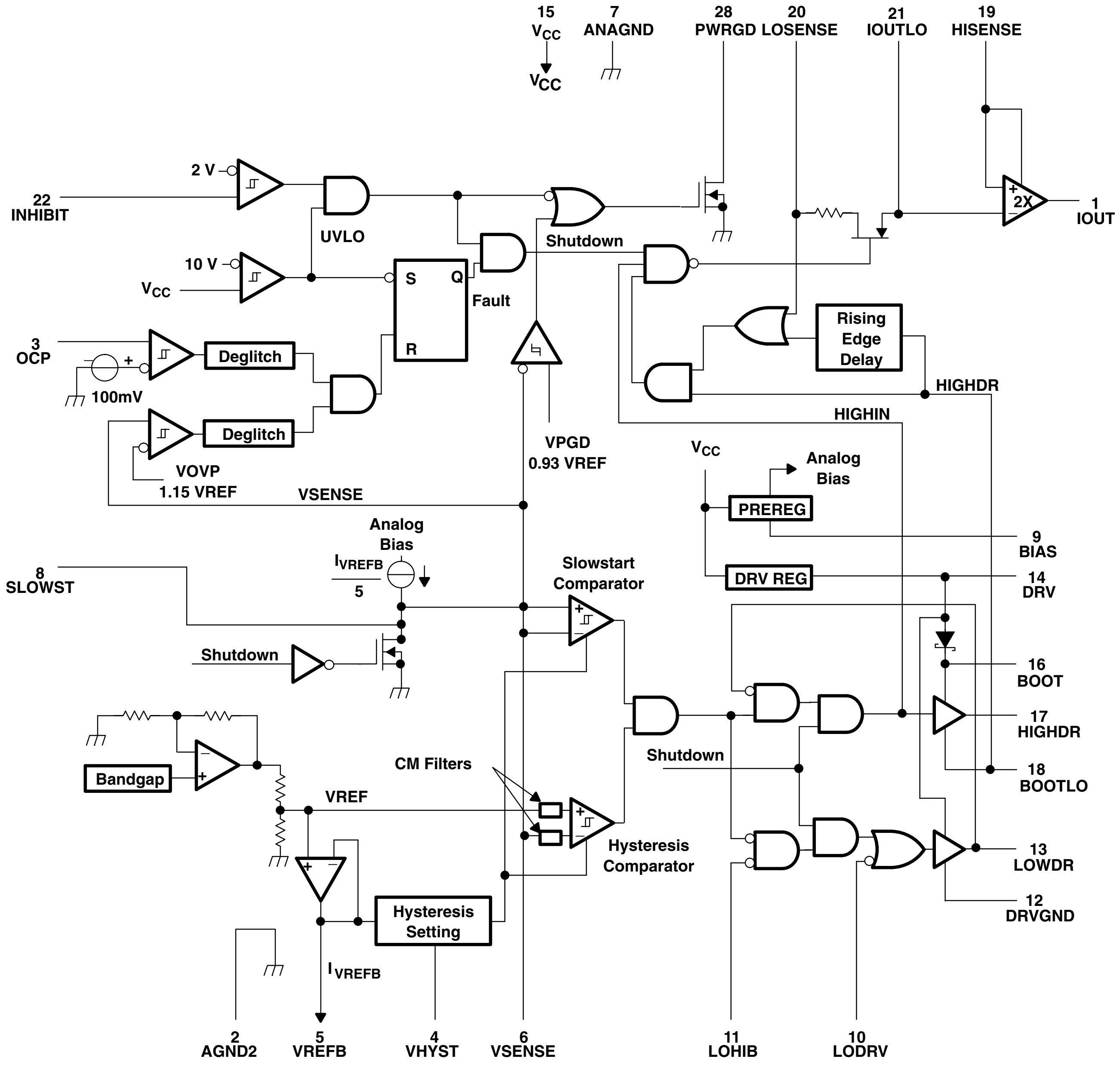
functional block diagram



Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AGND2	2		Analog ground (must be connected).
ANAGND	7		Analog ground
BIAS	9		Analog bias pin. A 1-µF capacitor should be connected from BIAS to ANAGND.
BOOT	16		Bootstrap. A 1-µF capacitor should be connected from BOOT to BOOTLO.
BOOTLO	18		Bootstrap low. Connect to the junction of the high-side and low-side FETs for floating drive configuration. Connect to PGND for ground-reference drive configuration.
DRV	14		Drive regulator for the FET drivers. A 1-µF capacitor should be connected from DRV to DRVGND.
DRVGND	12		Drive ground. Ground for FET drivers. Connect to FET PWRGND.
HIGHDR	17		High drive. Output drive to high-side power switching FETs.
HISENSE	19		High current sense. For current sensing across high-side FETs, connect to the drain of the high-side FETs; for optional current sensing scheme, connect to power supply side of current-sense resistor placed in series with high-side FET drain.
INHIBIT	22		Disables the drive signals to the MOSFET drivers. Also serves as UVLO for system logic supply (3.3 V or 5 V). An external pullup resistor should be connected to system-logic supply.
IOUT	1		Current out. Output voltage on this terminal is proportional to the load current as measured across the $R_{ds(on)}$ of the high side FET. The voltage on this terminal equals $2 \times R_{DS(ON)} \times$ IOUT. In applications where very accurate current-sensing is required, a sense resistor should be connected between the input supply and the drain of the high-side FETs.
IOUTLO	21		Current sense low output. This is the voltage on the LOSENSE terminal when the high-side FETs are on. A ceramic capacitor (between 0.033 µF and 0.1 µF) should be connected from IOUTLO to HISENSE to hold the sensed voltage.
LODRV	10		Low drive enable. Normally tied to 5 V. To configure the low-side FET as a crowbar, pull LODRV low.
LOHIB	11		Low side inhibit. Connect to the junction of the high- and low-side FETs to control the anti-cross-conduction and eliminate shoot-through current. Disabled when configured in crowbar mode.
LOSENSE	20		Low current sense. For current sensing across high-side FETs, connect to the source of the high-side FETs; for optional current sensing scheme, connect to high-side FET drain side of current-sense resistor placed in series with high-side FET drain.
LOWDR	13		Low drive. Output drive to synchronous rectifier FETs.
NC	23–27		No connect
OCP	3		Over current protection. Current limit trip point is set with a resistor divider between IOUT and ANAGND.
PWRGD	28		Power good. PWRGD signal goes high when output voltage is within 7% of voltage setpoint. Open-drain output.
SLOWST	8		Slow Start (soft start). A capacitor form SLOWST to ANAGND sets the slowstart time. Slowstart current = $I_{VREFB}/5$
VHYST	4		Hysteresis set input. The hysteresis is set with a resistor divider from VREFB to ANAGND. Hysteresis = 2 × (VREFB – VHYST)
V_{CC}	15		12-V supply. A 1-µF capacitor should be connected from V_{CC} to DRVGND.
VREFB	5		Buffered reference voltage
VSENSE	6		Voltage sense Input. To be connected from converter output voltage bus to sense and control output voltage. It is recommended that a RC low-pass filter be connected at this pin to filter noise.

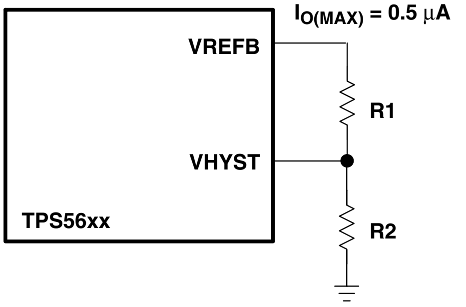
detailed description

Vref

The reference voltage section consists of a temperature-compensated bandgap reference and a resistive divider that sets the output voltage option. The output voltage, VREF, is within 1% of the nominal setting over the full junction temperature range of 0°C to 125°C, and a V_{CC} supply voltage range of 11.4 V to 12.6 V. The output of the reference network is indirectly brought out through a buffer to the VREFB pin. The voltage on this pin will be within 2% of VREF. It is not recommended to drive loads with VREFB, other than setting the hysteresis of the hysteretic comparator, because the current drawn from VREFB sets the charging current for the slowstart capacitor. Refer to the *slowstart* section for additional information.

hysteretic comparator

The hysteretic comparator regulates the output voltage of the synchronous-buck converter. The hysteresis is set by 2 external resistors and is centered on VREF. The 2 external resistors form a resistor divider from VREFB to ANAGND, with the output voltage connecting to the VHYST pin. The hysteresis of the propagation delay from the comparator inputs to the driver outputs is 250 ns (maximum). The maximum hysteresis setting is 60 mV.



$$R1 = \frac{R2 \times V_H}{2 \times VREFB - V_H}$$

Where

V_H = desired hysteresis voltage

$$= 2 \times \left(VREFB - V_H\right)$$

Figure 1. Setting the Hysteresis Voltage

low-side driver

The low-side driver is designed to drive low-$R_{ds(on)}$ n-channel MOSFETs. The current rating of the driver is 2 A, source or sink. The bias to the low-side driver is internally connected to the DRV regulator.

high-side driver

The high-side driver is designed to drive low-$R_{ds(on)}$ n-channel MOSFETs. The current rating of the driver is 2 A, source or sink. The high-side driver can be configured either as a ground-referenced driver or as a floating bootstrap driver. When configured as a floating driver, the bias voltage to the driver is developed from the DRV regulator. The internal bootstrap diode, connected between the DRV and BOOT pins, is a Schottky for improved drive efficiency. The maximum voltage that can be applied between BOOT and DRVGND is 30 V. The driver can be referenced to ground by connecting BOOTLO to DRVGND, and connecting BOOT to either DRV or V_{CC}.

deadtime control

Deadtime control prevents shoot-through current from flowing through the main power FETs during switching transitions by actively controlling the turn-on times of the MOSFET drivers. The high-side driver is not allowed to turn on until the gate-drive voltage to the low-side FET is below 2 V; the low-side driver is not allowed to turn on until the voltage at the junction of the 2 FETs (Vphase) is below 2 V.

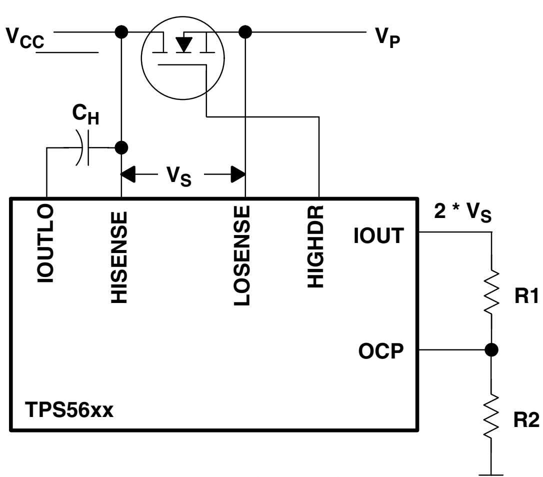
detailed description (continued)

current sensing

Current sensing is achieved by sampling and holding the voltage across the high-side power FET while the high-side FET is on. The sampling network consists of an internal 60-Ω switch and an external ceramic hold capacitor. Recommended value of the hold capacitor is between 0.033 µF and 0.1 µF. The actual value should give a time constant ($60\ \Omega \times C_H$) greater than the FET on time. Internal logic controls the turn-on and turn-off of the sample/hold switch such that the switch does not turn on until the Vphase voltage transitions high, and the switch turns off when the input to the high-side driver goes low. Thus sampling will occur only when the high side FET is conducting current. The voltage on the IOUT pin equals 2 times the sensed high-side voltage. In applications where a higher accuracy in current-sensing is required, a sense resistor can be placed in series with the high-side FET and the voltage across the sense resistor can be sampled by the current sensing circuit. See Figures 2 and 3.

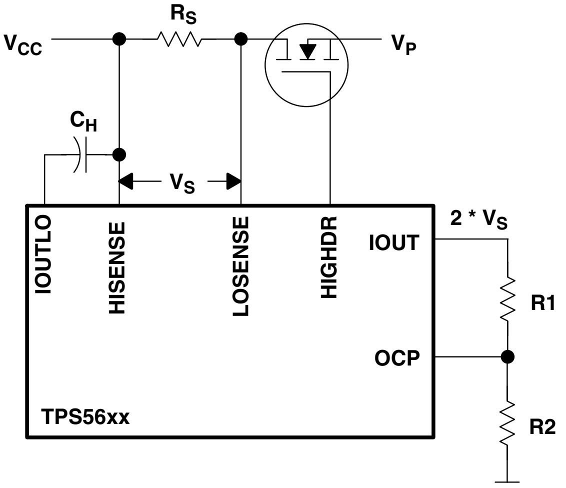
overcurrent protection

The overcurrent protection (OCP) circuit monitors the current through the high-side FET. The overcurrent threshold is adjustable with an external resistor divider between IOUT and ANAGND, with the divider voltage connected to OCP. If the voltage on OCP (V_S) exceeds 100 mV, then a fault latch is set and the output drivers are turned off. The latch will remain set until V_{CC} goes below the undervoltage lockout value. A 3-µs deglitch timer is included for noise immunity. The OCP circuit is also designed to protect the high-side power FET against a short-to-ground fault on the terminal common to both power FETs (Vphase).



$$R1 = \frac{R2 \times \left(V_S - 0.05\right)}{0.05}$$

Figure 2. OCP Using FET ON-Resistance



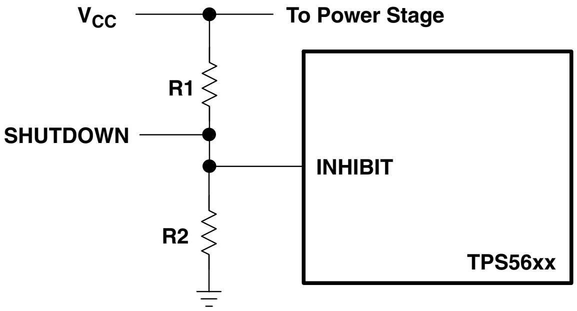
$$R1 = \frac{R2 \times \left(V_S - 0.05\right)}{0.05}$$

Figure 3. Precision OCP Using External Resistor

inhibit

INHIBIT is a TTL-compatible digital input used to enable the controller. When INHIBIT is low, the output drivers are low and the slowstart capacitor is discharged. When INHIBIT goes high, the short across the slowstart capacitor is released and normal converter operation begins. When the system-logic supply is connected to INHIBIT, it also controls power sequencing by locking out controller operation until the system-logic supply exceeds the input threshold voltage of the inhibit circuit. Thus the 12-V supply and the system-logic supply (either 5 V or 3.3 V) must be above UVLO thresholds before the controller is allowed to start up. The INHIBIT comparator start threshold is 2.1 V and the hysteresis is 100 mV.

detailed description (continued)



$$R2 = \frac{2.1 \times R1}{V_{TRIP} - 2.1}$$

Where

V_{TRIP}=desired V_{SUPPLY} trip voltage

Figure 4. Input Undervoltage Lockout Circuit Using INHIBIT

V_{CC} undervoltage lockout (UVLO)

The undervoltage lockout circuit disables the controller while the V_{CC} supply is below the 10-V start threshold during power up. While the controller is disabled, the output drivers will be low and the slowstart capacitor will be shorted. When V_{CC} exceeds the start threshold, the short across the slowstart capacitor is released and normal converter operation begins. There is a 2-V hysteresis in the undervoltage lockout circuit for noise immunity.

slowstart

The slowstart circuit controls the rate at which V_O powers up. A capacitor is connected between SLOWSST and ANAGND and is charged by an internal current source. The slowstart charging current is determined by the following equation:

$$I_{SLOWSTART} = \frac{I(VREFB)}{5}$$

where I(VREFB) is the current flowing out of VREFB. It is recommended that no additional loads be connected to VREFB, other than the resistor divider for setting the hysteresis voltage. The maximum current that can be sourced by the VREFB circuit is 500 µA. The slowstart time is set by:

$$t_{SLOWSTART} = 5 \times C_{SLOWST} \times R_{VREFB}$$

where R_{VREFB} is the total external resistance from VREFB to ANAGND.

power good

The power good circuit monitors for an undervoltage condition on V_O. If V_O is 7% below V_{REF}, then PWRGD is pulled low. PWRGD is an open-drain output.

overvoltage protection

The overvoltage protection (OVP) circuit monitors V_O for an overvoltage condition. If V_O is 15% above V_{REF}, then a fault latch is set and both output drivers are turned off. The latch will remain set until V_{CC} goes below the undervoltage lockout value. A 3-µs deglitch timer is included for noise immunity. Refer to the LODRV section for information on how to protect the load against overvoltages due to a shorted fault across the high-side power FET.

detailed description (continued)

drive regulator

The drive regulator provides drive voltage to the output drivers. The minimum drive voltage is 7 V. The minimum short circuit current is 100 mA. Connect a 1-µF ceramic capacitor from DRV to DRVGND.

LODRV

The LODRV circuit is designed to protect the load against overvoltages that occur if the high-side FETs become shorted. External components to sense an overvoltage condition are required to use this feature. When an overvoltage fault occurs, LODRV is pulled low and the low-side FET will be turned on, overriding all control signals inside the TPS56xx controller. The crowbar action will short the system-logic supply to ground through the faulted high-side FETs and the low-side FETs. A fuse, in series with V_{IN}, should be added to disconnect the short circuit.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)		–0.3 to 14 V
Input voltage range:	BOOT to DRVGND (high-side driver ON)	–0.3 to 30 V
	BOOT to HIGHDRV	–0.3 to 15 V
	BOOT to BOOTLO	–0.3 to 15 V
	INHIBIT, LODRV	–0.3 to 7.3 V
	PWRGD, OCP	–0.3 to 7 V
	LOHIB, LOSENSE, IOUTLO, HISENSE	–0.3 to 14 V
	VSENSE	–0.3 to 5 V
Voltage difference between ANAGND and DRVGND		±0.5 V
Output current, VREFB		0.5 mA
Short circuit duration, DRV		Continuous
Continuous total power dissipation		See Dissipation Rating Table
Operating junction temperature range, T_J		0°C to 125°C
Storage temperature range, T_{stg}		–65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds		260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Unless otherwise specified, all voltages are with respect to ANAGND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
PWP	1150 mW	11.5 mW/°C	630 mW	460 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}		11.4	13	V
Input voltage	BOOT to DRVGND	0	28	V
	BOOT to BOOTLO	0	13	
	INHIBIT, LODRV, PWRGD, OCP	0	6	
	LOHIB, LOSENSE, IOUTLO, HISENSE	0	13	
	VSENSE	0	4.5	
Voltage difference between ANAGND and DRVGND		0	±0.2	V
Output current, VREFB[†]		0	0.4	mA

[†] Not recommended to load VREFB other than to set hysteresis since I_{VREFB} sets slowstart time.

electrical characteristics over recommended operating virtual junction temperature range, V_{CC} = 12 V, I_{DRV} = 0 A (unless otherwise noted)

reference

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
VREF	Reference voltage	TPS5615	V_{CC} = 11.4 V to 12.6 V	1.485		1.515	V
		TPS5618		1.782		1.818	
		TPS5625		2.475		2.525	
		TPS5633		3.267		3.333	
VREFB	Output voltage		I_{REFB} = 50 µA	VREF−2%	VREF	VREF+2%	V
VREFB	Output regulation		10 µA ≤ I_O ≤ 500 µA		2		mV

power good

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Undervoltage trip threshold		90	93	95	%VREF
Low-level output voltage, PWRGD	I_O = 5 mA		0.5	0.75	V
High-level input current, PWRGD	V_{PWRGD} = 6 V		1		µA
Hysteresis			10		mV

overvoltage protection

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Overvoltage trip threshold		112	115	120	%VREF
Hysteresis	See Note 2		10		mV

NOTE 2: Ensured by design, not tested.

slowstart

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Charge current	V_{SLOWST} = 0.5 V, I_{VREFB} = 65 µA	10.4	13	15.6	µA
Discharge current	V_{SOFTST} = 1 V		3		mA
Comparator input offset voltage				10	mV
Comparator input bias current	See Note 2		10	100	nA
Hysteresis		−7.5		7.5	mV

NOTE 2: Ensured by design, not tested.

electrical characteristics over recommended operating virtual junction temperature range, V_{CC} = 12 V, I_{DRV} = 0 A (unless otherwise noted) (continued)

inhibit

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Startup threshold		1.9	2.1	2.35	V
Hysteresis		0.08	0.1	0.12	V
Stop threshold		1.85			V

input undervoltage lockout

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Startup threshold		9.25	10	10.75	V
Hysteresis		1.9	2	2.2	V
Stop threshold		7.5			V

hysteretic comparator

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input offset voltage		–2.5		2.5	mV
Input bias current	See Note 2			500	nA
Hysteresis accuracy	$V_{REFB} - V_{HYST}$ = 15 mV, (hysteresis window = 30 mV)	–3.5		3.5	mV
Maximum hysteresis setting	$V_{REFB} - V_{HYST}$ = 30 mV		60		mV

NOTE 2: Ensured by design, not tested.

overcurrent protection

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OCP trip threshold		90	100	110	mV
Input bias current				100	nA

electrical characteristics over recommended operating virtual junction temperature range, V_{CC} = 12 V, I_{DRV} = 0 A (unless otherwise noted) (continued)

high-side VDS sensing

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Gain				2		V/V
Initial accuracy	$V_{HISENSE}$ = 12 V, $V_{LOSENSE}$ = 11.9 V Differential input to Vds sensing amp = 100 mV		194		206	mV
IOUTLO sink current	5 V ≤ V_{IOUTLO} ≤ 13 V				250	nA
IOUT source current	V_{IOUT} = 0.5 V, $V_{HISENSE}$ = 12 V, V_{IOUTLO} = 11.5 V		500			µA
IOUT sink current	V_{IOUT} = 0.05 V, $V_{HISENSE}$ = 12 V, V_{IOUTLO} = 12 V		50			µA
Output voltage swing	$V_{HISENSE}$ = 11 V	R_{IOUT} = 10 kΩ	0		2	V
	$V_{HISENSE}$ = 4.5 V		0		1.5	
	$V_{HISENSE}$ = 3 V		0		0.75	
LOSENSE high-level input voltage	$V_{HISENSE}$ = 4.5 V, See Note 2		2.85			V
LOSENSE low-level input voltage	$V_{HISENSE}$ = 4.5 V, See Note 2				2.4	V
Sample/hold resistance	11.4 V ≤ $V_{HISENSE}$ ≤ 12.6 V, LOSENSE connected to HISENSE, $V_{HISENSE} - V_{IOUTLO}$ = 0.15 V		50	60	80	Ω
	4.5 V ≤ $V_{HISENSE}$ ≤ 5.5 V, LOSENSE connected to HISENSE, $V_{HISENSE} - V_{IOUTLO}$ = 0.15 V		62	85	123	
	3 V ≤ $V_{HISENSE}$ ≤ 3.6 V, LOSENSE connected to HISENSE, $V_{HISENSE} - V_{IOUTLO}$ = 0.15 V		67	95	144	
CMRR	$V_{HISENSE}$ = 12.6 V to 3 V, $V_{HISENSE} - V_{OUTLO}$ = 100 mV		69	75		dB

NOTE 2: Ensured by design, not tested.

deadtime

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOHIB	High-level input voltage	See Note 2	2.4			V
LODR		See Note 2	3			
LOHIB	Low-level input voltage	See Note 2			1.4	V
LODR		See Note 2			1.7	

NOTE 2: Ensured by design, not tested.

LODRV

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LODRV	High-level input voltage		1.85			V
	Low-level input voltage				0.95	V

drive regulator

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage	11.4 V ≤ VCC ≤ 12.6 V, I_{DRV} = 50 mA	7		9	V
Output regulation	1 mA ≤ I_{DRV} ≤ 500 mA		100		mV
Short-circuit current		100			mA

electrical characteristics over recommended operating virtual junction temperature range, V_{CC} = 12 V, I_{DRV} = 0 A (unless otherwise noted) (continued)

bias regulator

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage	11.4 V ≤ VCC ≤ 12.6 V, See Note 3	6			V

NOTE 3: The bias regulator is designed to provide a quiet bias supply for the TPS56xx controller. External loads should not be driven by the bias regulator.

output drivers

PARAMETER (see Note 4)		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Peak output current	High-side sink	Duty cycle < 2%, t_{pw} < 100 µs, T_J = 125°C, $V_{BOOT} - V_{BOOTLO}$ = 6.5 V, V_{HIGHDR} = 1.5 V (SRC) or 5 V (sink), See Note 2	2			A
	High-side source		2			
	Low-side sink	Duty cycle < 2%, t_{pw} < 100 µs, T_J = 125°C, V_{DRV} = 6.5 V, V_{LOWDR} = 1.5 V (SRC) or 5 V (sink), See Note 2	2			
	Low-side source		2			
Output resistance	High-side sink	T_J = 125°C, $V_{BOOT} - V_{BOOTLO}$ = 6.5 V, V_{HIGHDR} = 1.5 V (SRC) or 5 V (sink)			3	Ω
	High-side source				45	
	Low-side sink	T_J = 125°C, V_{DRV} = 6.5 V, V_{LOWDR} = 1.5 V (SRC) or 5 V (sink)			5.7	
	Low-side source				45	

NOTES: 2. Ensured by design, not tested.

4. The pull up/down circuits of the drivers are bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors. The output resistance is the $R_{DS(ON)}$ of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor.

supply current

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC} supply voltage range		11.4	12	13	V
V_{CC} quiescent current	$V_{INHIBIT}$ = 5 V, V_{CC} > 10.75 V at startup, V_{BOOTLO} = 0 V, See Note 2		3	10	mA
	$V_{INHIBIT}$ = 5 V, V_{CC} > 10.75 V at startup, V_{BOOTLO} = 0 V, C_{HIGHDR} = 50 pF, C_{LOWDR} = 50 pF, f_{swx} = 200 kHz		5		
High-side drive regulator quiescent current	$V_{INHIBIT}$ = 0 V or V_{CC} < 9.25 V at startup, V_{BOOT} = 13 V, V_{BOOTLO} = 0 V			80	µA
	$V_{INHIBIT}$ = 5 V, V_{CC} > 10.75 V at startup, V_{BOOT} = 13 V, V_{BOOTLO} = 0 V, C_{HIGHDR} = 50 pF, f_{swx} = 200 kHz		2		mA

NOTE 2: Ensured by design, not tested.

switching characteristics over recommended operating virtual junction temperature range, V_{CC} = 12 V, I_{DRV} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay	VSENSE to HIGHDR or LOWDR (excluding deadtime)	Overdrive = 10 mV (see Note 2)		150	250	ns
	OCP comparator	See Note 2		1		µs
	OVP comparator	See Note 2		1		
	PWRGD comparator	See Note 2		1		
	SLOWST comparator	Overdrive = 10 mV (see Note 2)		560	900	ns
Rise time	HIGHDR output	C_L = 9 nF, V_{BOOT} = 6.5 V, V_{BOOTLO} = 0 V, T_J = 125°C			60	ns
	LOWDR output	C_L = 9 nF, V_{DRV} = 6.5 V, T_J = 125°C			60	
Fall time	HIGHDR output	C_L = 9 nF, V_{BOOT} = 6.5 V, V_{BOOTLO} = 0 V, T_J = 125°C			60	ns
	LOWDR output	C_L = 9 nF, V_{DRV} = 6.5 V, T_J = 125°C			60	
Deglitch time (includes comparator propagation delay)	OCP	See Note 2	2		5	µs
	OVP	See Note 2	2		5	
Response time	High-side VDS sensing	$V_{HISENSE}$ = 12 V, V_{IOUTLO} pulsed from 12 V to 11.9 V, 100 ns rise/fall times, See Note 2			2	µs
		$V_{HISENSE}$ = 4.5 V, V_{IOUTLO} pulsed from 4.5 V to 4.4 V, 100 ns rise/fall times, See Note 2			3	
		$V_{HISENSE}$ = 3 V, V_{IOUTLO} pulsed from 3 V to 2.9 V, 100 ns rise/fall times, See Note 2			3	
Short-circuit protection rising-edge delay	SCP	LOSENSE = 0 V, (see Note 2)	300		500	ns
Turn-on/turn-off delay	V_{DS} sensing sample/hold switch	3 V ≤ $V_{HISENSE}$ ≤ 11 V, $V_{LOSENSE}$ = $V_{HISENSE}$ (see Note 2)	30		100	ns
Crossover delay time	LOWDR to HIGHDRV, and LOHIB to LOWDR	See Note 2	30		100	ns
Prefilter pole frequency	Hysteretic comparator	See Note 2		5		MHz
Propagation delay	LODRV	See Note 2			400	ns

NOTE 2: Ensured by design, not tested.

TYPICAL CHARACTERISTICS

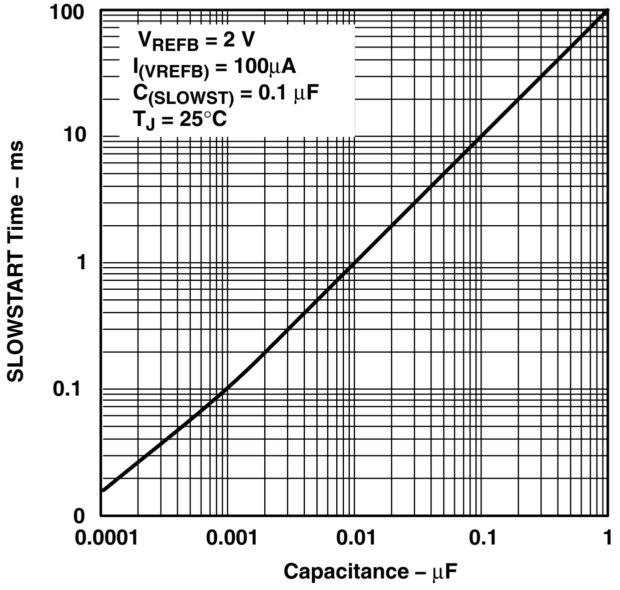

SLOWSTART TIMING
vs
CAPACITANCE

Figure 5

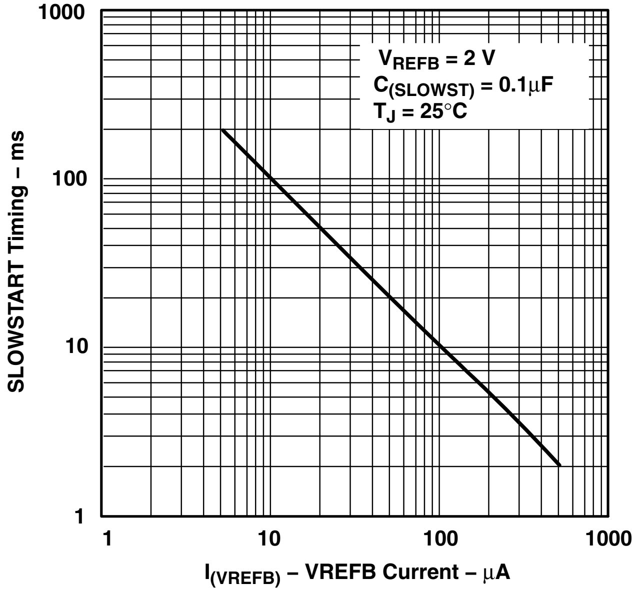

SLOWSTART TIMING
vs
VREFB CURRENT

Figure 6

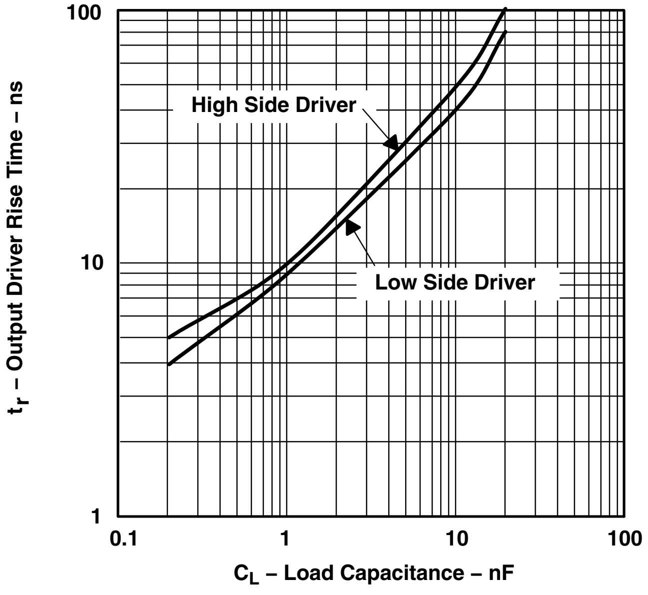

OUTPUT DRIVER RISE TIME
vs
LOAD CAPACITANCE

Figure 7

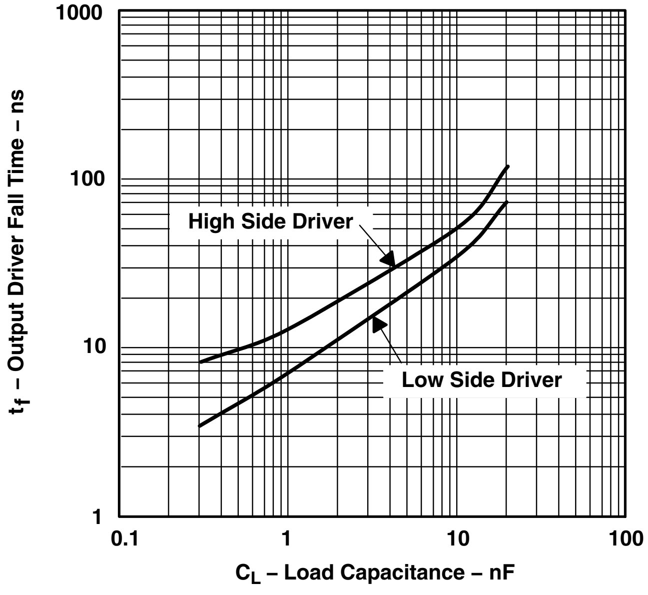

OUTPUT DRIVER FALL TIME
vs
LOAD CAPACITANCE

Figure 8

TYPICAL CHARACTERISTICS

OVP THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

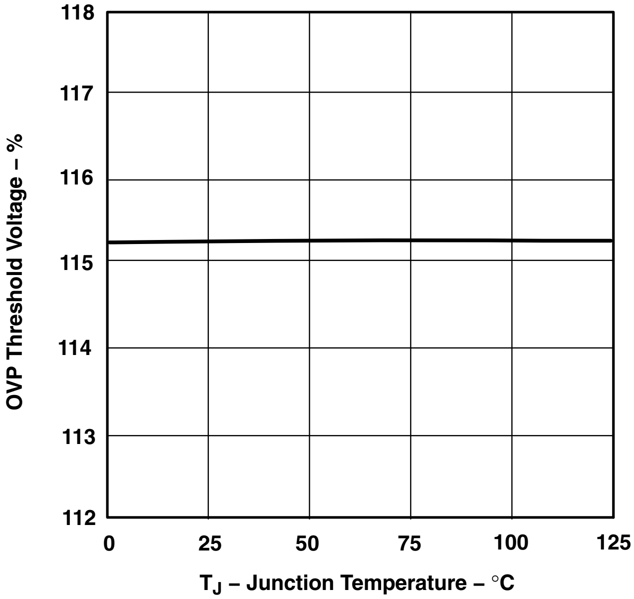


Figure 9

OCP THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

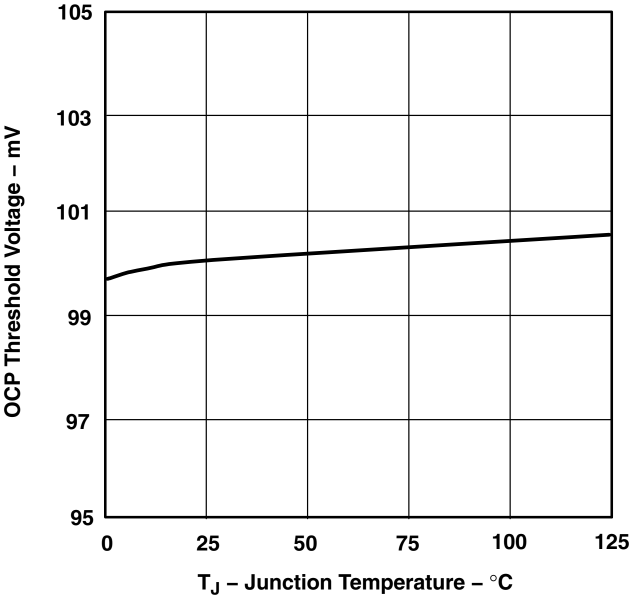


Figure 10

INHIBIT START THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

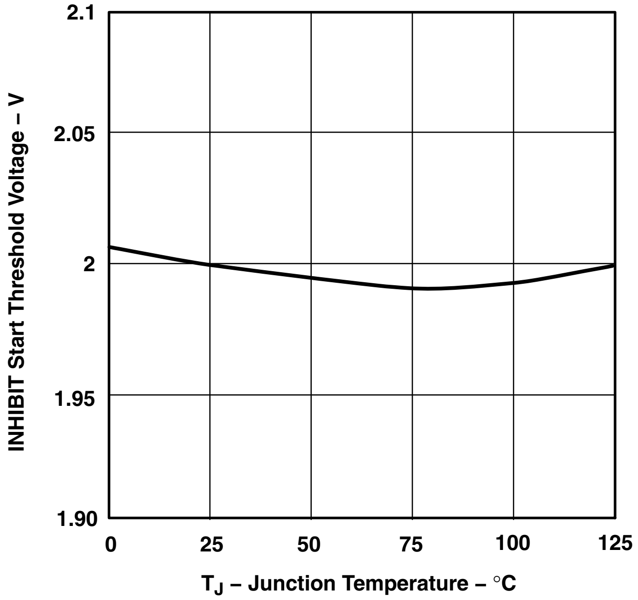


Figure 11

INHIBIT HYSTERESIS VOLTAGE
vs
JUNCTION TEMPERATURE

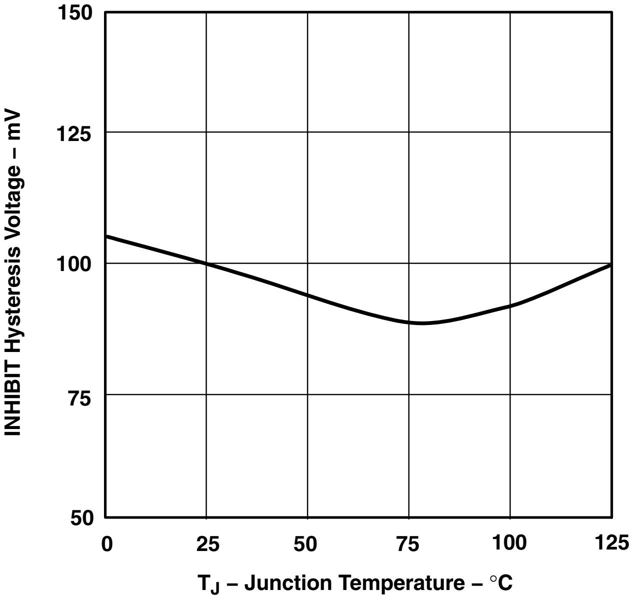


Figure 12

TYPICAL CHARACTERISTICS

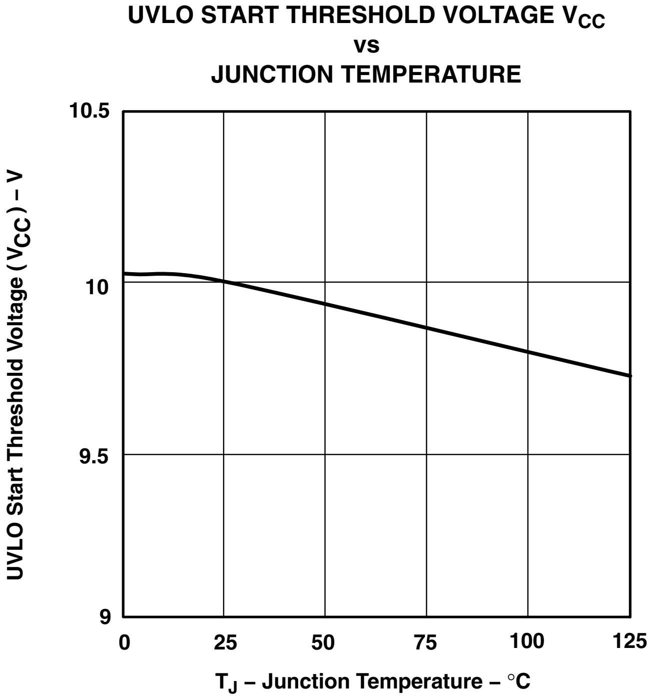


Figure 13

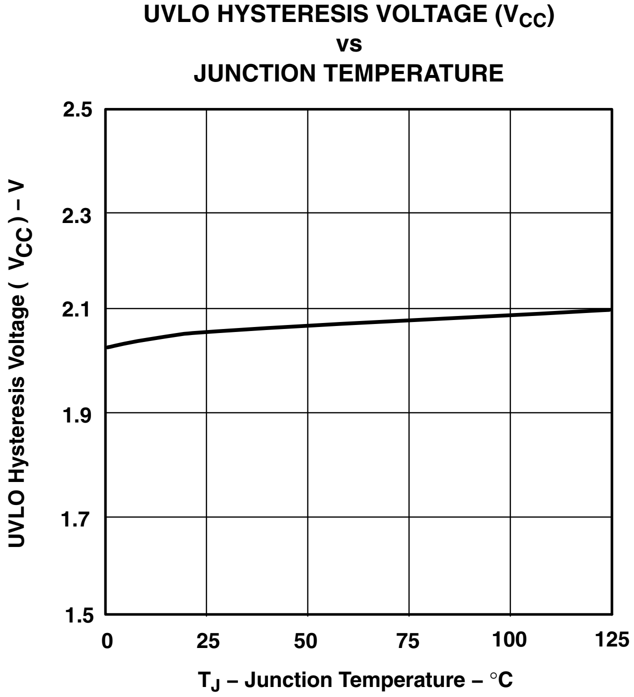


Figure 14

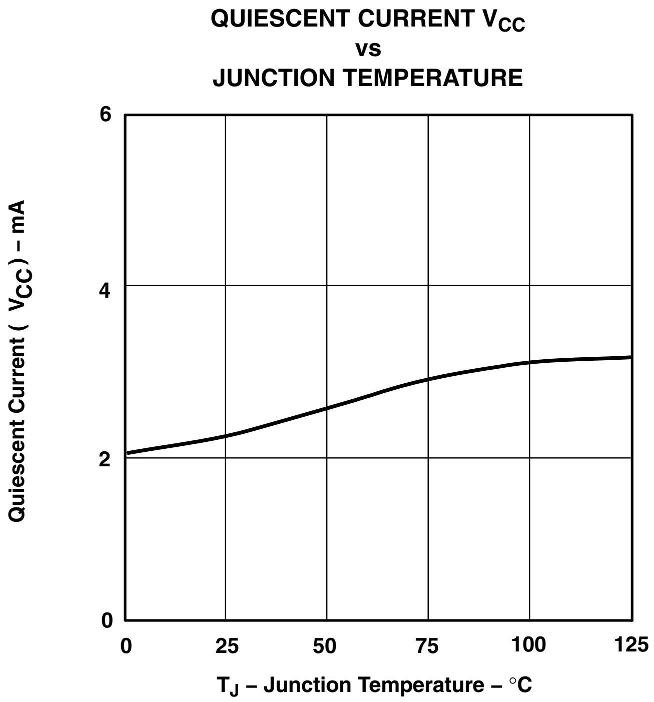


Figure 15

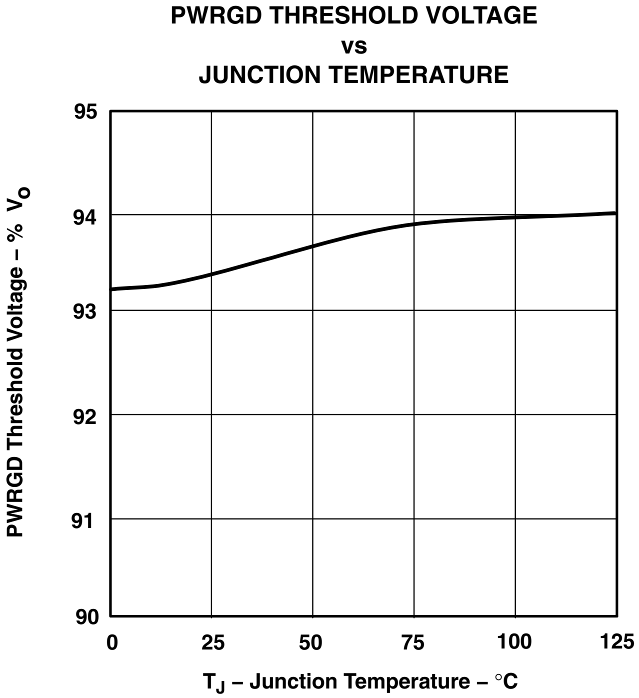


Figure 16

TYPICAL CHARACTERISTICS

SLOWSTART CHARGE CURRENT
vs
JUNCTION TEMPERATURE

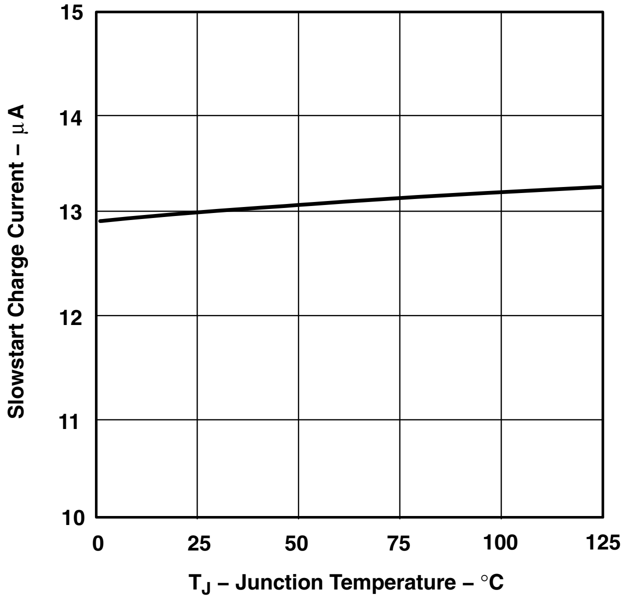


Figure 17

VDS SAMPLE/HOLD RESISTANCE
vs
JUNCTION TEMPERATURE

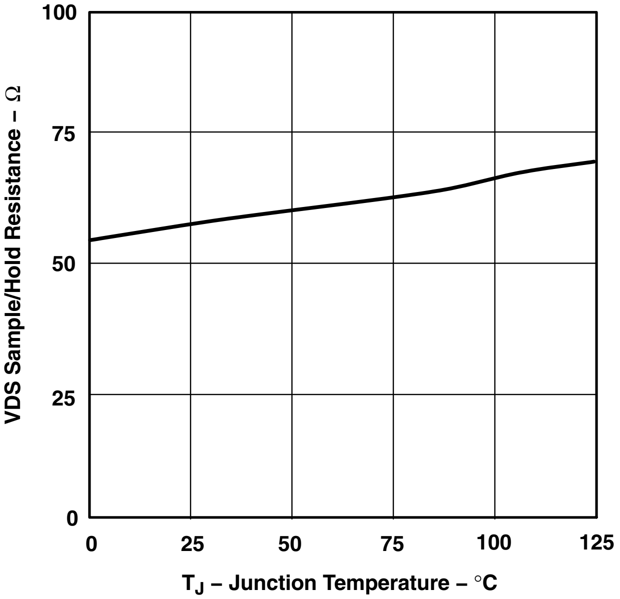


Figure 18

DRIVE REGULATOR OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE

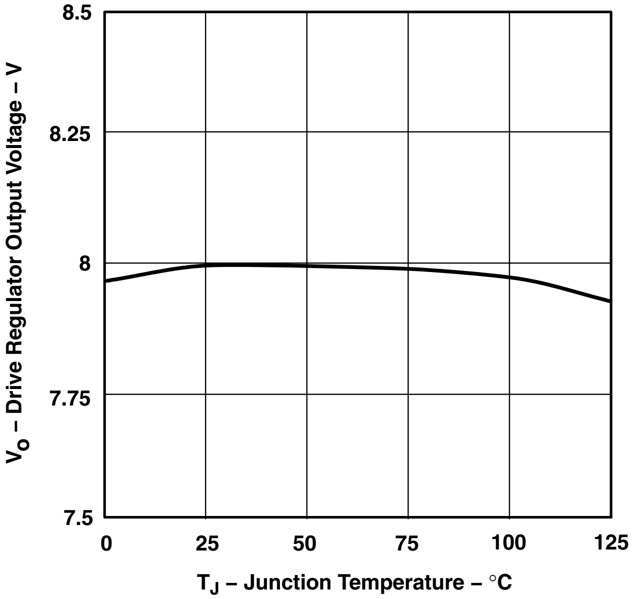


Figure 19

DRIVE REGULATOR LOAD REGULATION
vs
JUNCTION TEMPERATURE

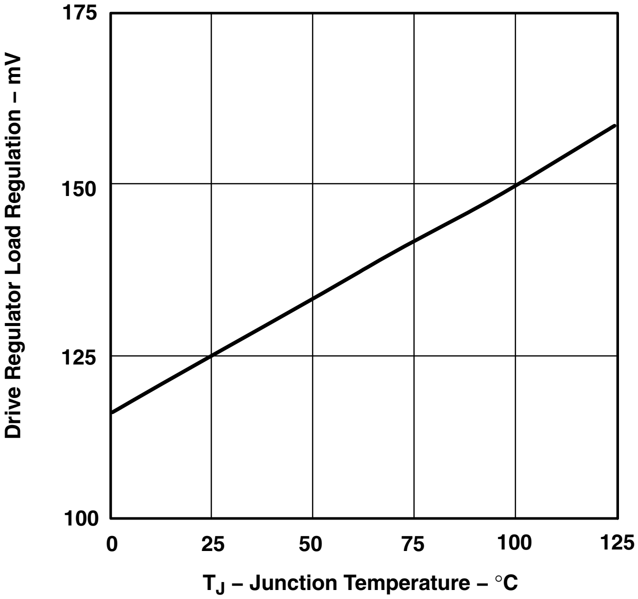


Figure 20

TYPICAL CHARACTERISTICS

DRIVE REGULATOR LINE REGULATION
vs
JUNCTION TEMPERATURE

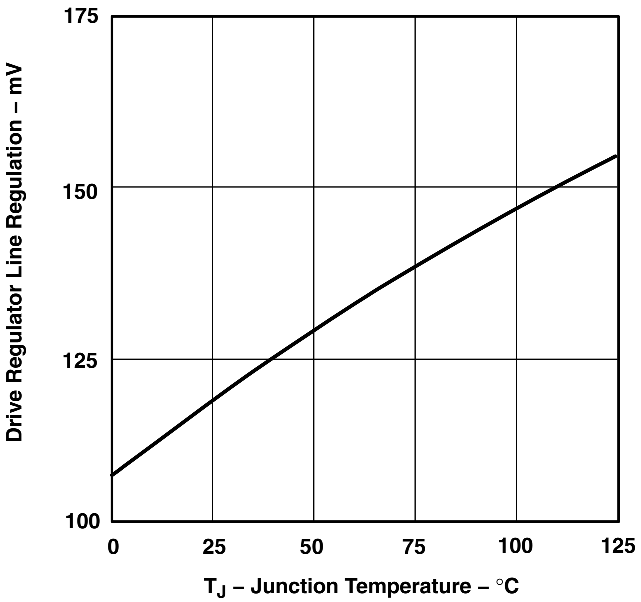


Figure 21

HIGH−SIDE DRIVER OUTPUT RESISTANCE
vs
JUNCTION TEMPERATURE

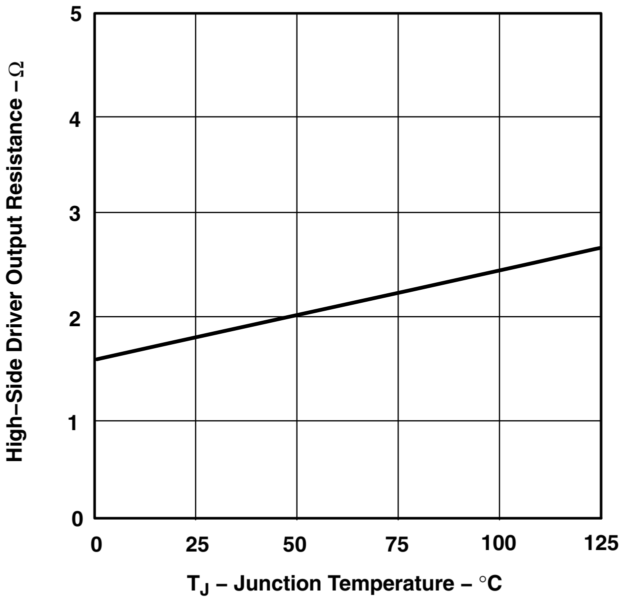


Figure 22

LOW−SIDE DRIVER OUTPUT RESISTANCE
vs
JUNCTION TEMPERATURE

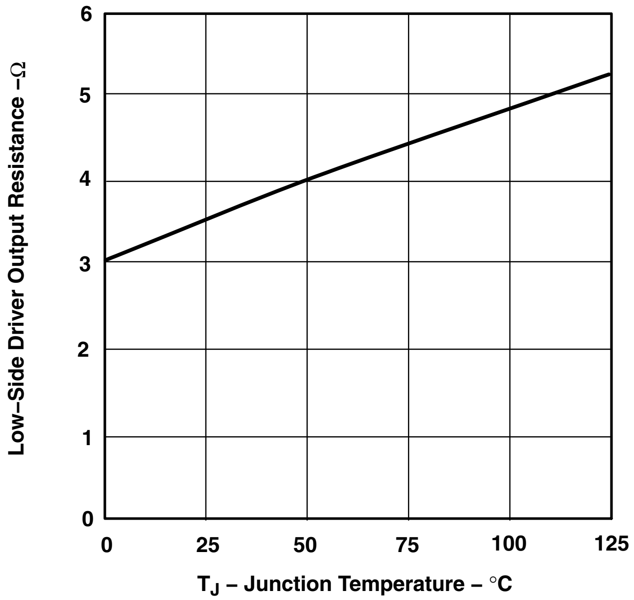


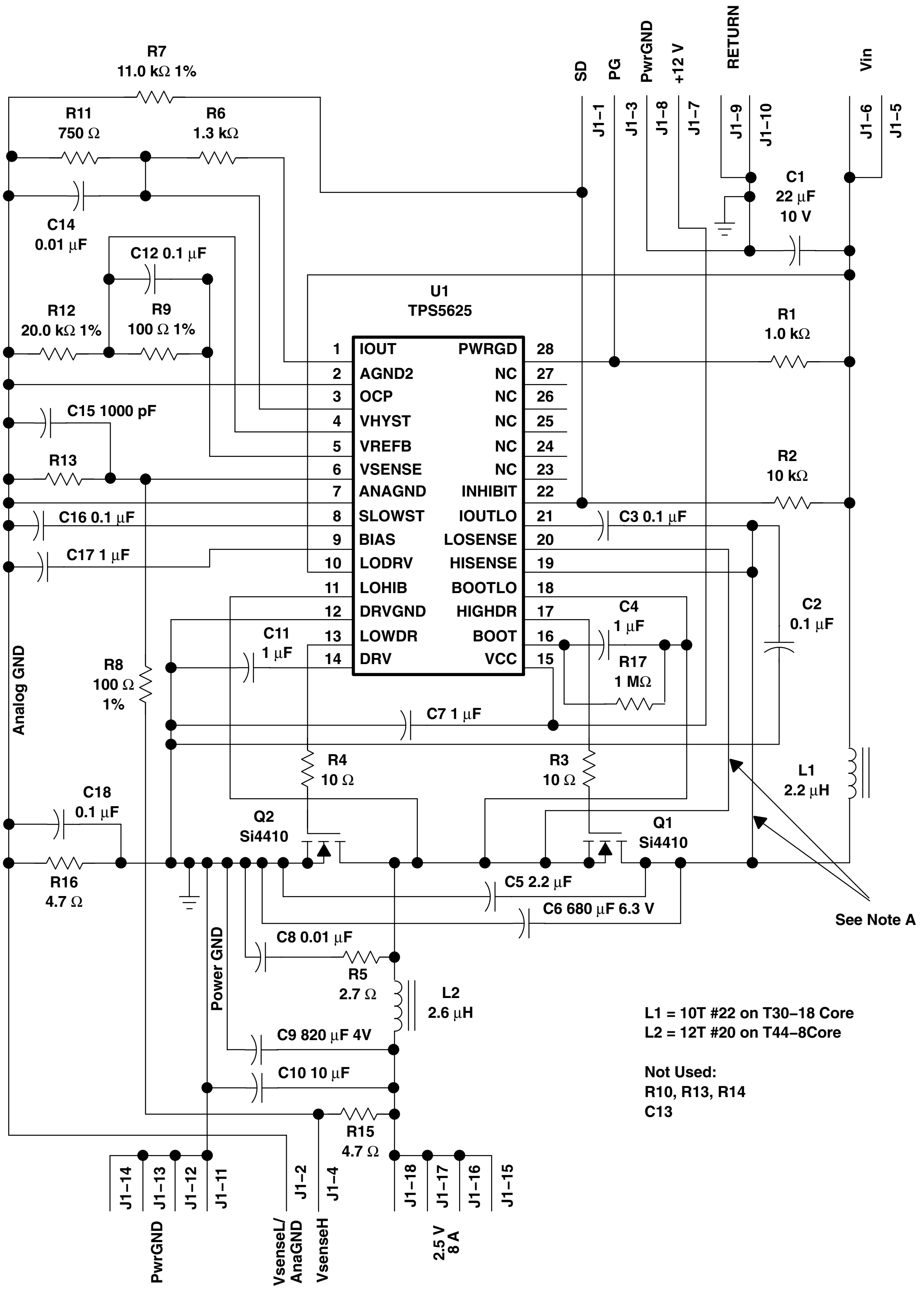
Figure 23

APPLICATION INFORMATION

Synchronous rectifier buck regulator circuits are used where high efficiency and low dropout voltages are required. The TPS56xx controller is useful in applications with very high transient loads and wide dc load ranges, such as multiple-DSP applications.

The circuit below will meet a wide variety of applications with maximum continuous-rated output currents of up to 8 A. Design tradeoffs, such as cost, size, or efficiency may need to be addressed for specific applications. Care should be taken in the proper layout (see last section of this data sheet for specific layout guidelines), especially in the higher-current configurations, to ensure that noise and ripple are kept to a minimum. Basic layout considerations are discussed in the *1996 Power Supply Circuits Databook* (Literature no. SLVD002). Design guidelines and equations are discussed in *Synchronous Buck Converter Design Using TPS56xx Controllers in SLVP10x EVMs User's Guide* (Literature no. SLVU007).

APPLICATION INFORMATION



NOTE A: Theses two traces should be physically close to each other for good noise immunity.

Figure 24. Typical Design Schematic

Table 1. Test Results for 2.5-V, 8-A Converter

TEST	CONDITIONS		QTY	UNITS
Output voltage	V_{IN} = 5.25 V,	I_O = 8 A	2.50	V
Load regulation	V_{IN} = 5.25 V,	I_O = 0.8 to 8 A	0.4	%
Line regulation	I_O =6 A,	V_{CC} = 4.5 V to 6 V	0.2	%
Ripple	V_{IN} = 5.25 V,	I_O = 8 A	50	mVpp
Efficiency	V_{IN} = 5.25 V,	I_O = 8 A	89	%

Table 2. 2.5-V, 8-A Converter Bill of Materials

REF DES	QTY	PART NUMBER	DESCRIPTION	MFG
C1	1	10SS22M	Capacitor, Os-Con, 22 µF, 10 V, 20%	Sanyo
C2	4	GRM39X7R104K016A	Capacitor, Ceramic, 0.1 µF, 16 V, 10%, X7R	muRata
C3		GRM39X7R104K016A	Capacitor, Ceramic, 0.1 µF, 16 V, 10%, X7R	muRata
C4	4	GRM42-6Y5V105Z016A	Capacitor, Ceramic, 1 µF, 16 V, +80%–20%	muRata
C5	1	GRM42-6Y5V225Z016A	Capacitor, Os-Con, 2.2 µF, 16 V, Y5U	muRata
C6	1	6SP680M	Capacitor, Os-Con, 680 µF, 6.3 V, 20%	Sanyo
C7		GRM42-6Y5V105Z016A	Capacitor, Ceramic, 1 µF, 16 V, +80%–20%	muRata
C8	2	GRM39X7R103K025A	Capacitor, Ceramic, 0.01 µF, 25 V, 10%, X7R	muRata
C9	1	4SP820M	Capacitor, Os-Con, 820 µF, 4 V, 20%	Sanyo
C10	1	GRM235Y5V106Z016A	Capacitor, Ceramic, 10 µF, 16 V, Y5V	muRata
C11		GRM42-6Y5V105Z016A	Capacitor, Ceramic, 1 µF, 16 V, +80%–20%	muRata
C12		GRM39X7R104K016A	Capacitor, Ceramic, 0.1 µF, 16 V, 10%, X7R	muRata
C14		GRM39X7R103K025A	Capacitor, Ceramic, 0.01 µF, 25 V, 10%, X7R	muRata
C15	1	GRM39X7R102K050A	Capacitor, Ceramic, 1000 pF, 50 V, 10%, X7R	muRata
C16		GRM39X7R104K016A	Capacitor, Ceramic, 0.1 µF, 16 V, 10%, X7R	muRata
C17		GRM42-6Y5V105Z016A	Capacitor, Ceramic, 1 µF, 16 V, +80%–20%	muRata
C18		GRM39X7R104K016A	Capacitor, Ceramic, 0.1 µF, 16 V, 10%, X7R	muRata
J1	1	S1122-18-ND	Header, RA, 18-pin, 0.23 Posts × 0.20 Tails	Sullins
L1	1		Inductor, Filter, 2.2 µH, 8.5 A (10T #22 on T30-18 Core)	
L2	1		Inductor, Filter, 2.6 µH, 8.5 A (12T #20 on T44-8 Core)	
Q1	2	Si4410DY	FET, N-ch, 30-V, 10-A, 13-mΩ	Siliconix
Q2		Si4410DY	FET, N-ch, 30-V, 10-A, 13-mΩ	Siliconix
R1	3	Std	Resistor, Chip, 1.0 kΩ, 1/16W, 5%	
R2	1	Std	Resistor, Chip, 10 kΩ, 1/16W, 5%	
R3	2	Std	Resistor, Chip, 10 Ω, 1/10W, 5%	
R4		Std	Resistor, Chip, 10 Ω, 1/10W, 5%	
R5	1	Std	Resistor, Chip, 2.7 Ω, 1/4W, 5%	
R6		Std	Resistor, Chip, 1.3 kΩ, 1/16W, 5%	
R7	1	Std	Resistor, Chip, 11.0 kΩ, 1/16W, 1%	
R8	2	Std	Resistor, Chip, 100 Ω, 1/16W, 1%	
R9		Std	Resistor, Chip, 100 Ω, 1/16W, 1%	
R11		Std	Resistor, Chip, 750 Ω, 1/16W, 5%	
R12	1	Std	Resistor, Chip, 20.0 kΩ, 1/16W, 1%	
R15	2	Std	Resistor, Chip, 4.7 Ω, 1/16W, 5%	
R16		Std	Resistor, Chip, 4.7 Ω, 1/16W, 5%	
R17	1	Std	Resistor, Chip, 1 MΩ, 1/16W, 5%	
U1	1	TPS5625PWP	IC, PWM Ripple Controller, FIxed 2.5 V	TI

APPLICATION INFORMATION

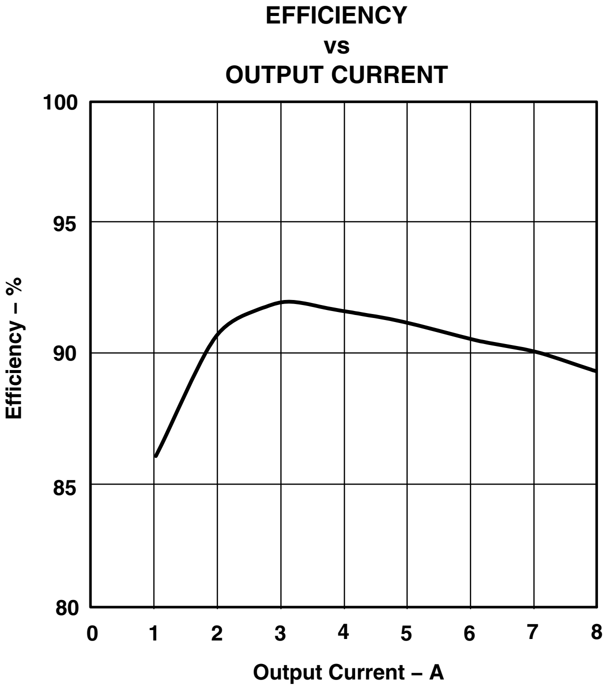


Figure 25

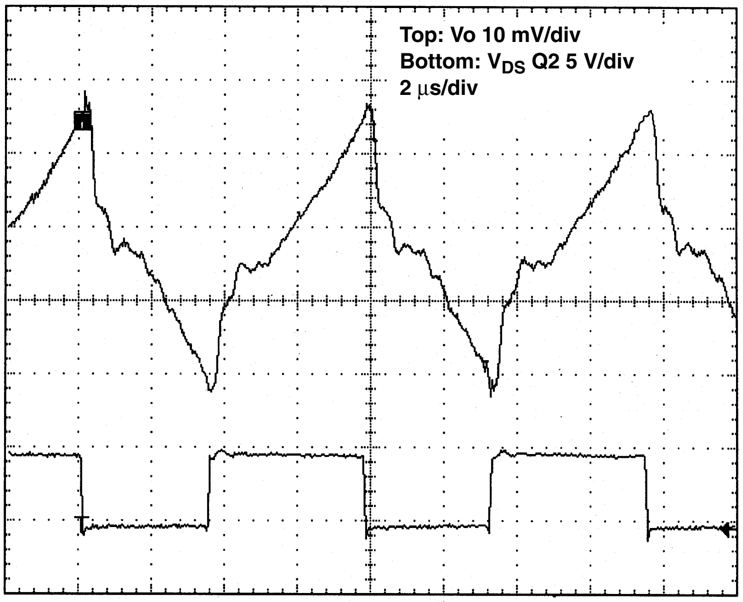


Figure 26. Output Voltage Ripple at 8 A

APPLICATION INFORMATION

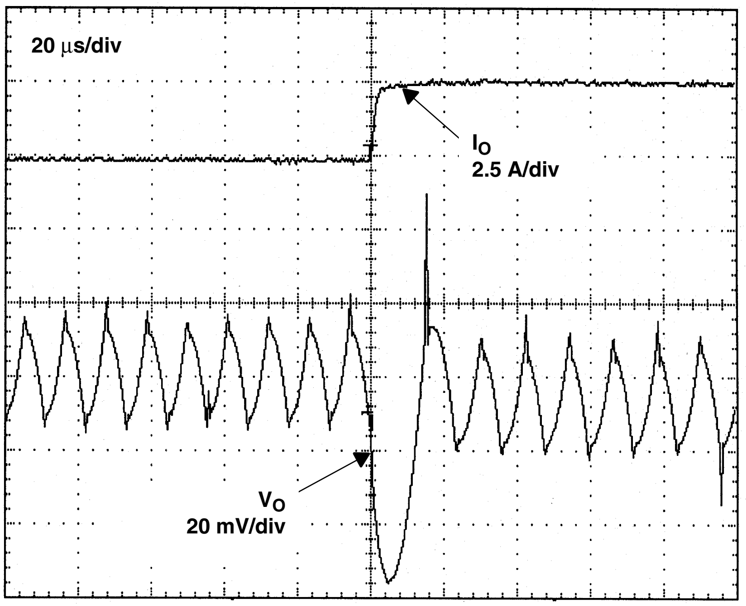


Figure 27. Rising Load Transient Response

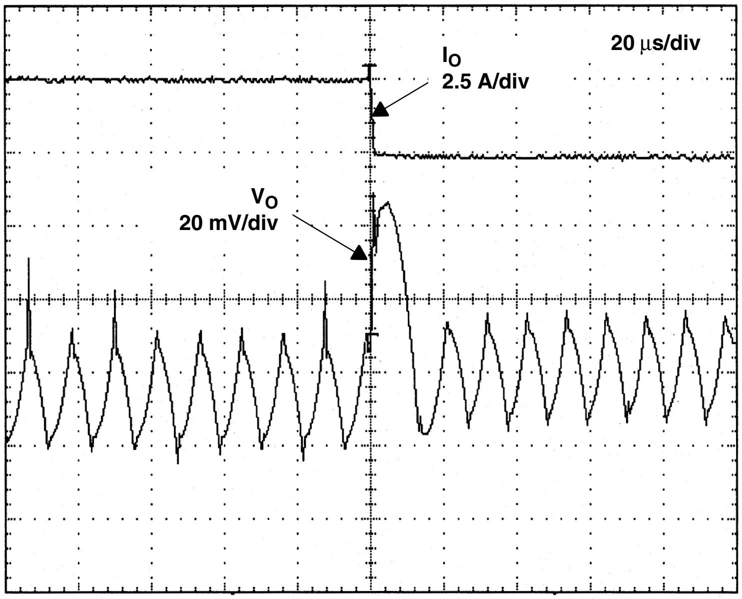


Figure 28. Falling Load Transient Response

APPLICATION INFORMATION

layout guidelines

Good power supply results will only occur when care is given to proper design and layout. Layout will affect noise pickup and generation and can cause a good design to perform with less than expected results. With a range of currents from milliamps to tens or even hundreds of amps, good power supply layout is much more difficult than most general PCB design. The general design should proceed from the switching node to the output, then back to the driver section and, finally, place the low-level components. Below are several specific points to consider before layout of a TPS56xx design begins.

1. All sensitive analog components should be referenced to ANAGND. These include components connected to SLOWST, IOUT, OCP, VSENSE, VREFB, VHYST, BIAS, and LOHIB.
2. Analog ground and drive ground should be isolated as much as possible. Ideally, analog ground will connect to the ground side of the bulk storage capacitors, on V_O, and drive ground will connect to the main ground plane close to the source of the low-side FET.
3. Connections from the drivers to the gate of the power FETs should be as short and wide as possible to reduce stray inductance. This becomes more critical if external gate resistors are not being used.
4. The bypass capacitor for the DRV regulator should be placed close to the TPS56xx and be connected to DRVGND.
5. The bypass capacitor for V_{CC} should be placed close to the TPS56xx and be connected to DRVGND.
6. When configuring the high-side driver as a floating driver, the connection from BOOTLO to the power FETs should be as short and as wide as possible. The other pins that also connect to the power FETs, LOHIB and LOSENSE, should have a separate connection to the FETs, since BOOTLO will have large peak currents flowing through it.
7. When configuring the high-side driver as a floating driver, the bootstrap capacitor (connected from BOOT to BOOTLO) should be placed close to the TPS56xx.
8. When configuring the high-side driver as a ground referenced driver, BOOTLO should be connected to DRVGND.
9. The bulk storage capacitors across V_I should be placed close to the power FETs. High-frequency bypass capacitors should be placed in parallel with the bulk capacitors and connected close to the drain of the high-side FET and close to the source of the low-side FET.
10. High-frequency bypass capacitors should be placed across the bulk storage capacitors on V_O.
11. HISENSE and LOSENSE should be connected very close to the drain and source, respectively, of the high-side FET. HISENSE and LOSENSE should be routed very close to each other to minimize differential-mode noise coupling to these traces.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS5618PWP	ACTIVE	HTSSOP	PWP	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		TPS5618	Samples
TPS5633PWP	ACTIVE	HTSSOP	PWP	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		TPS5633	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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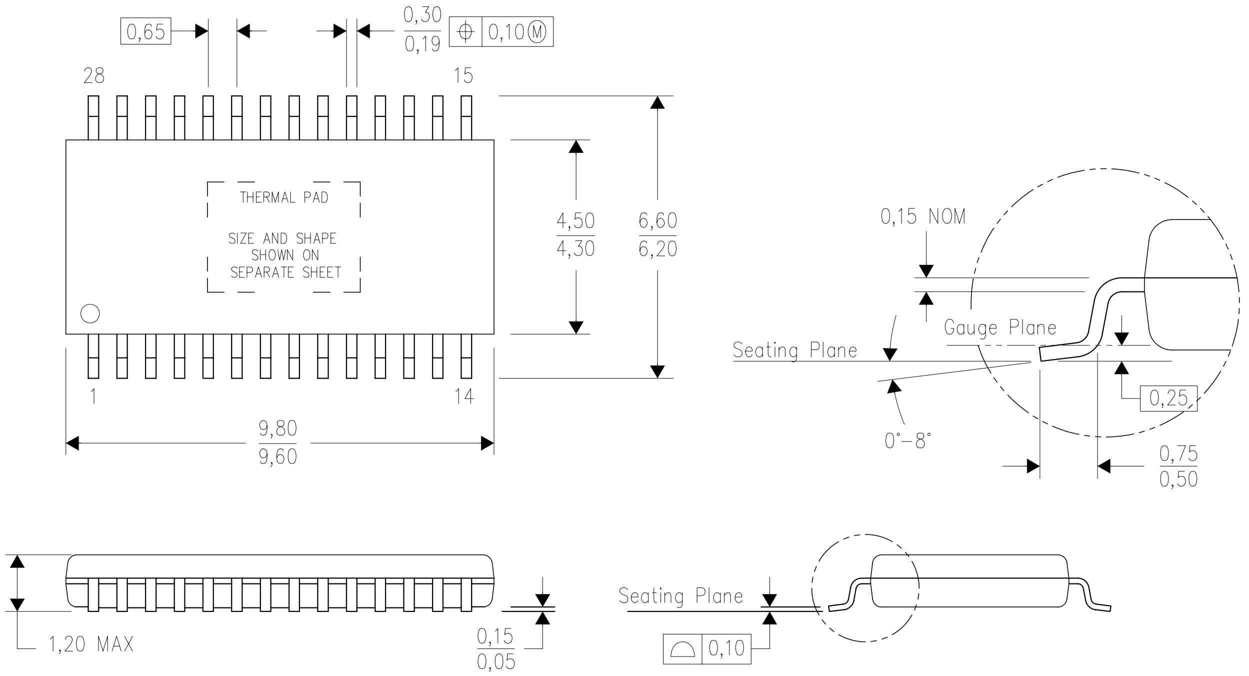
PWP (R-PDSO-G28) PowerPAD™ PLASTIC SMALL OUTLINE



4073225-6/I 05/11

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- E. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

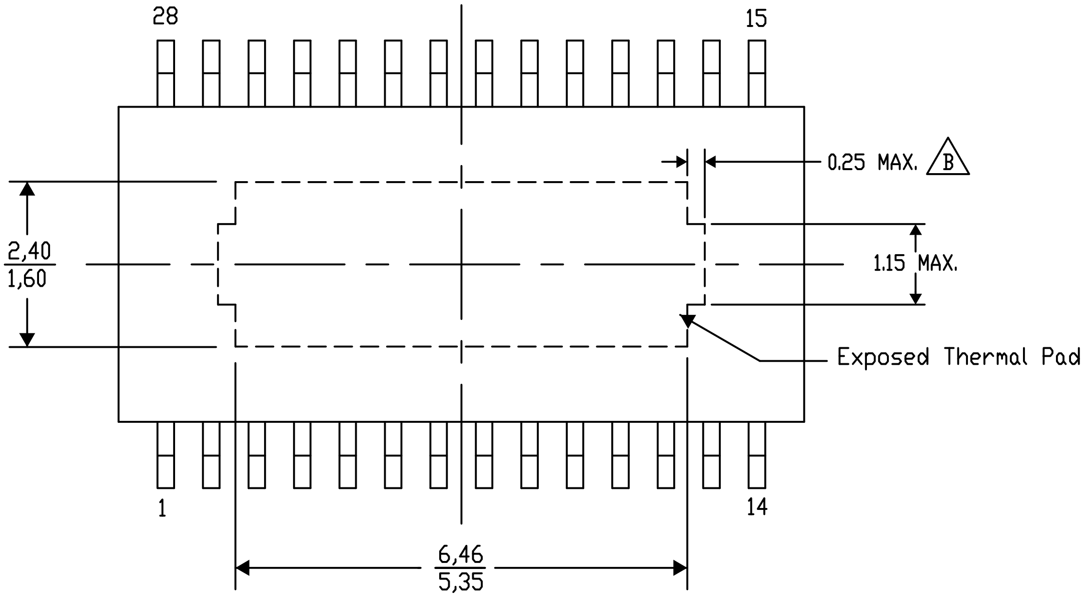
PWP (R-PDSO-G28) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332-34/AH 11/13

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

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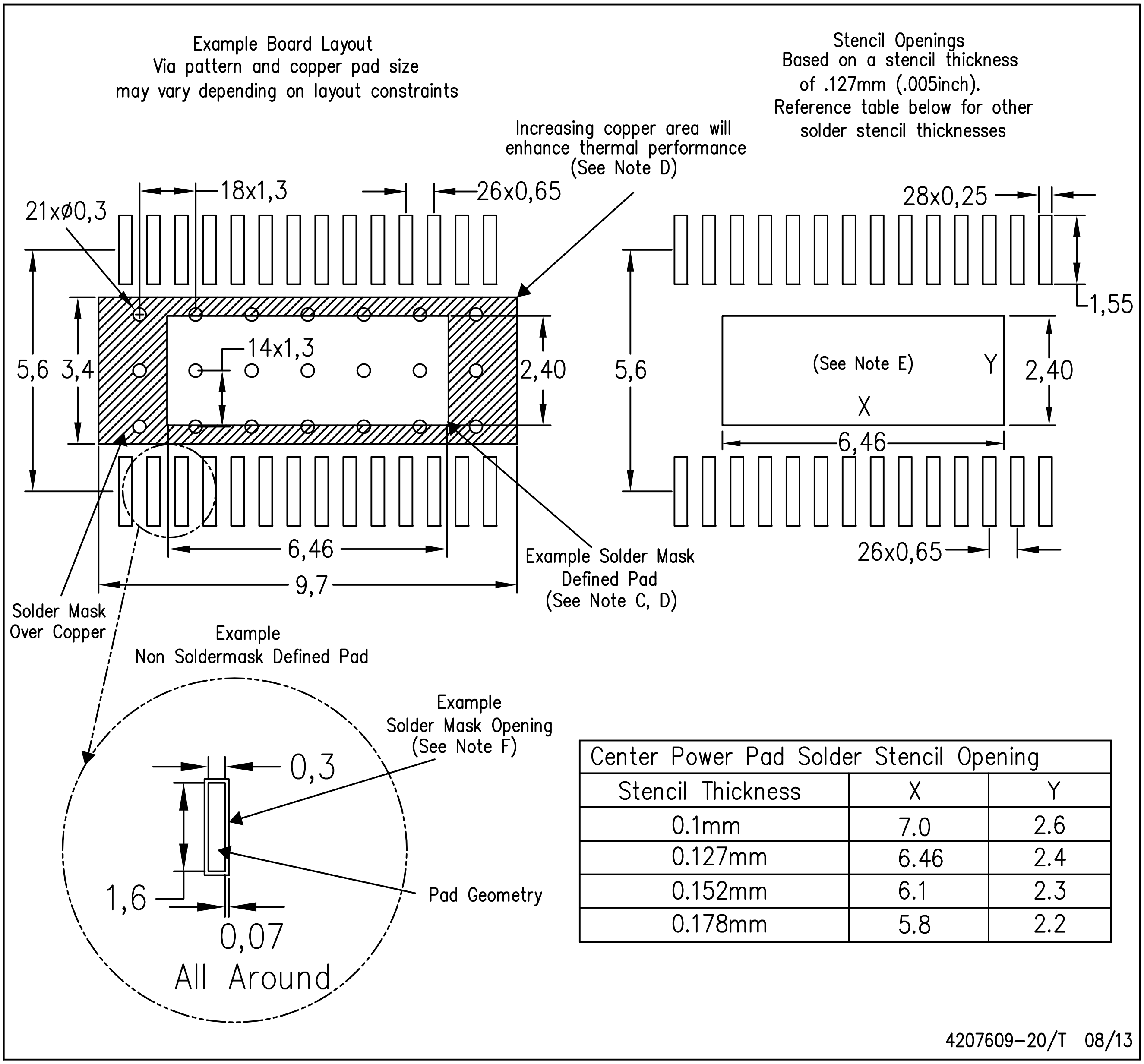

Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	7.0	2.6
0.127mm	6.46	2.4
0.152mm	6.1	2.3
0.178mm	5.8	2.2

4207609-20/T 08/13

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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