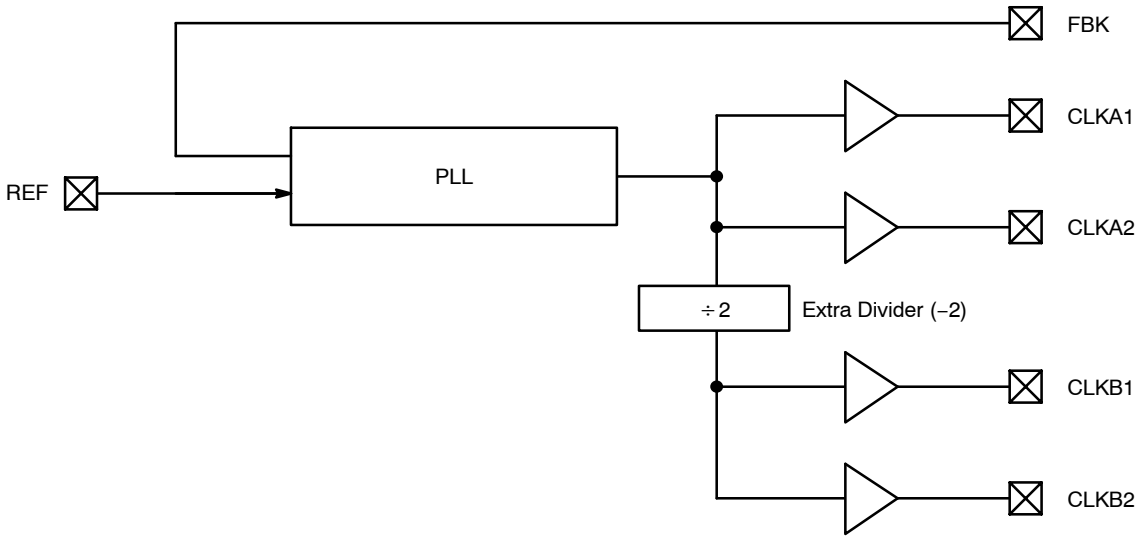


Figure 1. Basic Block Diagram
(see Figures 10 and 11 for device specific Block Diagrams)

Table 1. CONFIGURATIONS

Device	Feedback From	Bank A Frequency	Bank B Frequency
NB2304AI1	Bank A or Bank B	Reference	Reference
NB2304AI2	Bank A	Reference	Reference ÷2
NB2304AI2	Bank B	2 X Reference	Reference

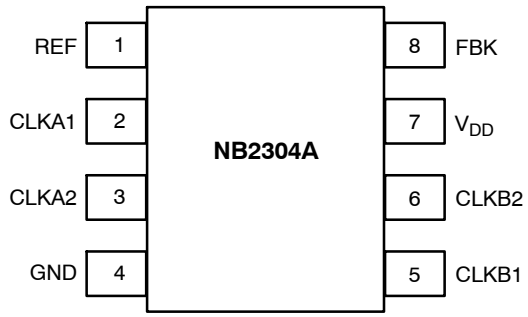


Figure 2. Pin Configuration

Table 2. PIN DESCRIPTION

Pin #	Pin Name	Description
1	REF (Note 1)	Input reference frequency, 5 V tolerant input.
2	CLKA1 (Note 2)	Buffered clock output, Bank A.
3	CLKA2 (Note 2)	Buffered clock output, Bank A.
4	GND	Ground.
5	CLKB1 (Note 2)	Buffered clock output, Bank B.
6	CLKB2 (Note 2)	Buffered clock output, Bank B.
7	V_{DD}	3.3 V supply.
8	FBK	PLL feedback input.

1. Weak pulldown.
2. Weak pulldown on all outputs.

Table 3. MAXIMUM RATINGS

Parameter	Min	Max	Unit
Supply Voltage to Ground Potential	−0.5	+7.0	V
DC Input Voltage (Except REF)	−0.5	V_{DD} + 0.5	V
DC Input Voltage (REF)	−0.5	7	V
Storage Temperature	−65	+150	°C
Maximum Soldering Temperature (10 sec)		260	°C
Junction Temperature		150	°C
Static Discharge Voltage (per MIL−STD−883, Method 3015)		> 2000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 4. OPERATING CONDITIONS

Parameter	Description		Min	Max	Unit
V_{DD}	Supply Voltage		3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	Industrial Commercial	−40 0	85 70	°C
C_L	Load Capacitance, 15 MHz to 100 MHz			30	pF
C_L	Load Capacitance, from 100 MHz to 133 MHz			15	pF
C_{IN}	Input Capacitance (Note 3)			7	pF

3. Applies to both REF Clock and FBK.

Table 5. ELECTRICAL CHARACTERISTICS V_{CC} = 3.0 V to 3.6 V, GND = 0 V, T_A = −40°C to +85°C

Parameter	Description	Test Conditions	Min	Max	Unit
V_{IL}	Input LOW Voltage			0.8	V
V_{IH}	Input HIGH Voltage		2.0		V
I_{IL}	Input LOW Current	V_{IN} = 0 V		50.0	μA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}		100.0	μA
V_{OL}	Output LOW Voltage	I_{OL} = 8 mA (−1, −2)		0.4	V
V_{OH}	Output HIGH Voltage	I_{OH} = −8 mA (−1, −2)	2.4		V
I_{DD}	Supply Current	Unloaded outputs 100 MHz REF Select inputs at V_{DD} or GND		45	mA
		Unloaded outputs, 66 MHz REF (−1, −2)		35	
		Unloaded outputs, 33 MHz REF (−1, −2)		20	

Table 6. SWITCHING CHARACTERISTICS V_{CC} = 3.0 V to 3.6 V, GND = 0 V, T_A = −40°C to +85°C
(All parameters are specified with loaded outputs)

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
t_1	Output Frequency	30 pF load (all devices) 15 pF load (−1, −2)	15 15		100 133.3	MHz
t_1	Duty Cycle = (t_2 / t_1) * 100 (all devices)	Measured at 1.4 V, $F_{OUT} \leq$ 66.66 MHz 30 pF load	40.0	50.0	60.0	%
		Measured at 1.4 V, $F_{OUT} \leq$ 50 MHz 15 pF load	45.0	50.0	55.0	
t_3	Output Rise Time (−1, −2)	Measured between 0.8 V and 2.0 V 30 pF load			2.50	ns
		Measured between 0.8 V and 2.0 V 15 pF load			1.50	
t_4	Output Fall Time (−1, −2)	Measured between 2.0 V and 0.8 V 30 pF load			2.50	ns
		Measured between 2.0 V and 0.8 V 15 pF load			1.50	
t_5	Output−to−Output Skew on same Bank (−1, −2)	All outputs equally loaded			200	ps
	Output Bank A−to−Output Bank B skew (−1)	All outputs equally loaded			200	
	Output Bank A−to−Output Bank B skew (−2)	All outputs equally loaded			400	
t_6	Delay, REF Rising Edge to FBK Rising Edge	Measured at V_{DD}/2		0	±250	ps
t_7	Device−to−Device Skew	Measured at V_{DD}/2 on the FBK pins of the device		0	500	ps
t_J	Cycle−to−Cycle Jitter (−1)	Measured at 66.67 MHz, loaded outputs, 15 pF load			180	ps
		Measured at 66.67 MHz, loaded outputs, 30 pF load			200	
		Measured at 133.3 MHz, loaded outputs, 15 pF load			100	
	Cycle−to−Cycle Jitter (−2)	Measured at 66.67 MHz, loaded outputs, 30 pF load			400	ps
		Measured at 66.67 MHz, loaded outputs, 15 pF load			380	
t_{LOCK}	PLL Lock Time	Stable power supply, valid clock presented on REF and FBK pins			1.0	ms

Zero Delay and Skew Control

For applications requiring zero input−output delay, all outputs must be equally loaded.

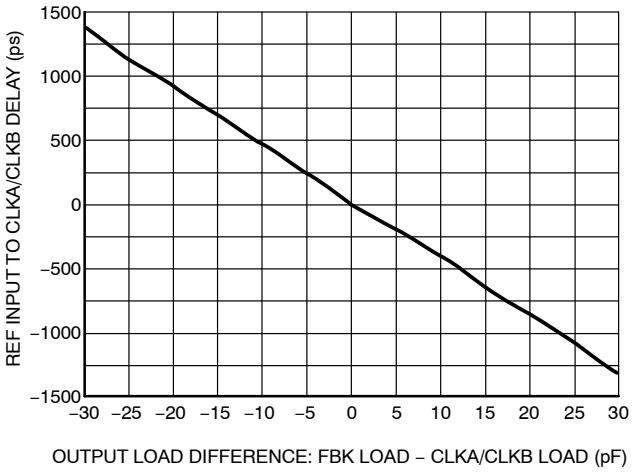


Figure 3. REF Input to CLKA/CLKB Delay vs. Difference in Loading between FBK Pin and CLKA/CLKB Pins

To close the feedback loop of the NB2304A, the FBK pin can be driven from any of the four available output pins. The output driving the FBK pin will be driving a total load of 7 pF plus any additional load that it drives. The relative loading of this output (with respect to the remaining outputs) can adjust the input output delay. This is shown in Figure 3.

For applications requiring zero input−output delay, all outputs including the one providing feedback should be equally loaded. If input−output delay adjustments are required, use Figure 3 to calculate loading differences between the feedback output and remaining outputs. For zero output−output skew, be sure to load outputs equally.

SWITCHING WAVEFORMS

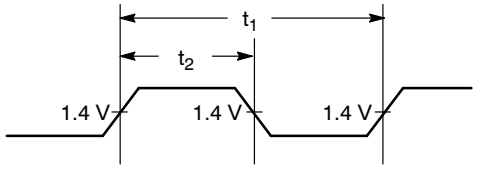


Figure 4. Duty Cycle Timing

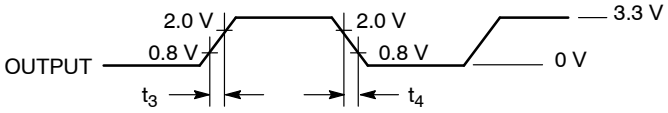


Figure 5. All Outputs Rise/Fall Time

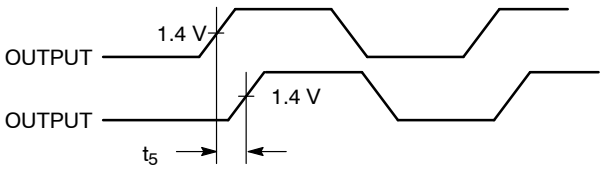


Figure 6. Output − Output Skew

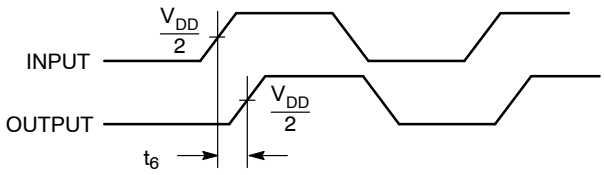


Figure 7. Input − Output Propagation Delay

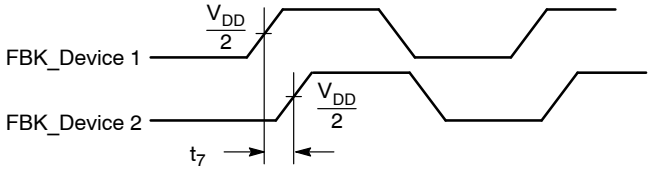


Figure 8. Device − Device Skew

TEST CIRCUITS

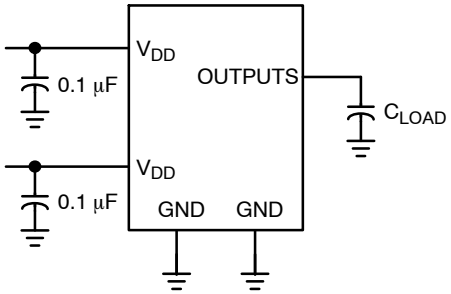


Figure 9. Test Circuit #1

BLOCK DIAGRAMS

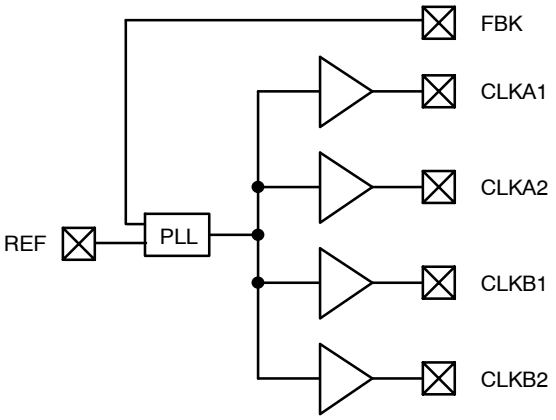


Figure 10. NB2304AI1

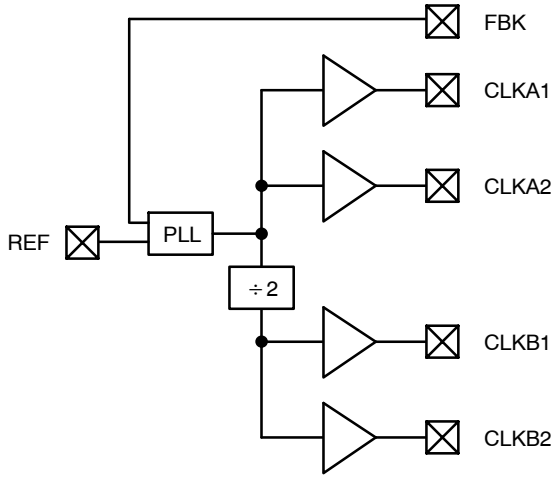


Figure 11. NB2304AI2

ORDERING INFORMATION

Device	Marking	Operating Range	Package	Shipping†	Availability
NB2304AI1DR2G	4I1	Industrial & Commercial	SOIC−8 (Pb−Free)	2500 Tape & Reel	*Now*
NB2304AI2DG	4I2	Industrial & Commercial	SOIC−8 (Pb−Free)	98 Units / Tube	*Now*
NB2304AI2DR2G	4I2	Industrial & Commercial	SOIC−8 (Pb−Free)	2500 Tape & Reel	*Now*

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

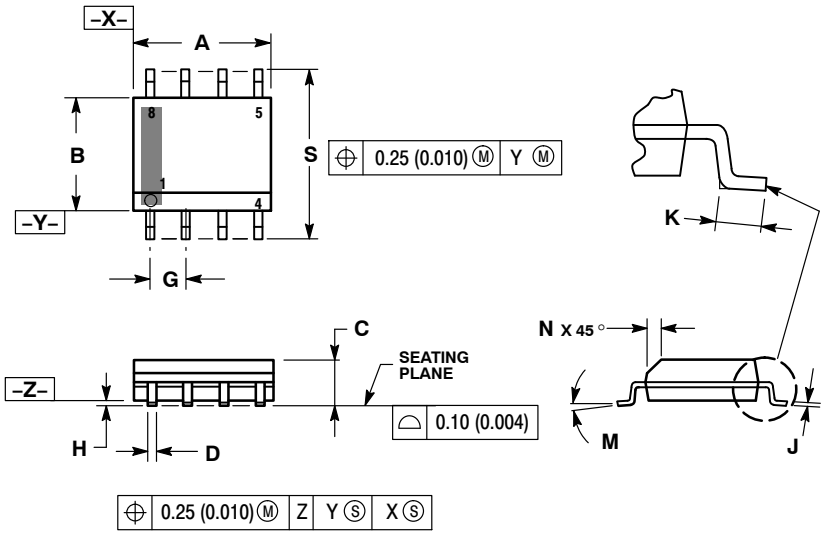
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

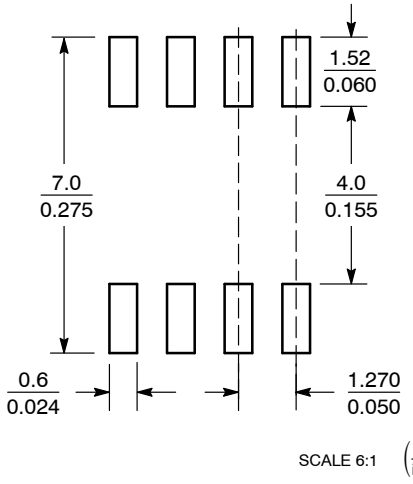
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

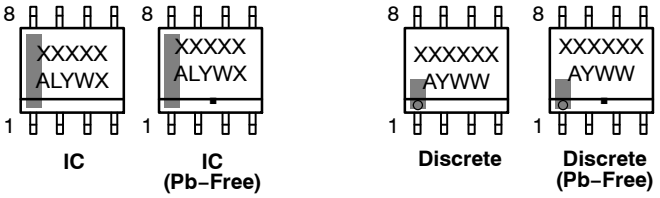
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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