SN74ACT7811
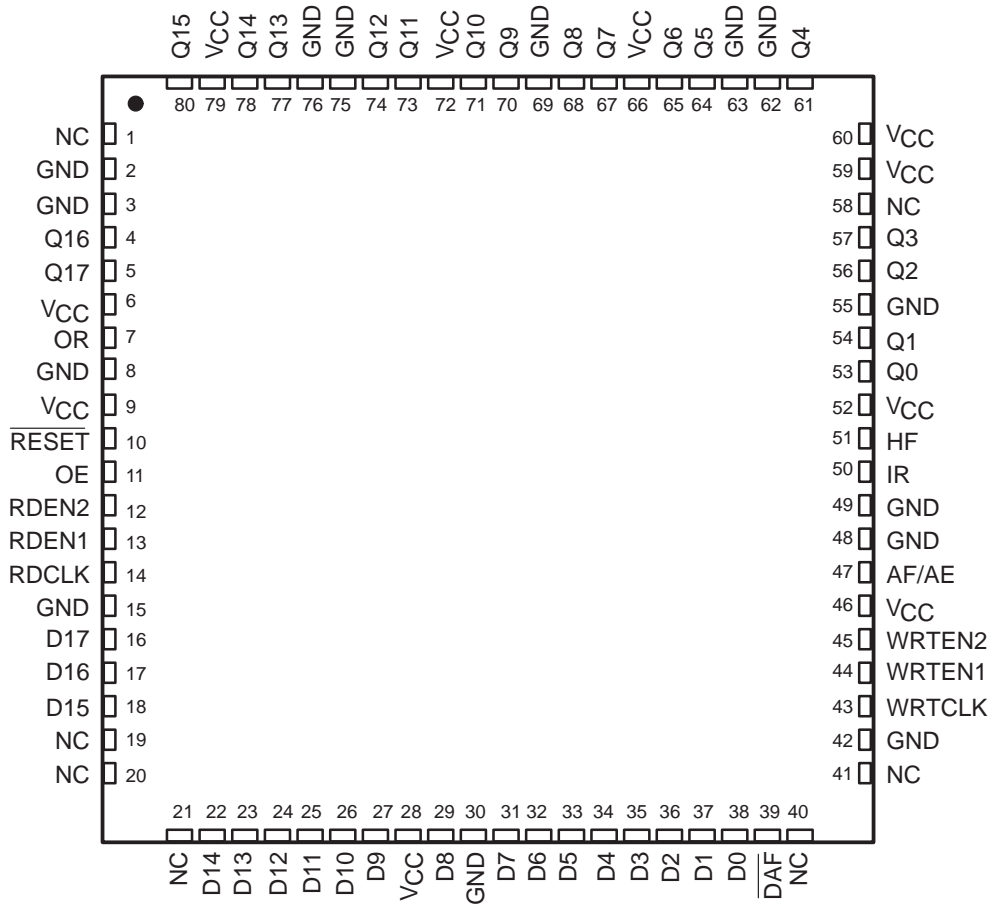## 1024 × 18
CLOCKED FIRST-IN, FIRST-OUT MEMORY

SCAS151C – JANUARY 1991 – REVISED FEBRUARY 1996

PN PACKAGE
(TOP VIEW)

Top pins (left to right): Q15, VCC, Q14, Q13, GND, GND, Q12, Q11, VCC, Q10, Q9, GND, Q8, Q7, VCC, Q6, Q5, GND, GND, Q4 (pins 80–61)

Left pins (top to bottom):
Pin	Signal
1	NC
2	GND
3	GND
4	Q16
5	Q17
6	VCC
7	OR
8	GND
9	VCC
10	RESET
11	OE
12	RDEN2
13	RDEN1
14	RDCLK
15	GND
16	D17
17	D16
18	D15
19	NC
20	NC

Right pins (top to bottom):
Pin	Signal
60	VCC
59	VCC
58	NC
57	Q3
56	Q2
55	GND
54	Q1
53	Q0
52	VCC
51	HF
50	IR
49	GND
48	GND
47	AF/AE
46	VCC
45	WRTEN2
44	WRTEN1
43	WRTCLK
42	GND
41	NC

Bottom pins (left to right, pins 21–40): NC, D14, D13, D12, D11, D10, D9, VCC, D8, GND, D7, D6, D5, D4, D3, D2, D1, D0, DAF, NC

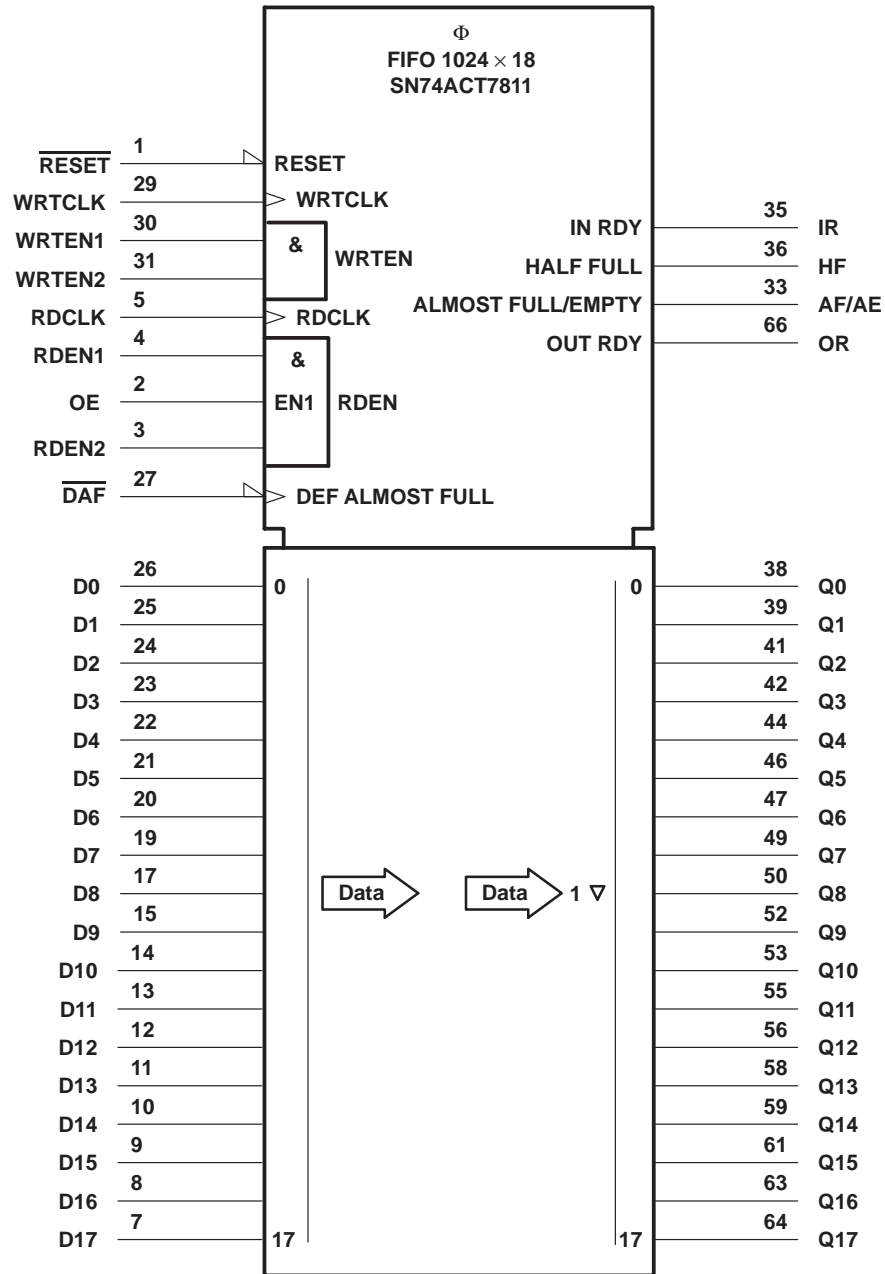NC – No internal connection

description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ACT7811 is a 1024 × 18-bit FIFO for high speed and fast access times. It processes data at rates up to 40 MHz and access times of 15 ns in a bit-parallel format. Data outputs are noninverting with respect to the data inputs. Expansion is easily accomplished in both word width and word depth.

The SN74ACT7811 has normal input-bus-to-output-bus asynchronous operation. The special enable circuitry adds the ability to synchronize independent read and write (interrupts or requests) to their respective system clock.

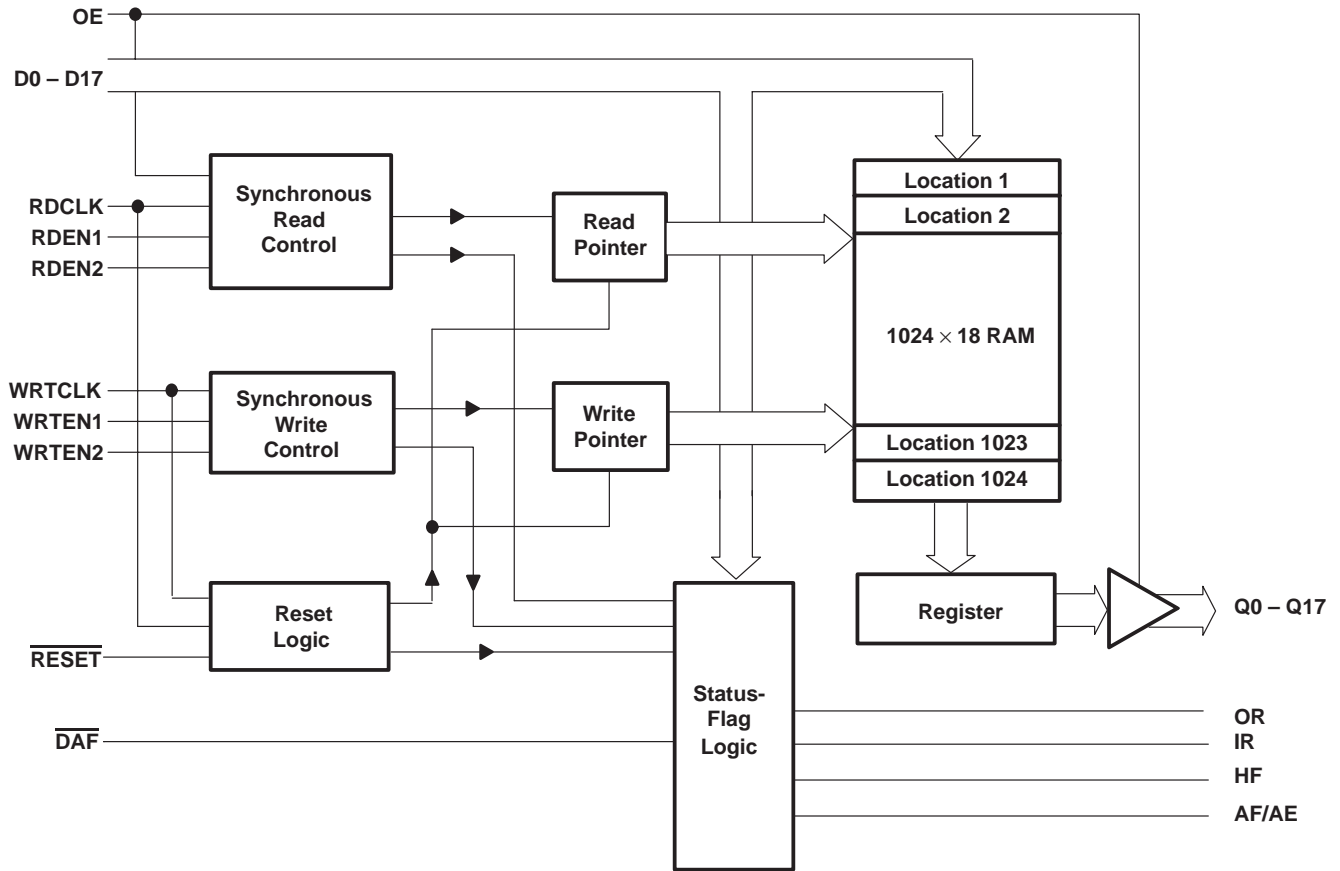The SN74ACT7811 is characterized for operation from 0°C to 70°C.

logic symbol†

Pin	Signal		Signal	Pin

Φ
FIFO 1024 × 18
SN74ACT7811

$\overline{\text{RESET}}$ — 1 — RESET

WRTCLK — 29 — WRTCLK

WRTEN1 — 30 — &
WRTEN2 — 31 — WRTEN

RDCLK — 5 — RDCLK

RDEN1 — 4 — &
OE — 2 — EN1 RDEN
RDEN2 — 3 —

$\overline{\text{DAF}}$ — 27 — DEF ALMOST FULL

IN RDY — 35 — IR
HALF FULL — 36 — HF
ALMOST FULL/EMPTY — 33 — AF/AE
OUT RDY — 66 — OR

D	Pin in	Pin out	Q
D0	26	38	Q0
D1	25	39	Q1
D2	24	41	Q2
D3	23	42	Q3
D4	22	44	Q4
D5	21	46	Q5
D6	20	47	Q6
D7	19	49	Q7
D8	17	50	Q8
D9	15	52	Q9
D10	14	53	Q10
D11	13	55	Q11
D12	12	56	Q12
D13	11	58	Q13
D14	10	59	Q14
D15	9	61	Q15
D16	8	63	Q16
D17	7	64	Q17

0 ... 17 Data → Data → 1 ▽ 0 ... 17

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the FN package.

functional block diagram

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Terminal Functions

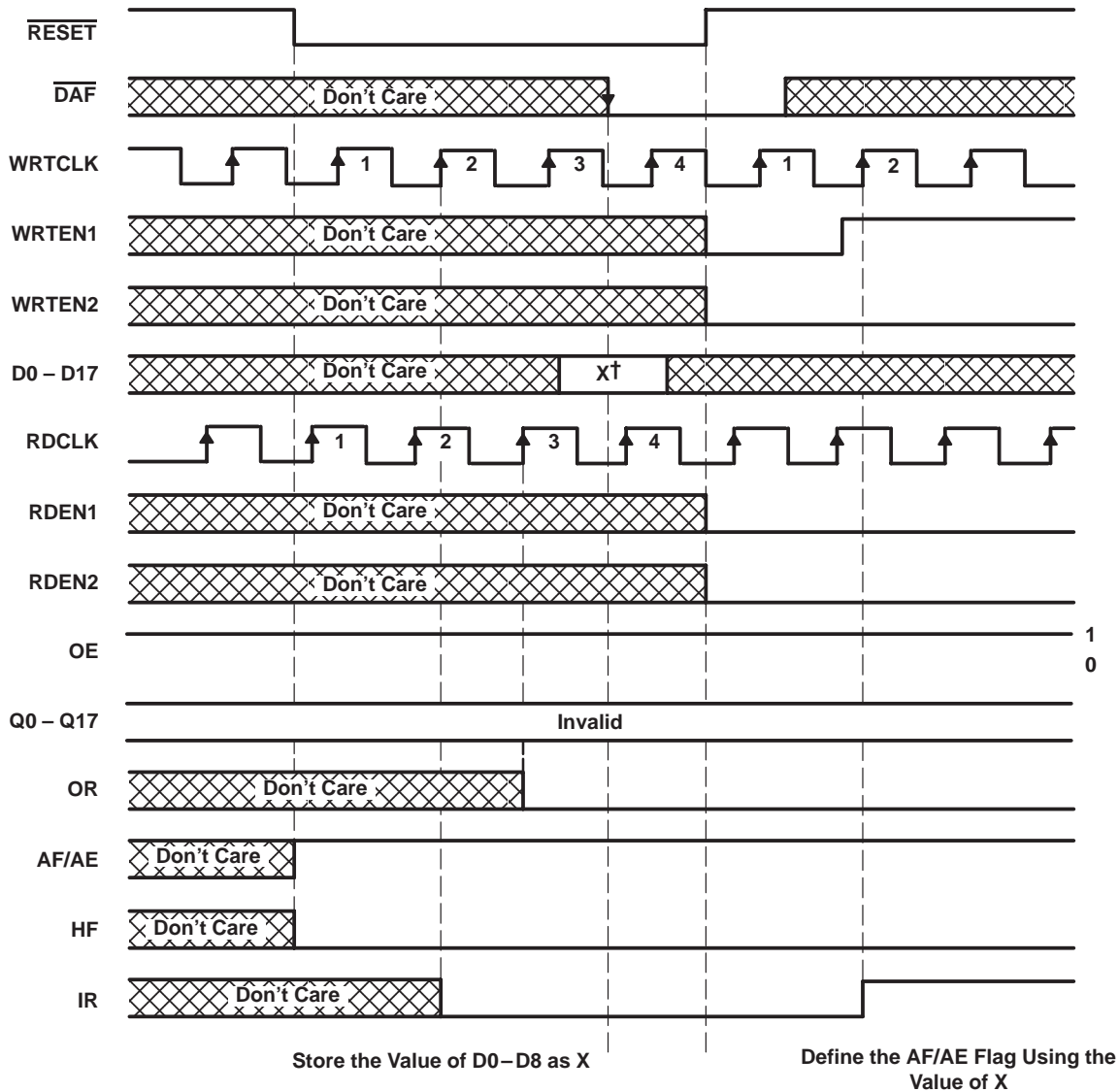| TERMINAL[†]		I/O	DESCRIPTION
NAME	NO.		
AF/AE	33	O	Almost-full/almost-empty flag. The AF/AE boundary is defined by the almost-full/almost-empty offset value (X). This value can be programmed during reset or the default value of 256 can be used. AF/AE is high when the FIFO contains (X + 1) or less words or (1025 – X) or more words. AF/AE is low when the FIFO contains between (X + 2) and (1024 - X) words. Programming procedure for AF/AE – The almost-full/almost-empty flag is programmed during each reset cycle. The almost-full/almost-empty offset value (X) is either a user-defined value or the default of X = 256. Instructions to program AF/AE using both methods are as follows: _User-defined X_ Step 1: Take $\overline{DAF}$ from high to low. Step 2: If $\overline{RESET}$ is not already low, take $\overline{RESET}$ low. Step 3: With $\overline{DAF}$ held low, take $\overline{RESET}$ high. This defines the AF/AE using X. Step 4: To retain the current offset for the next reset, keep $\overline{DAF}$ low. _Default X_ To redefine AF/AE using the default value of X = 256, hold $\overline{DAF}$ high during the reset cycle.
$\overline{DAF}$	27	I	Define almost full. The high-to-low transition of $\overline{DAF}$ stores the binary value of data inputs as the almost-full/almost-empty offset value (X). With $\overline{DAF}$ held low, a low pulse on $\overline{RESET}$ defines the AF/AE flag using X.
D0–D17	26–19, 17, 15–7	I	Data inputs for 18-bit-wide data to be stored in the memory. Data lines D0–D8 also carry the almost-full/almost-empty offset value (X) on a high-to-low transition of the $\overline{DAF}$.
HF	36	O	Half-full flag. HF is high when the FIFO contains 513 or more words and is low when it contains 512 or less words.
IR	35	O	Input-ready flag. IR is high when the FIFO is not full and low when the device is full. During reset, IR is driven low on the rising edge of the second WRTCLK pulse. IR is then driven high on the rising edge of the second WRTCLK pulse after $\overline{RESET}$ goes high. After the FIFO is filled and IR is driven low, IR is driven high on the second WRTCLK pulse after the first valid read.
OE	2	I	Output enable. The data-out (Q0–Q17) outputs are in the high-impedance state when OE is low. OE must be high before the rising edge of RDCLK to read a word from memory.
OR	66	O	Output-ready flag. OR is high when the FIFO is not empty and low when it is empty. During reset, OR is set low on the rising edge of the third RDCLK pulse. OR is set high on the rising edge of the third RDCLK pulse to occur after the first word is written into the FIFO. OR is set low on the rising edge of the first RDCLK pulse after the last word is read.
Q0–Q17	38–39, 41–42, 44, 46–47, 49–50, 52–53, 55–56, 58–59, 61, 63–64	O	Data outputs. The first data word to be loaded into the FIFO is moved to Q0–Q17 on the rising edge of the third RDCLK pulse to occur after the first valid write. The RDEN1 and RDEN2 inputs do not affect this operation. Following data is unloaded on the rising edge of RDCLK when RDEN1, RDEN2, OE, and the OR are high.
RDCLK	5	I	Read clock. Data is read out of memory on a low-to-high transition RDCLK if OR, OE, and RDEN1 and RDEN2 control inputs are high. RDCLK is a free-running clock and functions as the synchronizing clock for all data transfers out of the FIFO. OR is also driven synchronously with respect to RDCLK.
RDEN1, RDEN2	4, 3	I	Read enable. RDEN1 and RDEN2 must be high before a rising edge on RDCLK to read a word out of memory. RDEN1 and RDEN2 are not used to read the first word stored in memory.
$\overline{RESET}$	1	I	A reset is accomplished by taking $\overline{RESET}$ low and generating a minimum of four RDCLK and WRTCLK cycles. This ensures that the internal read and write pointers are reset and OR, HF, and IR are low and AF/AE is high. The FIFO must be reset upon power up. With $\overline{DAF}$ at a low level, a low pulse on $\overline{RESET}$ defines the AF/AE status flag using the almost-full/almost-empty offset value (X), where X is the value previously stored. With $\overline{DAF}$ at a high level, a low-level pulse on $\overline{RESET}$ defines the AF/AE flag using the default value of X = 256.

† Terminals listed are for the FN package.

Terminal Functions (Continued)

TERMINAL†		I/O	DESCRIPTION
NAME	**NO.**		
WRTCLK	29	I	Write clock. Data is written into memory on a low-to-high transition of WRTCLK if IR, WRTEN1, and WRTEN2 are high. WRTCLK is a free-running clock and functions as the synchronizing clock for all data transfers into the FIFO. IR is also driven synchronously with respect to WRTCLK.
WRTEN1, WRTEN2	30 31	I	Write enables. WRTEN1 and WRTEN2 must be high before a rising edge on WRTCLK for a word to be written into memory. WRTEN1 and WRTEN2 do not affect the storage of the almost-full/almost-empty offset value (X).

† Terminals listed are for the FN package.

† X is the binary value of D0−D8 only.

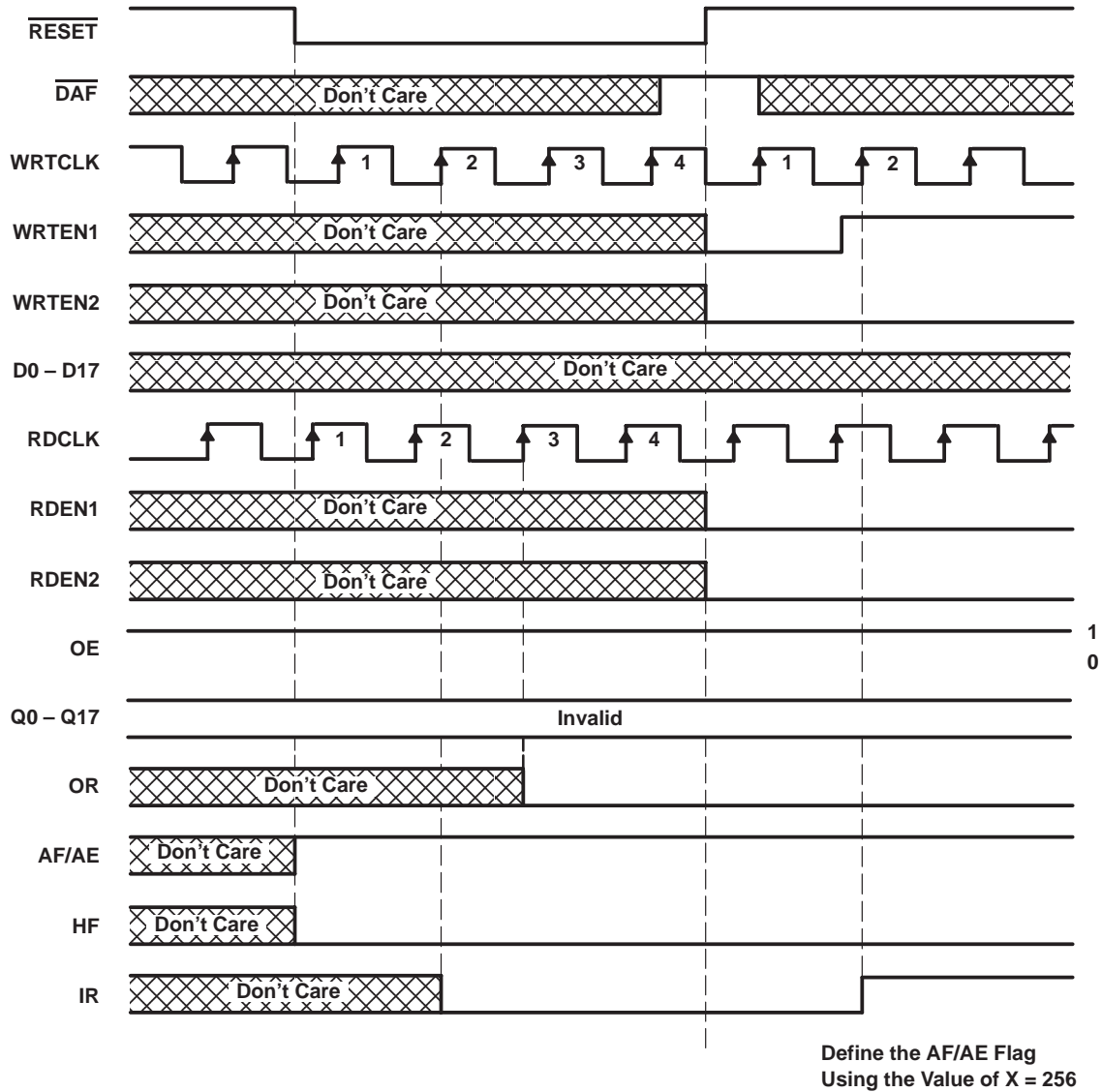**Figure 1. Reset Cycle: Define AF/AE Using the Value of X**

Define the AF/AE Flag
Using the Value of X = 256

Figure 2. Reset Cycle: Define AF/AE Using the Default Value

Figure 3. Write Cycle

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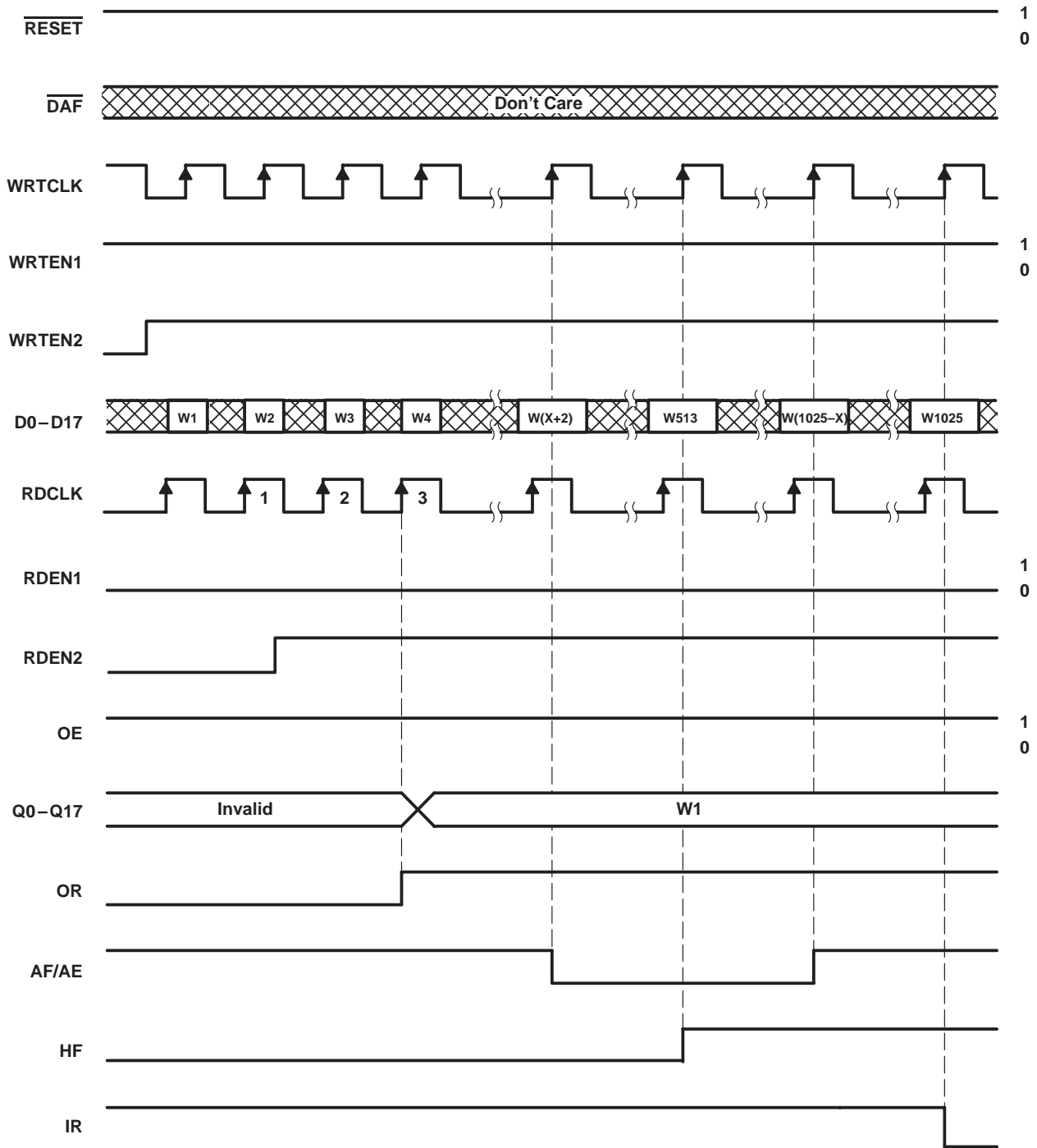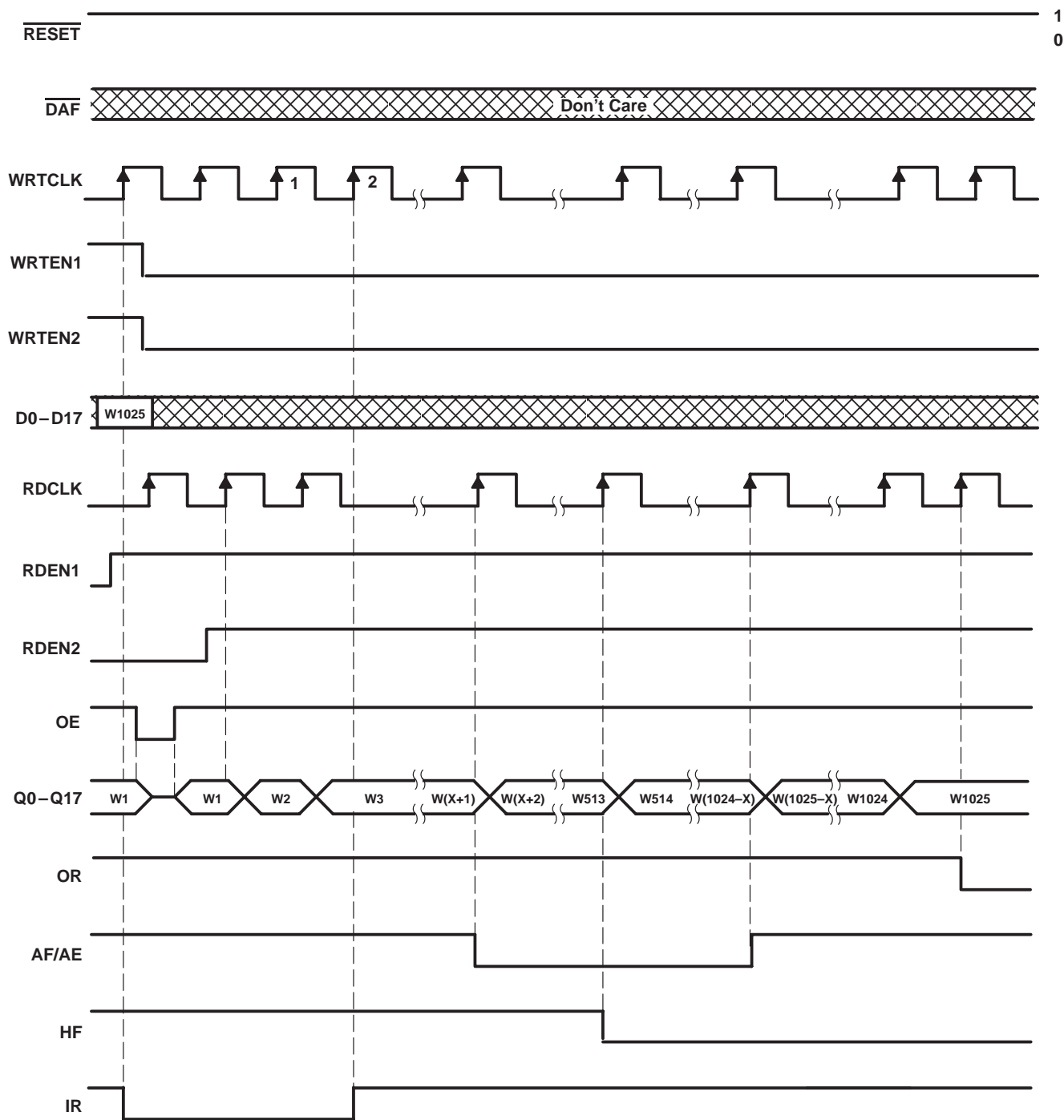
Figure 4. Read Cycle

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . −0.5 V to 7 V
Input voltage, V_I . . . . 7 V
Voltage applied to a disabled 3-state output . . . . 5.5 V
Operating free-air temperature range, T_A . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		−8	mA
I_{OL}	Low-level output current		16	mA
T_A	Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = − 8 mA	2.4			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 16 mA			0.5	V
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or 0 V			±5	µA
I_{OZ}	V_{CC} = 5.5 V,	V_O = V_{CC} or 0 V			±5	µA
I_{CC}§	V_I = V_{CC} − 0.2 V or 0 V				400	µA
	One input at 3.4 V,	Other inputs at V_{CC} or GND			1	mA
C_i	V_I = 0 V, f = 1 MHz			4		pF
C_o	V_O = 0 V, f = 1 MHz			8		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ I_{CC} tested with outputs open

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timing requirements (see Figures 1 through 8)

		'ACT7811-15		'ACT7811-18		'ACT7811-20		'ACT7811-25		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f$_{clock}$	Clock frequency	40		35		28.5		16.7		MHz
t$_w$	Pulse duration									ns
	D0−D17 high or low	10		12		14		20		
	WRTCLK high	7		8.5		10		17		
	WRTCLK low	10		11		14		23		
	RDCLK high	7		8.5		10		17		
	RDCLK low	10		11		14		23		
	$\overline{DAF}$ high	10		10		10		10		
	WRTEN1, WRTEN2 high or low	10		10		10		10		
	OE, RDEN1, RDEN2 high or low	10		10		10		10		
t$_{su}$	Setup time									ns
	D0−D17 before WRTCLK↑	5		5		5		5		
	WRTEN1, WRTEN2 high before WRTCLK↑	5		5		5		5		
	OE, RDEN1, RDEN2 high before RDCLK↑	5		5		5		5		
	Reset: $\overline{RESET}$ low before first WRTCLK and RDCLK↑	7		7		7		7		
	Define AF/AE: D0−D8 before $\overline{DAF}$↓	5		5		5		5		
	Define AF/AE: $\overline{DAF}$↓ before $\overline{RESET}$↑	7		7		7		7		
	Define AF/AE (default): $\overline{DAF}$ high before $\overline{RESET}$↑	5		5		5		5		
t$_h$	Hold time									ns
	D0−D17 after WRTCLK↑	1		1		1		1		
	WRTEN1, WRTEN2 high after WRTCLK↑	1		1		1		1		
	OE, RDEN1, RDEN2 high after RDCLK↑	1		1		1		1		
	Reset: $\overline{RESET}$ low after fourth WRTCLK and RDCLK↑	0		0		0		0		
	Define AF/AE: D0−D8 after $\overline{DAF}$↓	1		1		1		1		
	Define AF/AE: $\overline{DAF}$ low after $\overline{RESET}$↑	0		0		0		0		
	Define AF/AE (default): $\overline{DAF}$ high after $\overline{RESET}$↑	1		1		1		1		

† To permit the clock pulse to be utilized for reset purposes

switching characteristics over recommended operating free-air temperature range (see Figures 9 and 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 0°C to 70°C									UNIT
			'ACT7811-15			'ACT7811-18		'ACT7811-20		'ACT7811-25		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	WRTCLK or RDCLK		40			35		28.5		16.7		MHz
t_{pd}	RDCLK↑	Any Q	4	12	15	4	18	4	20	4	25	ns
t_{pd}†				10.5								
t_{pd}	WRTCLK↑	IR	2		10	2	12	2	14	2	16	ns
t_{pd}	RDCLK↑	OR	2		10	2	12	2	14	2	16	ns
t_{pd}	WRTCLK↑	AF/AE	6		20	6	22	6	24	6	26	ns
	RDCLK↑		6		20	6	22	6	24	6	26	
t_{PLH}	WRTCLK↑	HF	6		19	6	21	6	23	6	25	ns
t_{PHL}	RDCLK↑		6		19	6	21	6	23	6	25	
t_{PLH}	RESET↓	AF/AE	3		19	3	21	3	23	3	25	ns
t_{PHL}		HF	4		21	4	23	4	25	4	27	
t_{en}	OE	Any Q	2		11	2	11	2	11	2	11	ns
t_{dis}			2		14	2	14	2	14	2	14	

† This parameter is measured with C_L = 30 pF (see Figure 5).

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per 1K bits	C_L = 50 pF, f = 5 MHz	65	pF

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TYPICAL CHARACTERISTICS

TYPICAL PROPAGATION DELAY TIME
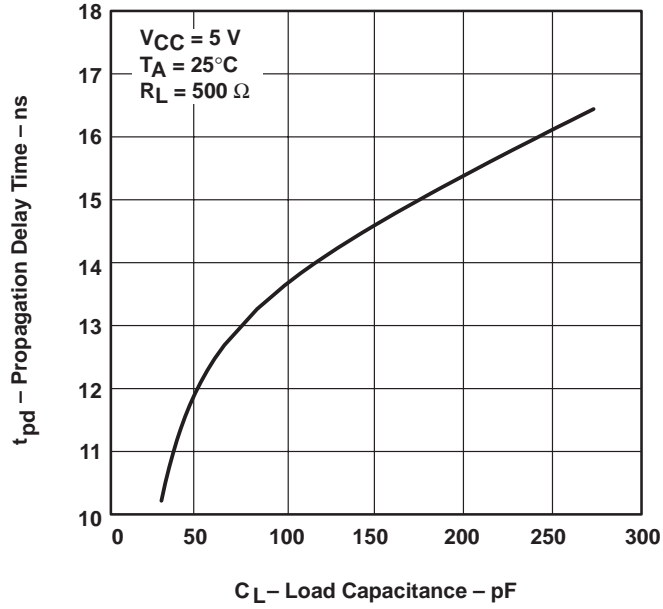**vs**
LOAD CAPACITANCE

Figure 5

TYPICAL CHARACTERISTICS

TYPICAL POWER DISSIPATION CAPACITANCE
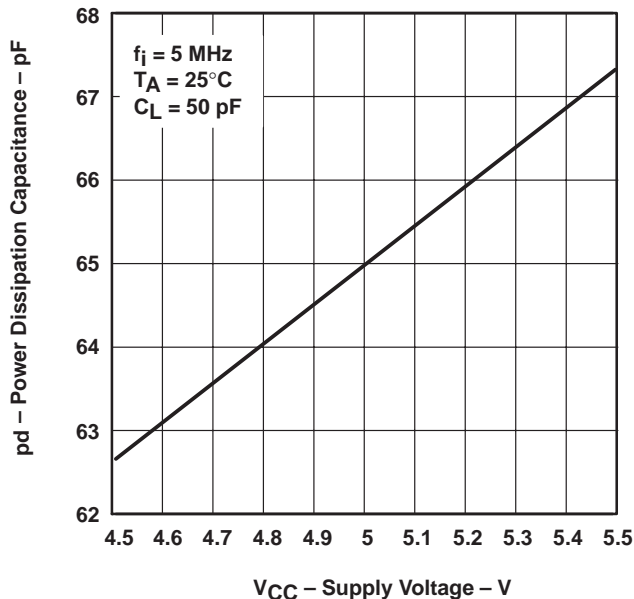**vs**
SUPPLY VOLTAGE

Figure 6

calculating power dissipation

The maximum power dissipation (P_T) of the SN74ACT7811 can be calculated by:

$$P_T = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + \Sigma\,(C_{pd} \times V_{CC}^2 \times f_i) + \Sigma\,(C_L \times V_{CC}^2 \times f_o)$$

where:

I_{CC}	=	power-down I_{CC} maximum
N	=	number of inputs driven by a TTL device
ΔI_{CC}	=	increase in supply current
dc	=	duty cycle of inputs at a TTL high level of 3.4 V
C_{pd}	=	power dissipation capacitance
C_L	=	output capacitive load
f_i	=	data input frequency
f_o	=	data output frequency

APPLICATION INFORMATION

expanding the SN74ACT7811

The SN74ACT7811 is expandable in width and depth. Expanding in word depth offers special timing considerations:

After the first data word is loaded into the FIFO, the word is unloaded and the output-ready flag (OR) output goes high after (N × 3) read-clock (RDCLK) cycles, where N is the number of devices used in depth expansion.

After the FIFO is filled, the input-ready flag (IR) output goes low, the first word is unloaded, and the IR flag output is driven high after (N × 2) write-clock cycles, where N is the number of devices used in depth expansion.
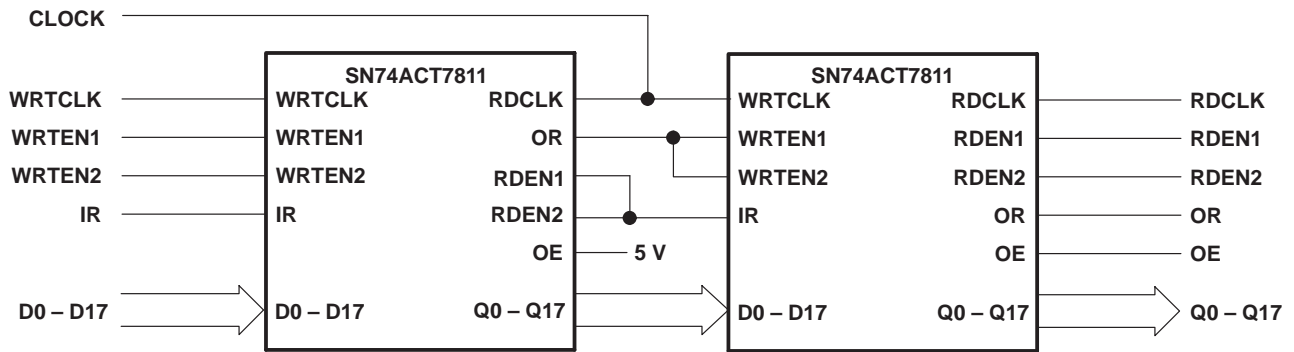

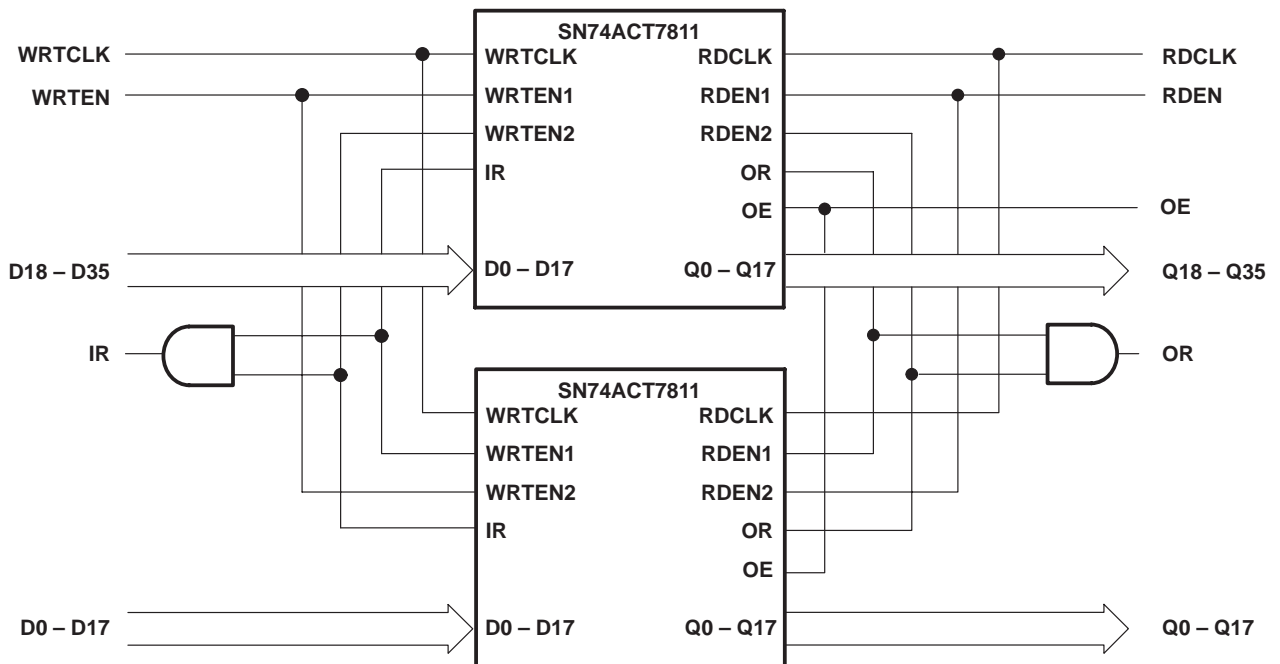Figure 7. Word-Depth Expansion: 2048 Words × 18 Bits, N = 2

Figure 8. Word-Width Expansion: 1024 Words × 36 Bits

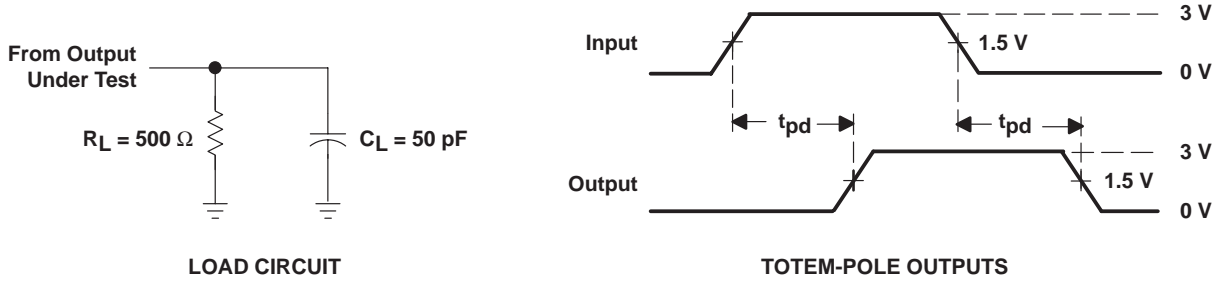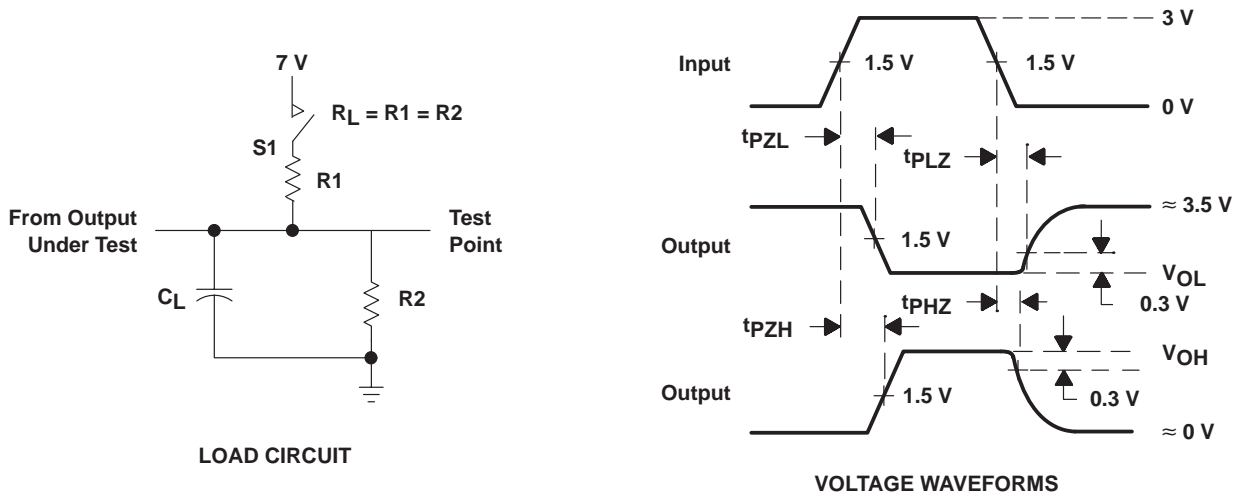## PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT

TOTEM-POLE OUTPUTS

Figure 9. Standard CMOS Outputs

LOAD CIRCUIT

VOLTAGE WAVEFORMS

PARAMETER		R1, R2	C_L†	S1
t_{en}	t_{PZH}	500 Ω	50 pF	Open
	t_{PZL}			Closed
t_{dis}	t_{PHZ}	500 Ω	50 pF	Open
	t_{PLZ}			Closed
t_{pd}		500 Ω	50 pF	Open

† Includes probe and test fixture capacitance

Figure 10. 3-State Outputs (Any Q)

TEXAS
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PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN74ACT7811-15FN	OBSOLETE	PLCC	FN	68		TBD	Call TI	Call TI
SN74ACT7811-15PN	OBSOLETE	LQFP	PN	80		TBD	Call TI	Call TI
SN74ACT7811-18FN	OBSOLETE	PLCC	FN	68		TBD	Call TI	Call TI
SN74ACT7811-18FNR	OBSOLETE	PLCC	FN	68		TBD	Call TI	Call TI
SN74ACT7811-18PN	OBSOLETE	LQFP	PN	80		TBD	Call TI	Call TI
SN74ACT7811-20PN	OBSOLETE	LQFP	PN	80		TBD	Call TI	Call TI
SN74ACT7811-25FN	OBSOLETE	PLCC	FN	68		TBD	Call TI	Call TI
SN74ACT7811-25PN	OBSOLETE	LQFP	PN	80		TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74ACT7811 :

● Military: SN54ACT7811

NOTE: Qualified Version Definitions:

● Military - QML certified for Military and Defense Applications

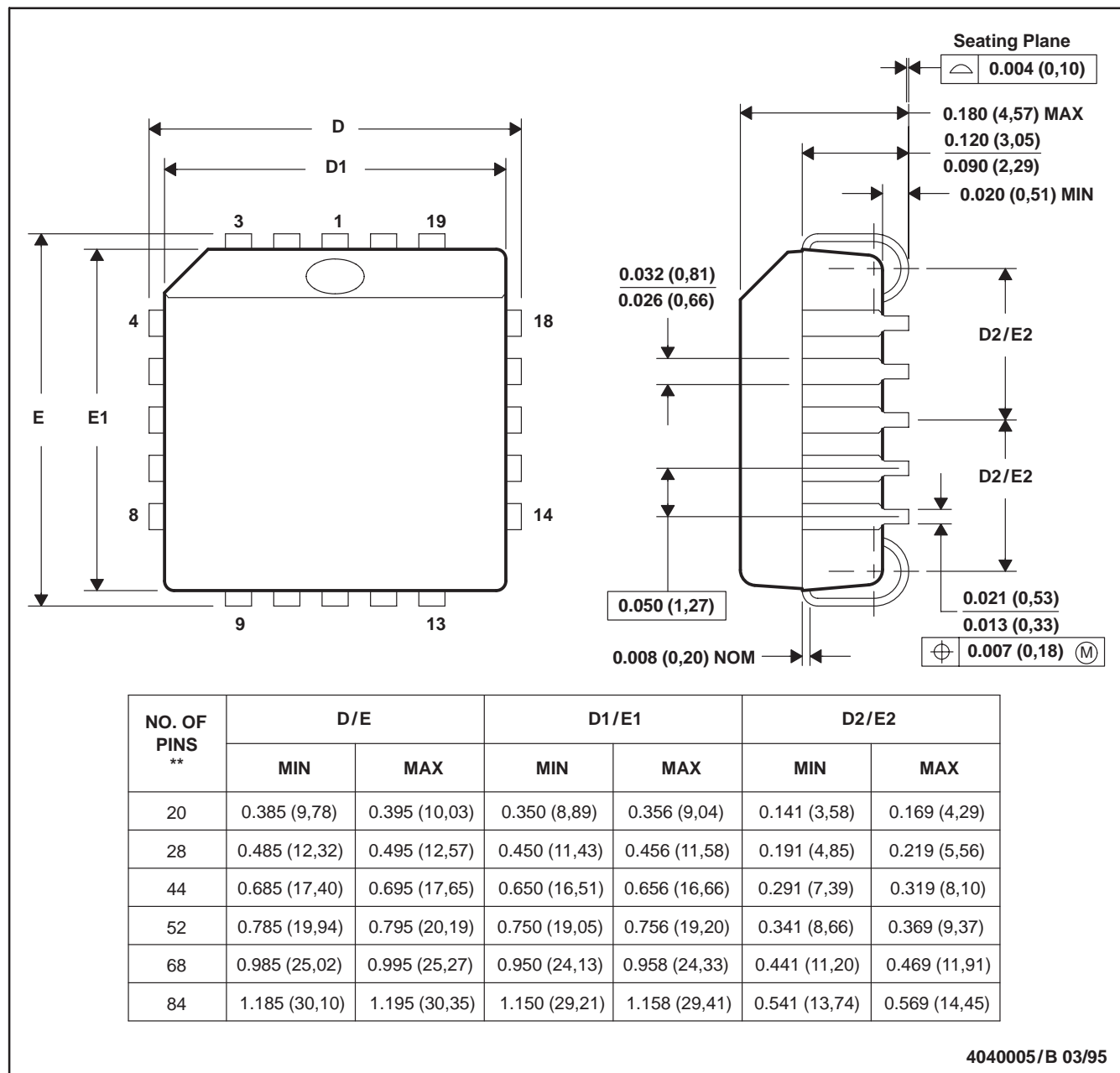**PN (S-PQFP-G80)**   **PLASTIC QUAD FLATPACK**

4040135 / B 11/96

NOTES: A. All linear dimensions are in millimeters.
              B. This drawing is subject to change without notice.
              C. Falls within JEDEC MS-026

TEXAS
INSTRUMENTS

FN (S-PQCC-J**)   **PLASTIC J-LEADED CHIP CARRIER**

20 PIN SHOWN

NO. OF PINS **	D/E		D1/E1		D2/E2	
	MIN	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

4040005/B 03/95

NOTES: A. All linear dimensions are in inches (millimeters).
           B. This drawing is subject to change without notice.
           C. Falls within JEDEC MS-018

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