Dual, 8-Bit, 60Msps, 3V, Low-Power ADC with Internal Reference and Parallel Outputs

ABSOLUTE MAXIMUM RATINGS

V_{DD}, OV_{DD} to GND ....-0.3V to +3.6V
OGND to GND...-0.3V to +0.3V
INA+, INA-, INB+, INB- to GND ....-0.3V to V_{DD}
REFIN, REFOUT, REFP, REFN,
COM, CLK to GND ....-0.3V to (V_{DD} + 0.3V)
$\overline{OE}$, PD, SLEEP, T/B, D7A–D0A,
D7B–D0B to OGND ....-0.3V to (OV_{DD} + 0.3V)

Continuous Power Dissipation (T_A = +70°C)
48-Pin TQFP (derate 12.5mW/°C above +70°C).........1000mW
Operating Temperature Range ....-40°C to +85°C
Junction Temperature..+150°C
Storage Temperature Range ....-60°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = OV_{DD} = 3V, 0.1µF and 2.2µF capacitors from REFP, REFN, and COM to GND; REFOUT connected to REFIN through a 10kΩ resistor, V_{IN} = $2V_{P-P}$ (differential with respect to COM), C_L = 10pF at digital outputs, f_{CLK} = 60MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. ≥ +25°C guaranteed by production test, < +25°C guaranteed by design and characterization. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Resolution			8			Bits
Integral Nonlinearity	INL	f_{IN} = 7.5MHz (Note 1)		±0.3	±1	LSB
Differential Nonlinearity	DNL	f_{IN} = 7.5MHz, no missing codes guaranteed (Note 1)		±0.2	±1	LSB
Offset Error					±4	%FS
Gain Error					±4	%FS
Gain Temperature Coefficient				±100		ppm/°C
ANALOG INPUT						
Differential Input Voltage Range	V_{DIFF}	Differential or single-ended inputs		±1.0		V
Common-Mode Input Voltage Range	V_{CM}			V_{DD} / 2 ±0.2		V
Input Resistance	R_{IN}	Switched capacitor load		95		kΩ
Input Capacitance	C_{IN}			5		pF
CONVERSION RATE						
Maximum Clock Frequency	f_{CLK}		60			MHz
Data Latency				5		Clock Cycles
DYNAMIC CHARACTERISTICS (f_{CLK} = 60MHz, 4096-point FFT)						
Signal-to-Noise Ratio	SNR	$f_{INA\ or\ B}$ = 7.5MHz at -1dB FS		48.7		dB
		$f_{INA\ or\ B}$ = 20MHz at -1dB FS	47	48.7		
		$f_{INA\ or\ B}$ = 30MHz at -1dB FS		48.6		
		$f_{INA\ or\ B}$ = 115.1MHz at -1dB FS		48.3		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = OV_{DD} = 3V, 0.1µF and 2.2µF capacitors from REFP, REFN, and COM to GND; REFOUT connected to REFIN through a 10kΩ resistor, V_{IN} = $2V_{P-P}$ (differential with respect to COM), C_L = 10pF at digital outputs, f_{CLK} = 60MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. ≥ +25°C guaranteed by production test, < +25°C guaranteed by design and characterization. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Signal-to-Noise and Distortion	SINAD	$f_{INA\ or\ B}$ = 7.5MHz at -1dB FS		48.6		dB
		$f_{INA\ or\ B}$ = 20MHz at -1dB FS	46.5	48.6		
		$f_{INA\ or\ B}$ = 30MHz at -1dB FS		48.5		
		$f_{INA\ or\ B}$ = 115.1MHz at -1dB FS		48.2		
Spurious-Free Dynamic Range	SFDR	$f_{INA\ or\ B}$ = 7.5MHz at -1dB FS		71		dBc
		$f_{INA\ or\ B}$ = 20MHz at -1dB FS	60	69		
		$f_{INA\ or\ B}$ = 30MHz at -1dB FS		69		
		$f_{INA\ or\ B}$ = 115.1MHz at -1dB FS		68		
Third-Harmonic Distortion	HD3	$f_{INA\ or\ B}$ = 7.5MHz at -1dB FS		-75		dBc
		$f_{INA\ or\ B}$ = 20MHz at -1dB FS		-72		
		$f_{INA\ or\ B}$ = 30MHz at -1dB FS		-72		
		$f_{INA\ or\ B}$ = 115.1MHz at -1dB FS		-68		
Intermodulation Distortion (First Five Odd-Order IMDs)	IMD	$f_{IN1(A\ or\ B)}$ = 1.985MHz at -7dB FS $f_{IN2(A\ or\ B)}$ = 2.029MHz at -7dB FS (Note 2)		-70		dBc
Third-Order Intermodulation Distortion	IM3	$f_{IN1(A\ or\ B)}$ = 1.985MHz at -7dB FS $f_{IN2(A\ or\ B)}$ = 2.029MHz at -7dB FS (Note 2)		-71.8		dBc
Total Harmonic Distortion (First Four Harmonics)	THD	$f_{INA\ or\ B}$ = 7.5MHz at -1dB FS		-69		dBc
		$f_{INA\ or\ B}$ = 20MHz at -1dB FS		-67	-57	
		$f_{INA\ or\ B}$ = 30MHz at -1dB FS		-67		
		$f_{INA\ or\ B}$ = 115.1MHz at -1dB FS		-65		
Small-Signal Bandwidth		Input at -20dB FS, differential inputs		500		MHz
Full-Power Bandwidth	FPBW	Input at -1dB FS, differential inputs		400		MHz
Gain Flatness (12MHz Spacing)		$f_{IN1(A\ or\ B)}$ = 106 MHz at -1dB FS $f_{IN2(A\ or\ B)}$ = 118 MHz at -1dB FS (Note 3)		0.05		dB
Aperture Delay	t_{AD}			1		ns
Aperture Jitter	t_{AJ}	1dB SNR degradation at Nyquist		2		ps_{RMS}
Overdrive Recovery Time		For 1.5 × full-scale input		2		ns
INTERNAL REFERENCE (REFIN = REFOUT through 10kΩ resistor; REFP, REFN, and COM levels are generated internally.)						
Reference Output Voltage	V_{REFOUT}	(Note 4)		2.048 ±3%		V
Positive Reference Output Voltage	V_{REFP}	(Note 5)		2.012		V
Negative Reference Output Voltage	V_{REFN}	(Note 5)		0.988		V
Common-Mode Level	V_{COM}	(Note 5)		V_{DD} / 2 ±0.1		V

Dual, 8-Bit, 60Msps, 3V, Low-Power ADC with Internal Reference and Parallel Outputs

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = OV_{DD} = 3V, 0.1μF and 2.2μF capacitors from REFP, REFN, and COM to GND; REFOUT connected to REFIN through a 10kΩ resistor, V_{IN} = $2V_{P-P}$ (differential with respect to COM), C_L = 10pF at digital outputs, f_{CLK} = 60MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. ≥ +25°C guaranteed by production test, < +25°C guaranteed by design and characterization. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Reference Output Voltage Range	ΔV_{REF}	$\Delta V_{REF} = V_{REFP} - V_{REFN}$		1.024 ±3%		V
Reference Temperature Coefficient	TC_{REF}			±100		ppm/°C
BUFFERED EXTERNAL REFERENCE (V_{REFIN} = 2.048V)						
Positive Reference Output Voltage	V_{REFP}	(Note 5)		2.012		V
Negative Reference Output Voltage	V_{REFN}	(Note 5)		0.988		V
Common-Mode Level	V_{COM}	(Note 5)		V_{DD} / 2 ±0.1		V
Differential Reference Output Voltage Range	ΔV_{REF}	$\Delta V_{REF} = V_{REFP} - V_{REFN}$		1.024 ±2%		V
REFIN Resistance	R_{REFIN}			750		MΩ
Maximum REFP, COM Source Current	I_{SOURCE}			5		mA
Maximum REFP, COM Sink Current	I_{SINK}			-250		μA
Maximum REFN Source Current	I_{SOURCE}			250		μA
Maximum REFN Sink Current	I_{SINK}			-5		mA
UNBUFFERED EXTERNAL REFERENCE (V_{REFIN} = AGND, reference voltage applied to REFP, REFN, and COM)						
REFP, REFN Input Resistance	R_{REFP}, R_{REFN}	Measured between REFP, COM, REFN, and COM		4		kΩ
REFP, REFN, COM Input Capacitance	C_{IN}			15		pF
Differential Reference Input Voltage Range	ΔV_{REF}	$\Delta V_{REF} = V_{REFP} - V_{REFN}$		1.024 ±10%		V
COM Input Voltage Range	V_{COM}			V_{DD} / 2 ±5%		V
REFP Input Voltage	V_{REFP}			V_{COM} + ΔV_{REF} / 2		V
REFN Input Voltage	V_{REFN}			V_{COM} - ΔV_{REF} / 2		V
DIGITAL INPUTS (CLK, PD, $\overline{OE}$, SLEEP, T/B)						
Input High Threshold	V_{IH}	CLK	0.8 × V_{DD}			V
		PD, $\overline{OE}$, SLEEP, T/B	0.8 × OV_{DD}			

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = OV_{DD} = 3V, 0.1µF and 2.2µF capacitors from REFP, REFN, and COM to GND; REFOUT connected to REFIN through a 10kΩ resistor, V_{IN} = $2V_{P-P}$ (differential with respect to COM), C_L = 10pF at digital outputs, f_{CLK} = 60MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. ≥ +25°C guaranteed by production test, < +25°C guaranteed by design and characterization. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Threshold	V_{IL}	CLK			0.2 × V_{DD}	V
		PD, $\overline{OE}$, SLEEP, T/B			0.2 × OV_{DD}	
Input Hysteresis	V_{HYST}			0.15		V
Input Leakage	I_{IH}	V_{IH} = V_{DD} = OV_{DD}			±20	µA
	I_{IL}	V_{IL} = 0			±20	
Input Capacitance	C_{IN}			5		pF
DIGITAL OUTPUTS (D7A–D0A, D7B–D0B)						
Output Voltage Low	V_{OL}	I_{SINK} = -200µA			0.2	V
Output Voltage High	V_{OH}	I_{SOURCE} = 200µA	OV_{DD} - 0.2			V
Three-State Leakage Current	I_{LEAK}	$\overline{OE}$ = OV_{DD}			±10	µA
Three-State Output Capacitance	C_{OUT}	$\overline{OE}$ = OV_{DD}		5		pF
POWER REQUIREMENTS						
Analog Supply Voltage Range	V_{DD}		2.7	3	3.6	V
Output Supply Voltage Range	OV_{DD}	C_L = 15pF	1.7	3	3.6	V
Analog Supply Current	I_{VDD}	Operating, $f_{INA\ \&\ B}$ = 20MHz at -1dB FS applied to both channels		40	50	mA
		Sleep mode		3		
		Shutdown, clock idle, PD = $\overline{OE}$ = OV_{DD}		0.1	20	µA
Output Supply Current	I_{OVDD}	Operating, $f_{INA\ \&\ B}$ = 20MHz at -1dB FS applied to both channels (Note 6)		9		mA
		Sleep mode		3		µA
		Shutdown, clock idle, PD = $\overline{OE}$ = OV_{DD}		3	10	
Analog Power Dissipation	PDISS	Operating, $f_{INA\ \&\ B}$ = 20MHz at -1dB FS applied to both channels		120	150	mW
		Sleep mode		9		
		Shutdown, clock idle, PD = $\overline{OE}$ = OV_{DD}		0.3	60	µW
Power-Supply Rejection	PSRR	Offset, V_{DD} ±5%		±3		mV/V
		Gain, V_{DD} ±5%		±3		
TIMING CHARACTERISTICS						
CLK Rise to Output Data Valid Time	t_{DO}	C_L = 20pF (Notes 1, 7)		6	9	ns
$\overline{OE}$ Fall to Output Enable Time	t_{ENABLE}			5		ns
$\overline{OE}$ Rise to Output Disable Time	$t_{DISABLE}$			5		ns
CLK Pulse Width High	t_{CH}	Clock period: 16.67ns (Note 7)		8.33 ±1.5		ns
CLK Pulse Width Low	t_{CL}	Clock period: 16.67ns (Note 7)		8.33 ±1.5		ns

Dual, 8-Bit, 60Msps, 3V, Low-Power ADC with Internal Reference and Parallel Outputs

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = OV_{DD} = 3V, 0.1µF and 2.2µF capacitors from REFP, REFN, and COM to GND; REFOUT connected to REFIN through a 10kΩ resistor, V_{IN} = $2V_{P-P}$ (differential with respect to COM), C_L = 10pF at digital outputs, f_{CLK} = 60MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. ≥ +25°C guaranteed by production test, < +25°C guaranteed by design and characterization. Typical values are at T_A = +25°C.)

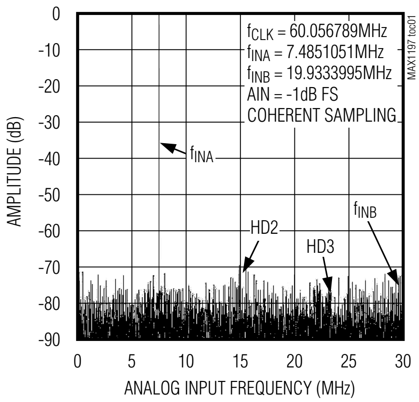
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Wake-Up Time	t_{WAKE}	Wake up from sleep mode		1		µs
		Wake up from shutdown mode (Note 11)		20		
CHANNEL-TO-CHANNEL MATCHING						
Crosstalk		$f_{INA\ or\ B}$ = 20MHz at -1dB FS (Note 8)		-72		dB
Gain Matching		$f_{INA\ or\ B}$ = 20MHz at -1dB FS (Note 9)		0.05		dB
Phase Matching		$f_{INA\ or\ B}$ = 20MHz at -1dB FS (Note 10)		±0.05		Degrees

Note 1: Guaranteed by design. Not subject to production testing.
Note 2: Intermodulation distortion is the total power of the intermodulation products relative to the total input power.
Note 3: Analog attenuation is defined as the amount of attenuation of the fundamental bin from a converted FFT between two applied input signals with the same magnitude (peak-to-peak) at f_{IN1} and f_{IN2}.
Note 4: REFIN and REFOUT should be bypassed to GND with a 0.1µF (min) and 2.2µF (typ) capacitor.
Note 5: REFP, REFN, and COM should be bypassed to GND with a 0.1µF (min) and 2.2µF (typ) capacitor.
Note 6: Typical analog output current at $f_{INA\&B}$ = 20MHz. For digital output currents vs. analog input frequency, see *Typical Operating Characteristics*.
Note 7: See Figure 3 for detailed system timing diagrams. Clock to data valid timing is measured from 50% of the clock level to 50% of the data output level.
Note 8: Crosstalk rejection is tested by applying a test tone to one channel and holding the other channel at DC level. Crosstalk is measured by calculating the power ratio of the fundamental of each channel's FFT.
Note 9: Amplitude matching is measured by applying the same signal to each channel and comparing the magnitude of the fundamental of the calculated FFT.
Note 10: Phase matching is measured by applying the same signal to each channel and comparing the phase of the fundamental of the calculated FFT. The data from both ADC channels must be captured simultaneously during this test.
Note 11: SINAD settles to within 0.5dB of its typical value in unbuffered external reference mode.

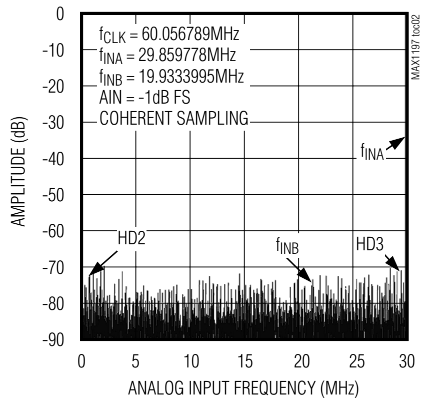
Typical Operating Characteristics

(V_{DD} = 3V, OV_{DD} = 3V, V_{REFIN} = 2.048V, differential input at -1dB FS, f_{CLK} = 40MHz, C_L ≈ 10pF T_A = +25°C, unless otherwise noted.)

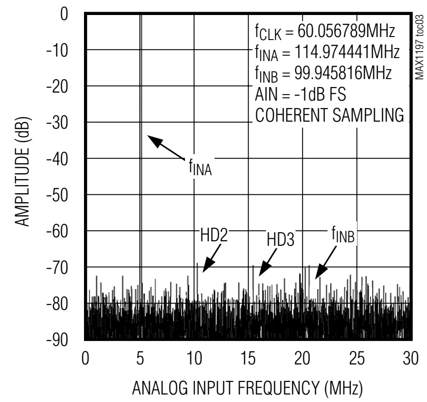
FFT PLOT CHA (DIFFERENTIAL INPUT, 8192-POINT DATA RECORD)



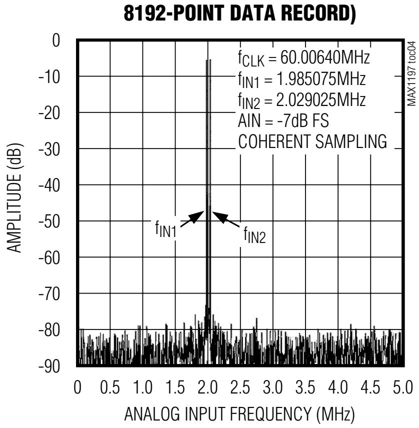
FFT PLOT CHA (DIFFERENTIAL INPUT, 8192-POINT DATA RECORD)



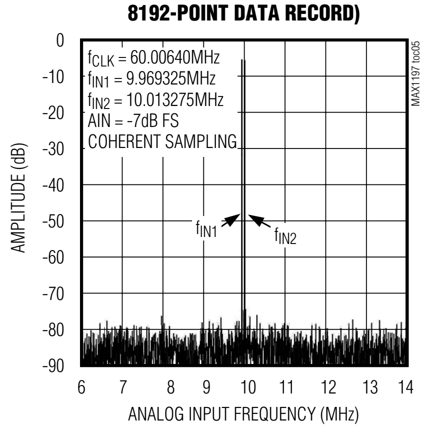
FFT PLOT CHA (DIFFERENTIAL INPUT, 8192-POINT DATA RECORD)



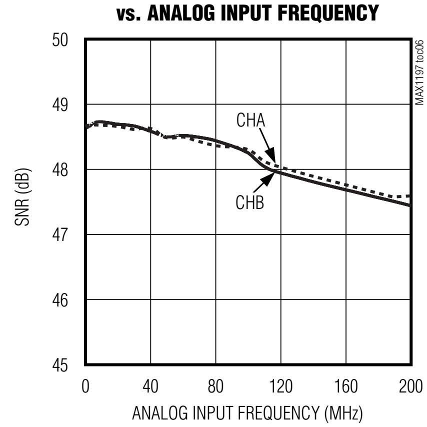
TWO-TONE IMD PLOT (DIFFERENTIAL INPUT, 8192-POINT DATA RECORD)



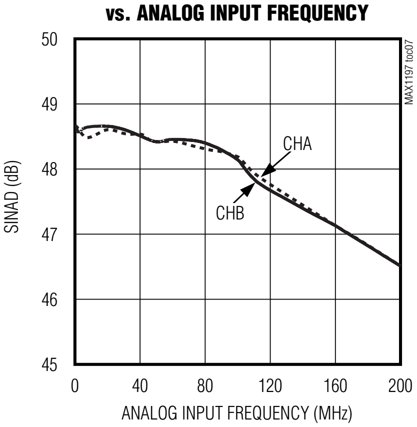
TWO-TONE IMD PLOT (DIFFERENTIAL INPUT, 8192-POINT DATA RECORD)



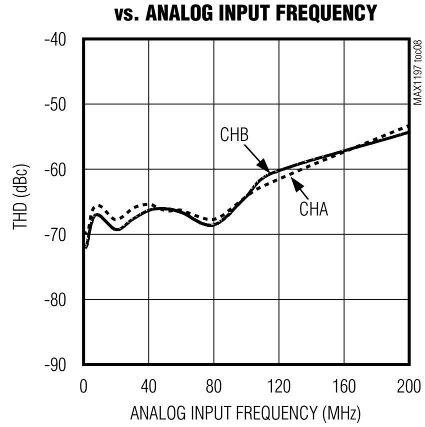
SIGNAL-TO-NOISE RATIO vs. ANALOG INPUT FREQUENCY



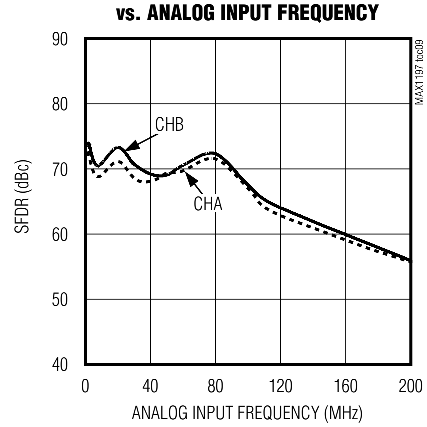
SIGNAL-TO-NOISE + DISTORTION vs. ANALOG INPUT FREQUENCY



TOTAL HARMONIC DISTORTION vs. ANALOG INPUT FREQUENCY



SPURIOUS-FREE DYNAMIC RANGE vs. ANALOG INPUT FREQUENCY

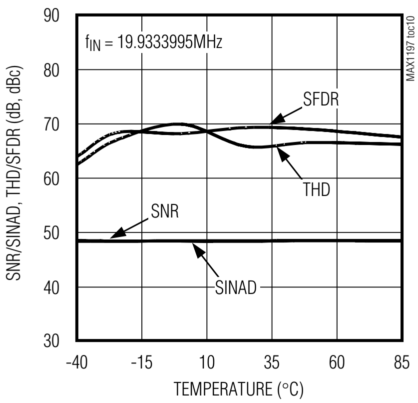


Dual, 8-Bit, 60Msps, 3V, Low-Power ADC with Internal Reference and Parallel Outputs

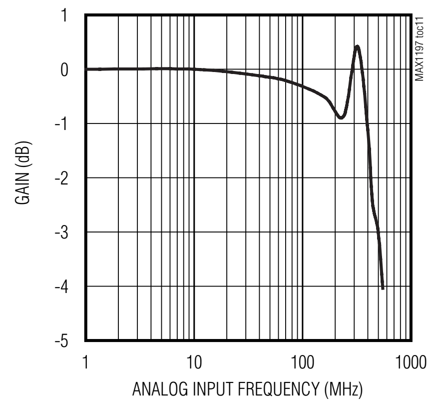
Typical Operating Characteristics (continued)

(V_{DD} = 3V, OV_{DD} = 3V, V_{REFIN} = 2.048V, differential input at -1dB FS, f_{CLK} = 40MHz, $C_L \approx$ 10pF T_A = +25°C, unless otherwise noted.)

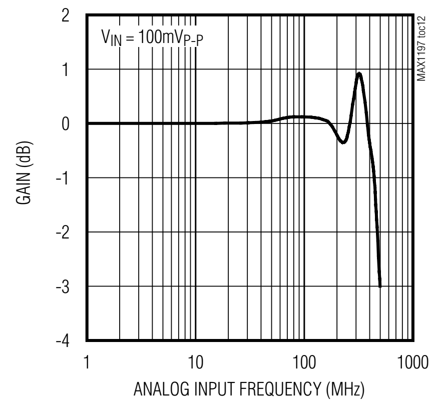
SNR/SINAD, THD/SFDR vs. TEMPERATURE



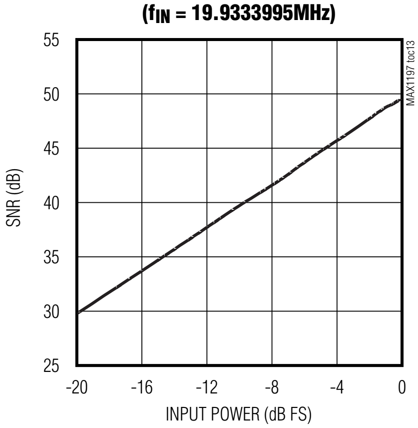
FULL-POWER INPUT BANDWIDTH vs. ANALOG INPUT FREQUENCY



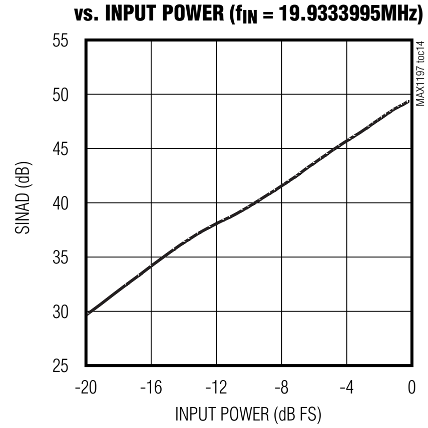
SMALL-SIGNAL INPUT BANDWIDTH vs. ANALOG INPUT FREQUENCY



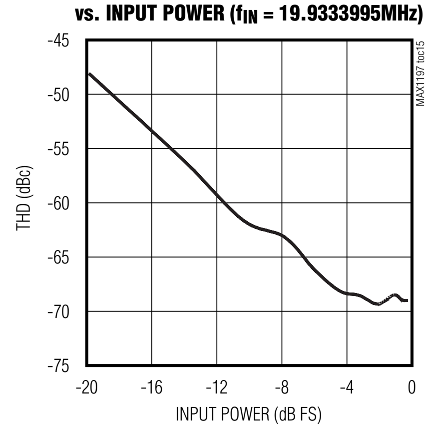
SIGNAL-TO-NOISE RATIO vs. INPUT POWER (f_{IN} = 19.9333995MHz)



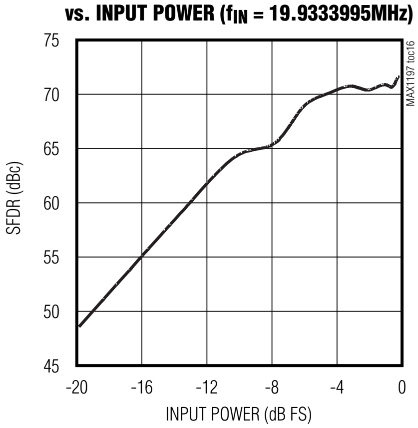
SIGNAL-TO-NOISE + DISTORTION vs. INPUT POWER (f_{IN} = 19.9333995MHz)



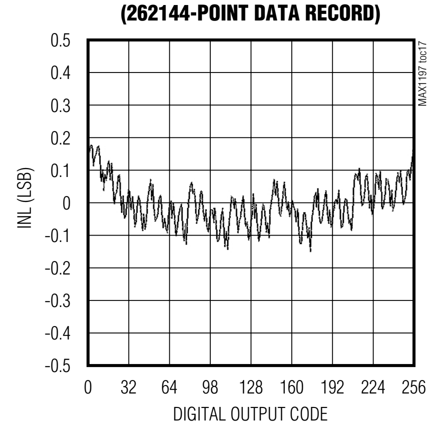
TOTAL HARMONIC DISTORTION vs. INPUT POWER (f_{IN} = 19.9333995MHz)



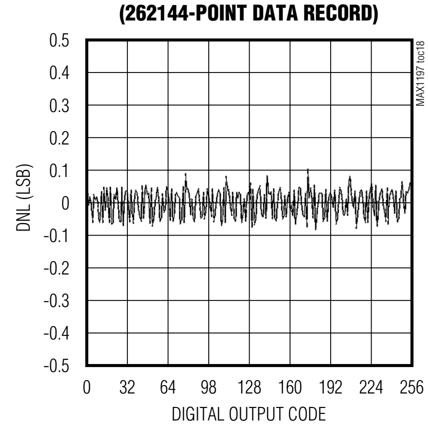
SPURIOUS-FREE DYNAMIC RANGE vs. INPUT POWER (f_{IN} = 19.9333995MHz)



INTEGRAL NONLINEARITY (262144-POINT DATA RECORD)



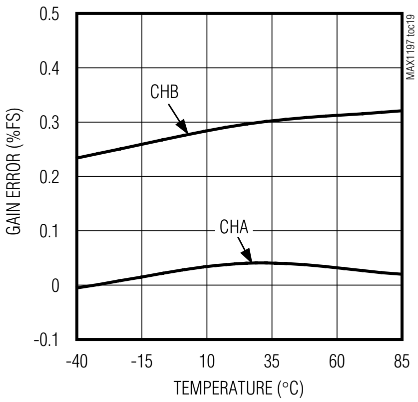
DIFFERENTIAL NONLINEARITY (262144-POINT DATA RECORD)



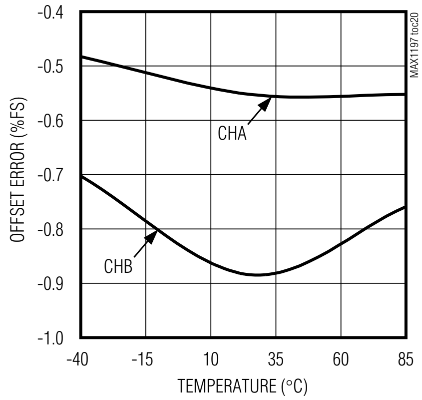
Typical Operating Characteristics (continued)

(V_{DD} = 3V, OV_{DD} = 3V, V_{REFIN} = 2.048V, differential input at -1dB FS, f_{CLK} = 40MHz, C_L ≈ 10pF T_A = +25°C, unless otherwise noted.)

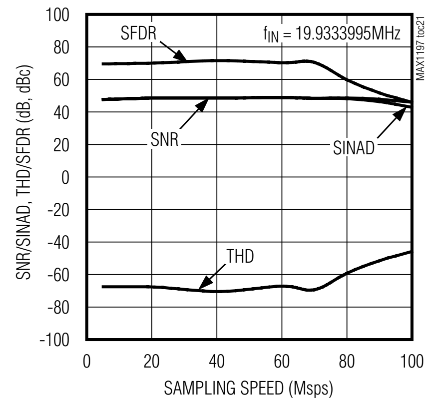
GAIN ERROR vs. TEMPERATURE, EXTERNAL REFERENCE V_{REFIN} = 2.048V



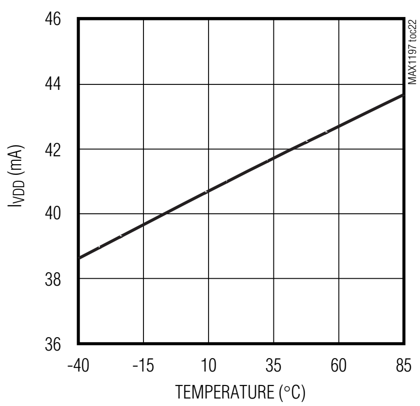
OFFSET ERROR vs. TEMPERATURE, EXTERNAL REFERENCE V_{REFIN} = 2.048V



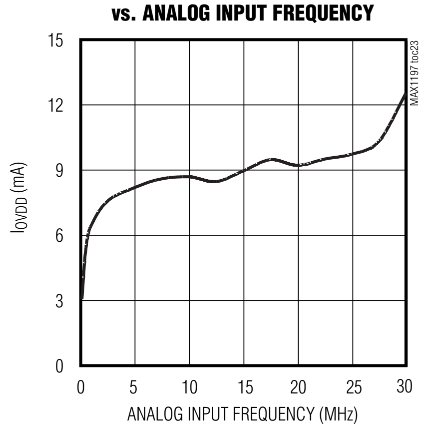
SNR/SINAD, THD/SFDR vs. SAMPLING SPEED



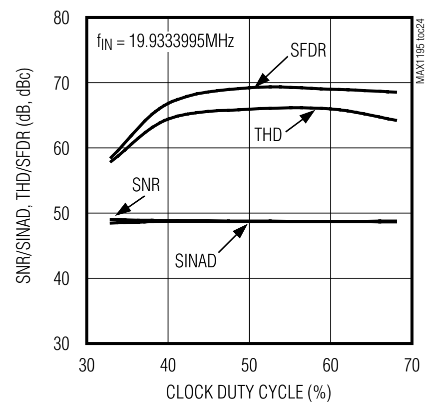
ANALOG SUPPLY CURRENT vs. TEMPERATURE



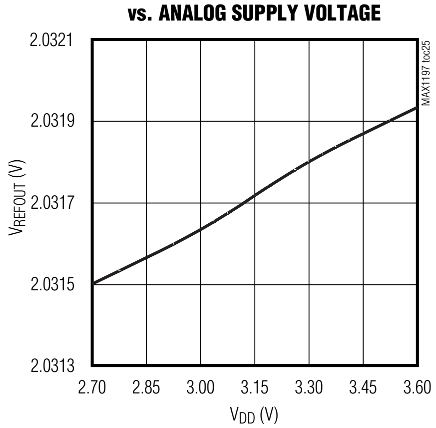
DIGITAL SUPPLY CURRENT vs. ANALOG INPUT FREQUENCY



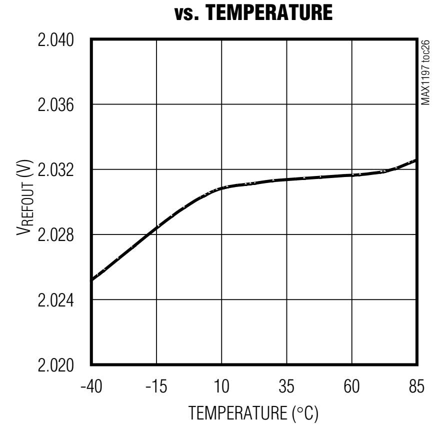
SNR/SINAD, THD/SFDR vs. CLOCK DUTY CYCLE



INTERNAL REFERENCE VOLTAGE vs. ANALOG SUPPLY VOLTAGE



INTERNAL REFERENCE VOLTAGE vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1	COM	Common-Mode Voltage I/O. Bypass to GND with a ≥ 0.1µF capacitor.
2, 6, 11, 14, 15	V_{DD}	Analog Supply Voltage. Bypass to GND with a capacitor combination of 2.2µF in parallel with 0.1µF.
3, 7, 10, 13, 16	GND	Analog Ground
4	INA+	Channel A Positive Analog Input. For single-ended operation connect signal source to INA+.
5	INA-	Channel A Negative Analog Input. For single-ended operation connect INA- to COM.
8	INB-	Channel B Negative Analog Input. For single-ended operation connect INB- to COM.
9	INB+	Channel B Positive Analog Input. For single-ended operation connect signal source to INB+.
12	CLK	Converter Clock Input
17	T/B	T/B Selects the ADC Digital Output Format High: Two's complement Low: Straight offset binary
18	SLEEP	Sleep Mode Input High: Disables both quantizers, but leaves the reference bias circuit active Low: Normal operation
19	PD	High-Active Power Down Input High: Power-down mode Low: Normal operation
20	$\overline{OE}$	Low-Active Output Enable Input High: Digital outputs disabled Low: Digital outputs enabled
21	D7B	Three-State Digital Output, Bit 7 (MSB), Channel B
22	D6B	Three-State Digital Output, Bit 6, Channel B
23	D5B	Three-State Digital Output, Bit 5, Channel B
24	D4B	Three-State Digital Output, Bit 4, Channel B
25	D3B	Three-State Digital Output, Bit 3, Channel B
26	D2B	Three-State Digital Output, Bit 2, Channel B
27	D1B	Three-State Digital Output, Bit 1, Channel B
28	D0B	Three-State Digital Output, Bit 0, Channel B
29, 30, 35, 36	N.C.	No Connect
31, 34	OGND	Output Driver Ground
32, 33	OV_{DD}	Output Driver Supply Voltage. Bypass to OGND with a capacitor combination of 2.2µF in parallel with 0.1µF.
37	D0A	Three-State Digital Output, Bit 0, Channel A
38	D1A	Three-State Digital Output, Bit 1, Channel A
39	D2A	Three-State Digital Output, Bit 2, Channel A
40	D3A	Three-State Digital Output, Bit 3, Channel A
41	D4A	Three-State Digital Output, Bit 4, Channel A

Pin Description (continued)

PIN	NAME	FUNCTION
42	D5A	Three-State Digital Output, Bit 5, Channel A
43	D6A	Three-State Digital Output, Bit 6, Channel A
44	D7A	Three-State Digital Output, Bit 7 (MSB), Channel A
45	REFOUT	Internal Reference Voltage Output. May be connected to REFIN through a resistor or a resistor divider.
46	REFIN	Reference Input. $V_{REFIN} = 2 \times (V_{REFP} - V_{REFN})$. Bypass to GND with a > 0.1µF capacitor.
47	REFP	Positive Reference I/O. Conversion range is $\pm(V_{REFP} - V_{REFN})$. Bypass to GND with a > 0.1µF capacitor.
48	REFN	Negative Reference I/O. Conversion range is $\pm(V_{REFP} - V_{REFN})$. Bypass to GND with a > 0.1µF capacitor.

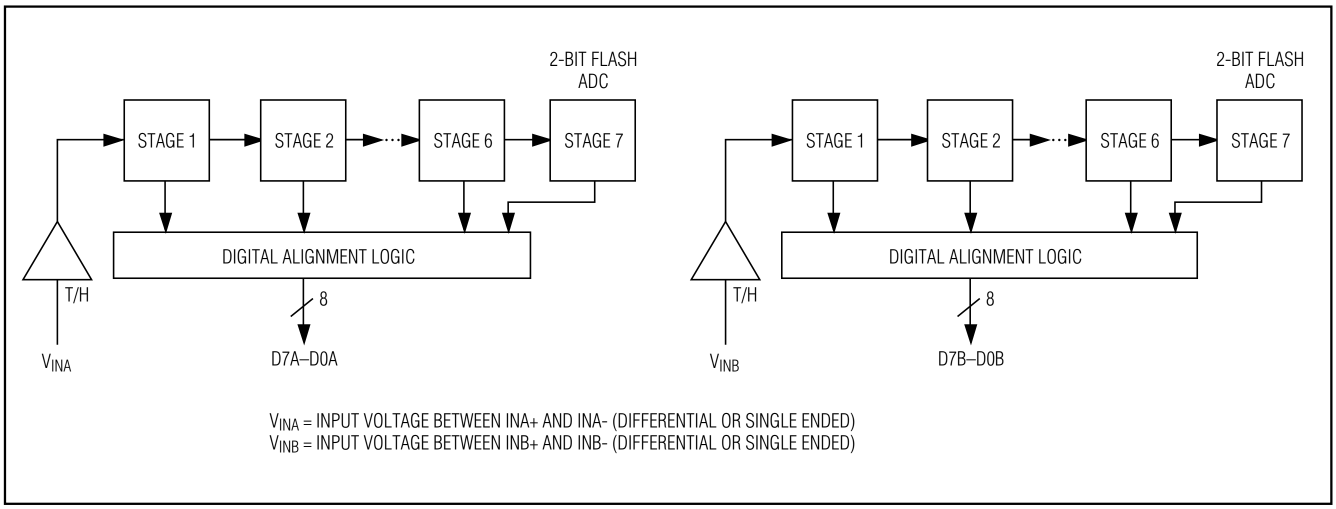


Figure 1. Pipelined Architecture—Stage Blocks

Detailed Description

The MAX1197 uses a seven-stage, fully differential, pipelined architecture (Figure 1) that allows for high-speed conversion while minimizing power consumption. Samples taken at the inputs move progressively through the pipeline stages every half-clock cycle. Including the delay through the output latch, the total clock-cycle latency is five clock cycles.

Flash ADCs convert the held input voltages into a digital code. Internal MDACs convert the digitized results back into analog voltages, which are then subtracted from the original held input signals. The resulting error signals are then multiplied by two, and the residues are passed along to the next pipeline stages where the process is repeated until the signals have been processed by all seven stages.

Input Track-and-Hold Circuits

Figure 2 displays a simplified functional diagram of the input T/H circuits in both track and hold mode. In track mode, switches S1, S2a, S2b, S4a, S4b, S5a, and S5b

Dual, 8-Bit, 60Msps, 3V, Low-Power ADC with Internal Reference and Parallel Outputs

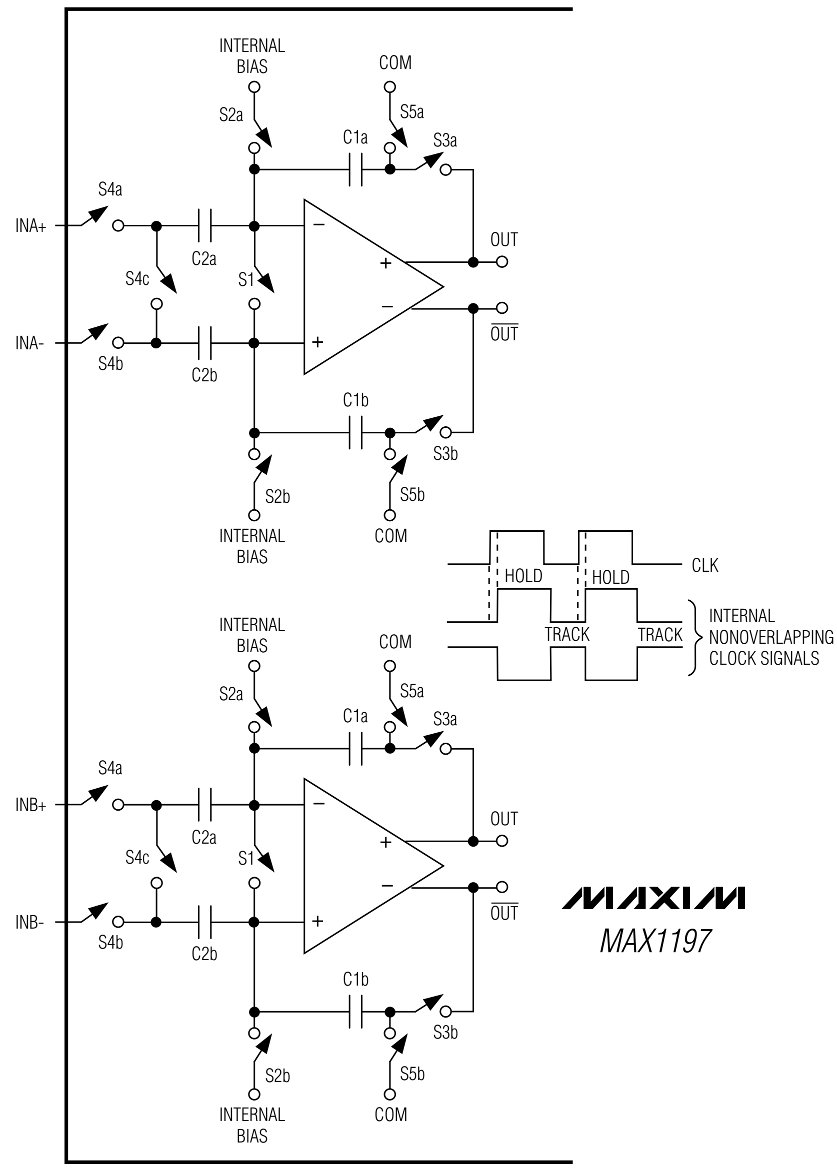


Figure 2. MAX1197 T/H Amplifiers

are closed. The fully differential circuits sample the input signals onto the two capacitors (C2a and C2b) through switches S4a and S4b. S2a and S2b set the common mode for the amplifier input, and open simultaneously with S1 sampling the input waveform. Switches S4a, S4b, S5a, and S5b are then opened before switches S3a and S3b connects capacitors C1a and C1b to the output of the amplifier and switch S4c is closed. The resulting differential voltages are held on capacitors C2a and C2b. The amplifiers are used to charge capacitors C1a and C1b to the same values originally held on C2a and C2b. These values are then presented to the first-stage quantizers and isolate the pipelines from the fast-changing inputs. The wide input bandwidth T/H amplifiers allow the MAX1197 to track and sample/hold analog inputs of high frequencies (>Nyquist). Both ADC inputs (INA+, INB+ and INA-, INB-) can be driven either differentially or single-ended.

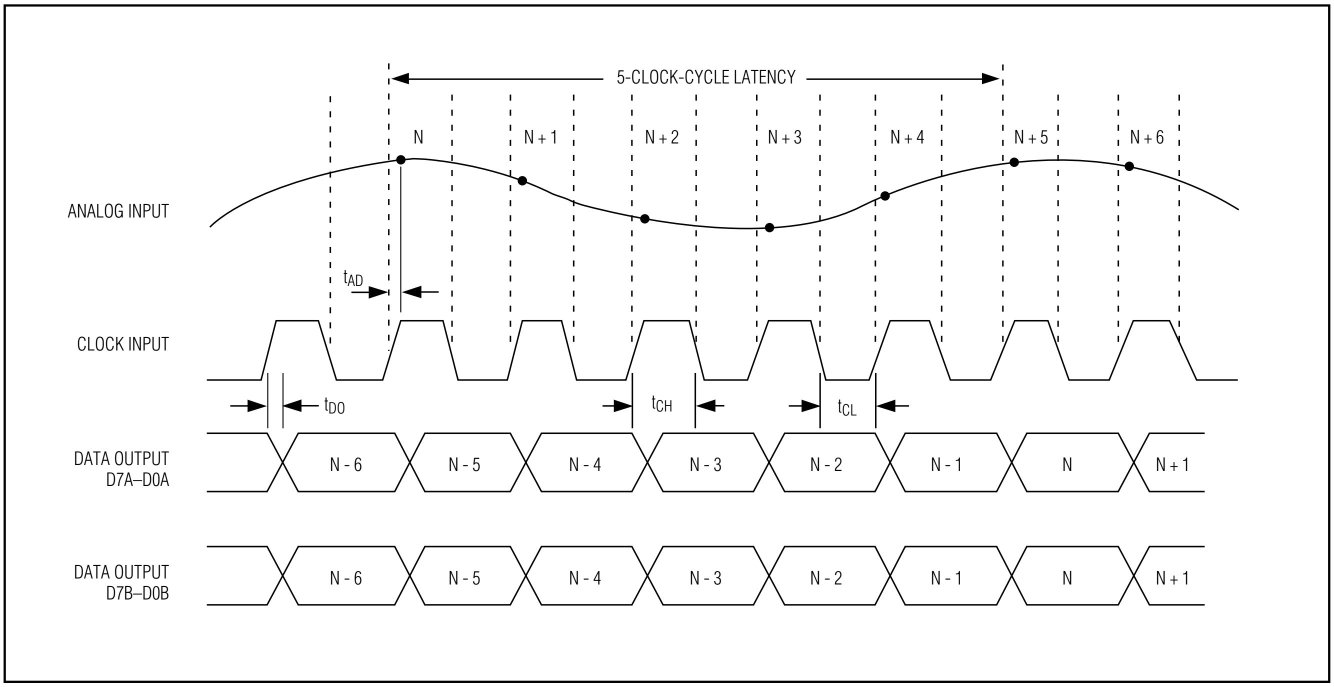


Figure 3. System Timing Diagram

Match the impedance of INA+ and INA-, as well as INB+ and INB-, and set the common-mode voltage to mid-supply ($V_{DD}/2$) for optimum performance.

Analog Inputs and Reference Configurations

The full-scale range of the MAX1197 is determined by the internally generated voltage difference between REFP ($V_{DD}/2 + V_{REFIN}/4$) and REFN ($V_{DD}/2 - V_{REFIN}/4$). The full-scale range for both on-chip ADCs is adjustable through the REFIN pin, which is provided for this purpose.

The MAX1197 provides three modes of reference operation:

- Internal reference mode
- Buffered external reference mode
- Unbuffered external reference mode

In internal reference mode, connect the internal reference output REFOUT to REFIN through a resistor (e.g., 10kΩ) or resistor divider, if an application requires a reduced full-scale range. For stability and noise-filtering purposes, bypass REFIN with a >10nF capacitor to GND. In internal reference mode, REFOUT, COM, REFP, and REFN become low-impedance outputs.

In buffered external reference mode, adjust the reference voltage levels externally by applying a stable and accurate voltage at REFIN. In this mode, COM, REFP, and REFN are outputs. REFOUT can be left open or connected to REFIN through a >10kΩ resistor.

In unbuffered external reference mode, connect REFIN to GND. This deactivates the on-chip reference buffers for REFP, COM, and REFN. With their buffers shut down, these nodes become high-impedance inputs and can be driven through separate, external reference sources.

For detailed circuit suggestions and how to drive this dual ADC in buffered/unbuffered external reference mode, see the *Applications Information* section.

Clock Input (CLK)

The MAX1197's CLK input accepts a CMOS-compatible clock signal. Since the interstage conversion of the device depends on the repeatability of the rising and falling edges of the external clock, use a clock with low jitter and fast rise and fall times (<2ns). In particular, sampling occurs on the rising edge of the clock signal, requiring this edge to provide lowest possible jitter. Any significant aperture jitter would limit the SNR performance of the on-chip ADCs as follows:

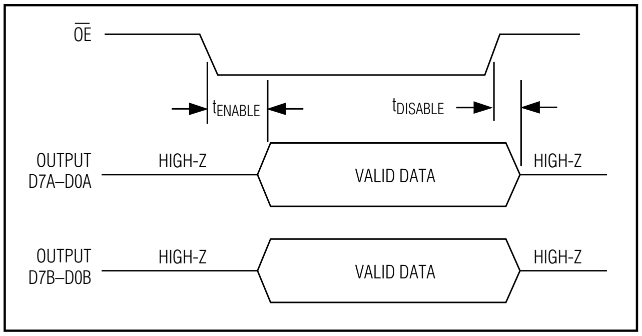


Figure 4. Output Timing Diagram

$$SNR = 20 \times \log \frac{1}{2 \times \pi \times f_{IN} \times t_{AJ}}$$

where f_{IN} represents the analog input frequency and t_{AJ} is the time of the aperture jitter.

Clock jitter is especially critical for undersampling applications. The clock input should always be considered as an analog input and routed away from any analog input or other digital signal lines.

The MAX1197 clock input operates with a voltage threshold set to $V_{DD}/2$. Clock inputs with a duty cycle other than 50% must meet the specifications for high and low periods as stated in the *Electrical Characteristics* table.

System Timing Requirements

Figure 3 depicts the relationship between the clock input, analog input, and data output. The MAX1197 samples at the rising edge of the input clock. Output data for channels A and B is valid on the next rising edge of the input clock. The output data has an internal latency of five clock cycles. Figure 3 also determines the relationship between the input clock parameters and the valid output data on channels A and B.

Digital Output Data (D0A/B–D7A/B), Output Data Format Selection (T/B), Output Enable (OE)

All digital outputs, D0A–D7A (channel A) and D0B–D7B (channel B), are TTL/CMOS-logic compatible. There is a five-clock-cycle latency between any particular sample and its corresponding output data. The output coding can either be straight offset binary or two's complement (Table 1) controlled by a single pin (T/B). Pull T/B low to select offset binary and high to activate two's complement output coding. The capacitive load on the digital outputs D0A–D7A and D0B–D7B should be kept as low as possible (<15pF), to avoid large digital currents that could feed back into the analog portion of the MAX1197, thereby degrading its dynamic performance. Using buffers on the digital outputs of the ADCs can further isolate the digital outputs from heavy capacitive loads. To further improve the dynamic performance of the MAX1197, small series resistors (e.g., 100Ω) may be added to the digital output paths close to the MAX1197.

Figure 4 displays the timing relationship between output enable and data output valid, as well as power-down/wake-up and data output valid.

Table 1. MAX1197 Output Codes For Differential Inputs

DIFFERENTIAL INPUT VOLTAGE*	DIFFERENTIAL INPUT	STRAIGHT OFFSET BINARY T/B = 0	TWO'S COMPLEMENT T/B = 1
V_{REF} x 255/256	+Full Scale -1LSB	1111 1111	0111 1111
V_{REF} x 1/256	+1LSB	1000 0001	0000 0001
0	Bipolar zero	1000 0000	0000 0000
$-V_{REF}$ x 1/256	-1LSB	0111 1111	1111 1111
$-V_{REF}$ x 255/256	-Full Scale +1LSB	0000 0001	1000 0001
$-V_{REF}$ x 256/256	-Full Scale	0000 0000	1000 0000

$^*V_{REF} = V_{REFP} - V_{REFN}$

Power-Down and Sleep Modes

The MAX1197 offers two power-save modes—sleep mode (SLEEP) and full power-down (PD) mode. In sleep mode (SLEEP = 1), only the reference bias circuit is active (both ADCs are disabled), and current consumption is reduced to 3mA.

To enter full power-down mode, pull PD high. With $\overline{OE}$ simultaneously low, all outputs are latched at the last value prior to the power down. Pulling $\overline{OE}$ high forces the digital outputs into a high-impedance state.

Applications Information

Figure 5 depicts a typical application circuit containing two single-ended-to-differential converters. The internal reference provides a $V_{DD}/2$ output voltage for level-shifting purposes. The input is buffered and then split to a voltage follower and inverter. One lowpass filter per amplifier suppresses some of the wideband noise associated with high-speed operational amplifiers. The user can select the R_{ISO} and C_{IN} values to optimize the filter performance, to suit a particular application. For the application in Figure 5, a R_{ISO} of 50Ω is placed before the capacitive load to prevent ringing and oscil-

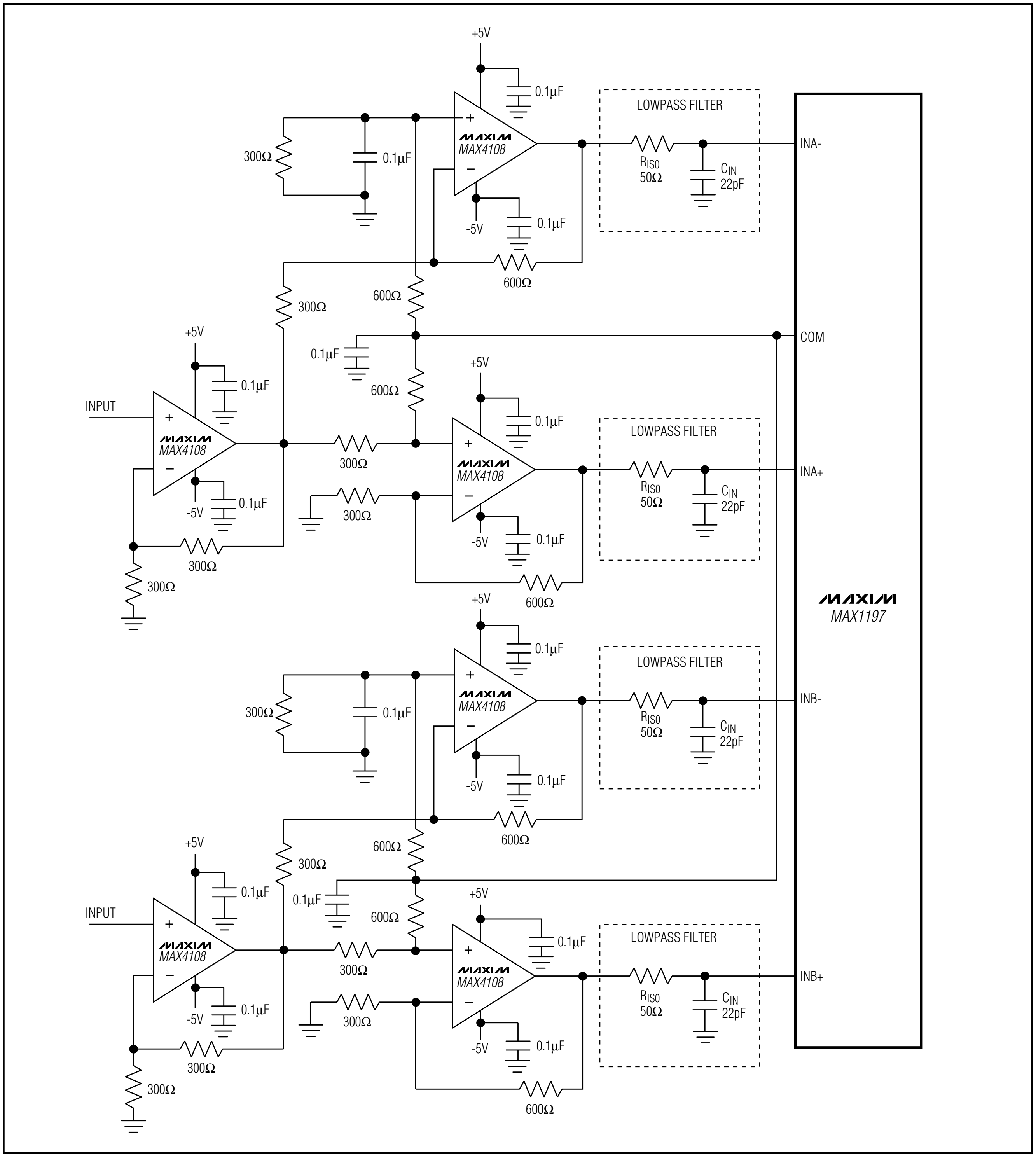


Figure 5. Typical Application for Single-Ended-to-Differential Conversion

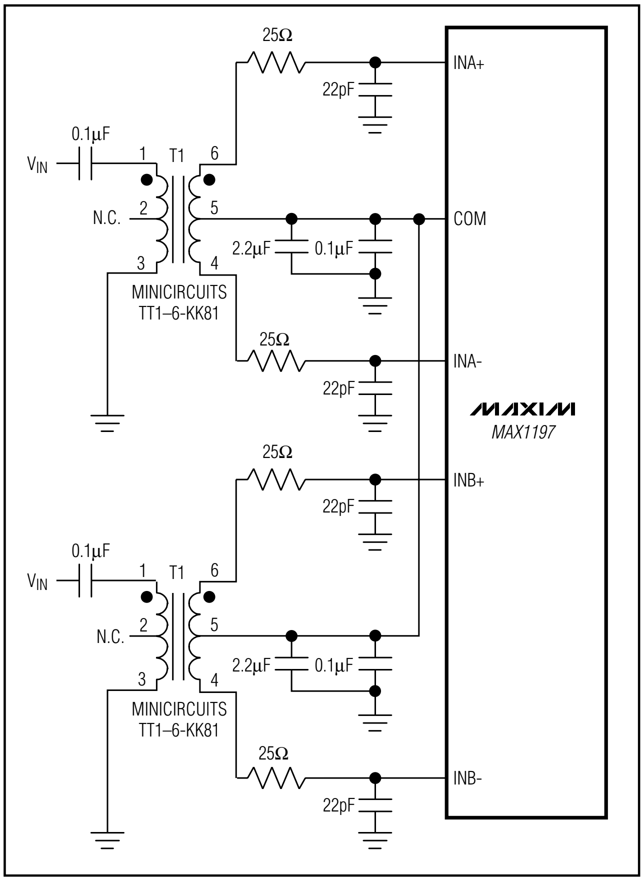


Figure 6. Transformer-Coupled Input Drive

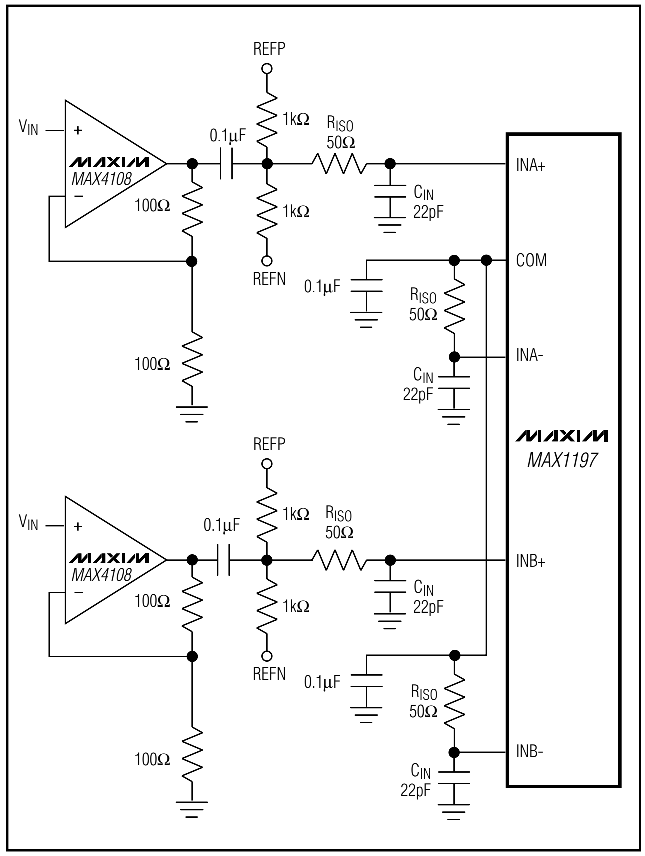


Figure 7. Using an Op Amp for Single-Ended, AC-Coupled Input Drive

lation. The 22pF C_{IN} capacitor acts as a small filter capacitor.

Using Transformer Coupling

An RF transformer (Figure 6) provides an excellent solution to convert a single-ended source signal to a fully differential signal, required by the MAX1197 for optimum performance. Connecting the center tap of the transformer to COM provides a $V_{DD}/2$ DC level shift to the input. Although a 1:1 transformer is shown, a step-up transformer can be selected to reduce the drive requirements. A reduced signal swing from the input driver, such as an op amp, can also improve the overall distortion.

In general, the MAX1197 provides better SFDR and THD with fully differential input signals than single-ended drive, especially for very high input frequencies. In differential input mode, even-order harmonics are lower as both inputs (INA+, INA- and/or INB+, INB-) are balanced, and each of the ADC inputs only requires half the signal swing compared to single-ended mode.

Single-Ended AC-Coupled Input Signal

Figure 7 shows an AC-coupled, single-ended application. Amplifiers like the MAX4108 provide high speed, high bandwidth, low noise, and low distortion to maintain the integrity of the input signal.

Buffered External Reference Drives Multiple ADCs

Multiple-converter systems based on the MAX1197 are well suited for use with a common reference voltage. The REFIN pin of those converters can be connected directly to an external reference source.

A precision bandgap reference like the MAX6062 generates an external DC level of 2.048V (Figure 8), and exhibits a noise voltage density of $150nV/\sqrt{Hz}$. Its output passes through a 1-pole lowpass filter (with 10Hz

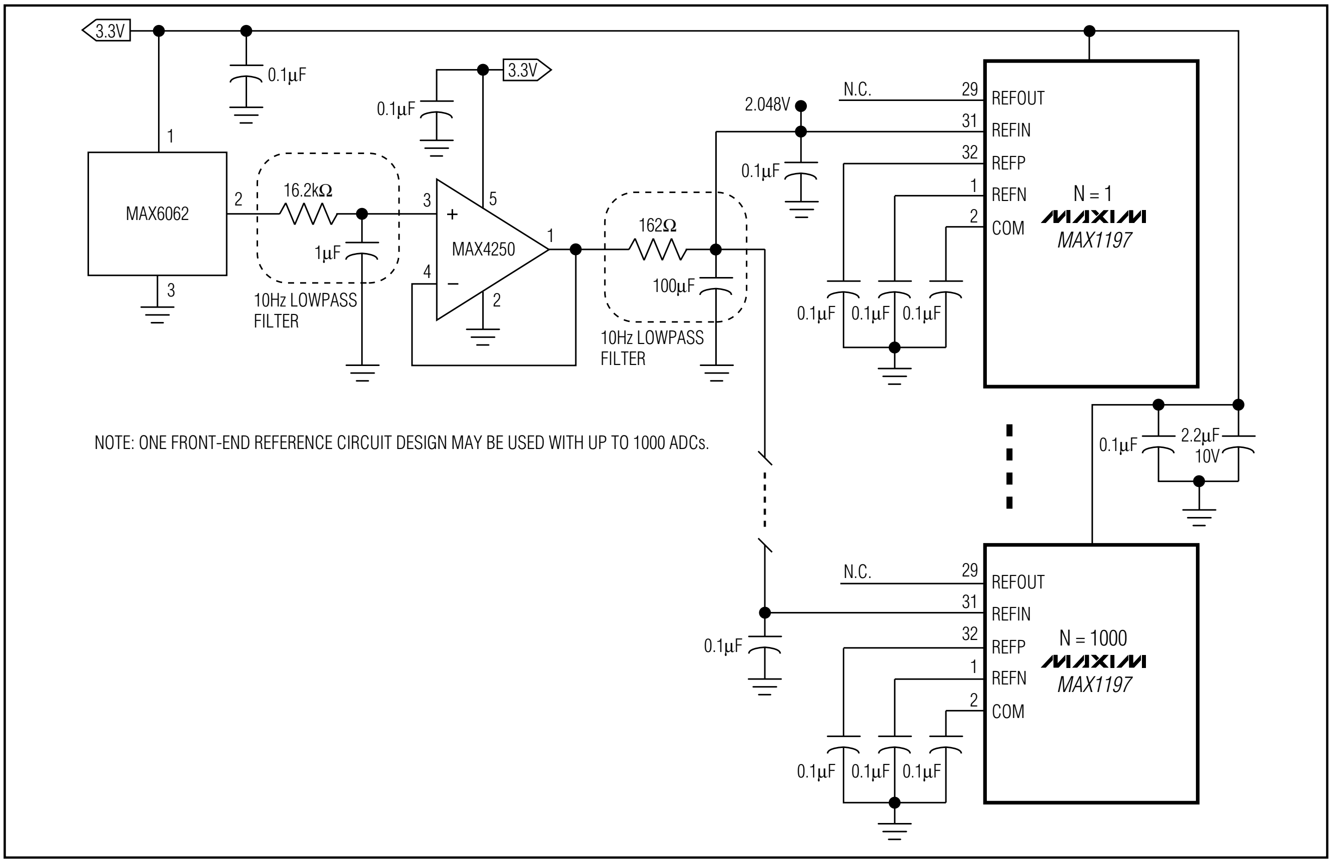


Figure 8. External Buffered (MAX4250) Reference Drive Using a MAX6062 Bandgap Reference

cutoff frequency) to the MAX4250, which buffers the reference before its output is applied to a second 10Hz lowpass filter. The MAX4250 provides a low offset voltage (for high gain accuracy) and a low noise level. The passive 10Hz filter following the buffer attenuates noise produced in the voltage reference and buffer stages. This filtered noise density, which decreases for higher frequencies, meets the noise levels specified for precision ADC operation.

Unbuffered External Reference Drives Multiple ADCs

Connecting each REFIN to analog ground disables the internal reference of each device, allowing the internal reference ladders to be driven directly by a set of external reference sources. Followed by a 10Hz lowpass filter and precision voltage divider, the MAX6066 generates a DC level of 2.500V. The buffered outputs of this divider are set to 2.0V, 1.5V, and 1.0V, with an accuracy that depends on the tolerance of the divider resistors. These three voltages are buffered by the MAX4252, which provides low noise and low DC offset. The individual voltage followers are connected to 10Hz lowpass filters, which filter both the reference voltage and amplifier noise to a level of $3nV/\sqrt{Hz}$. The 2.0V and 1.0V reference voltages set the differential full-scale range of the associated ADCs at $2V_{P-P}$. The 2.0V and 1.0V buffers drive the ADC's internal ladder resistances between them.

Note that the common power supply for all active components removes any concern regarding power-supply sequencing when powering up or down. With the outputs of the MAX4252 matching better than 0.1%, the buffers and subsequent lowpass filters can be replicated to support as many as 32 ADCs. For applications that require more than 32 matched ADCs, a voltage reference and divider string common to all converters is highly recommended.

Typical QAM Demodulation Application

A frequently used modulation technique in digital communications applications is quadrature amplitude

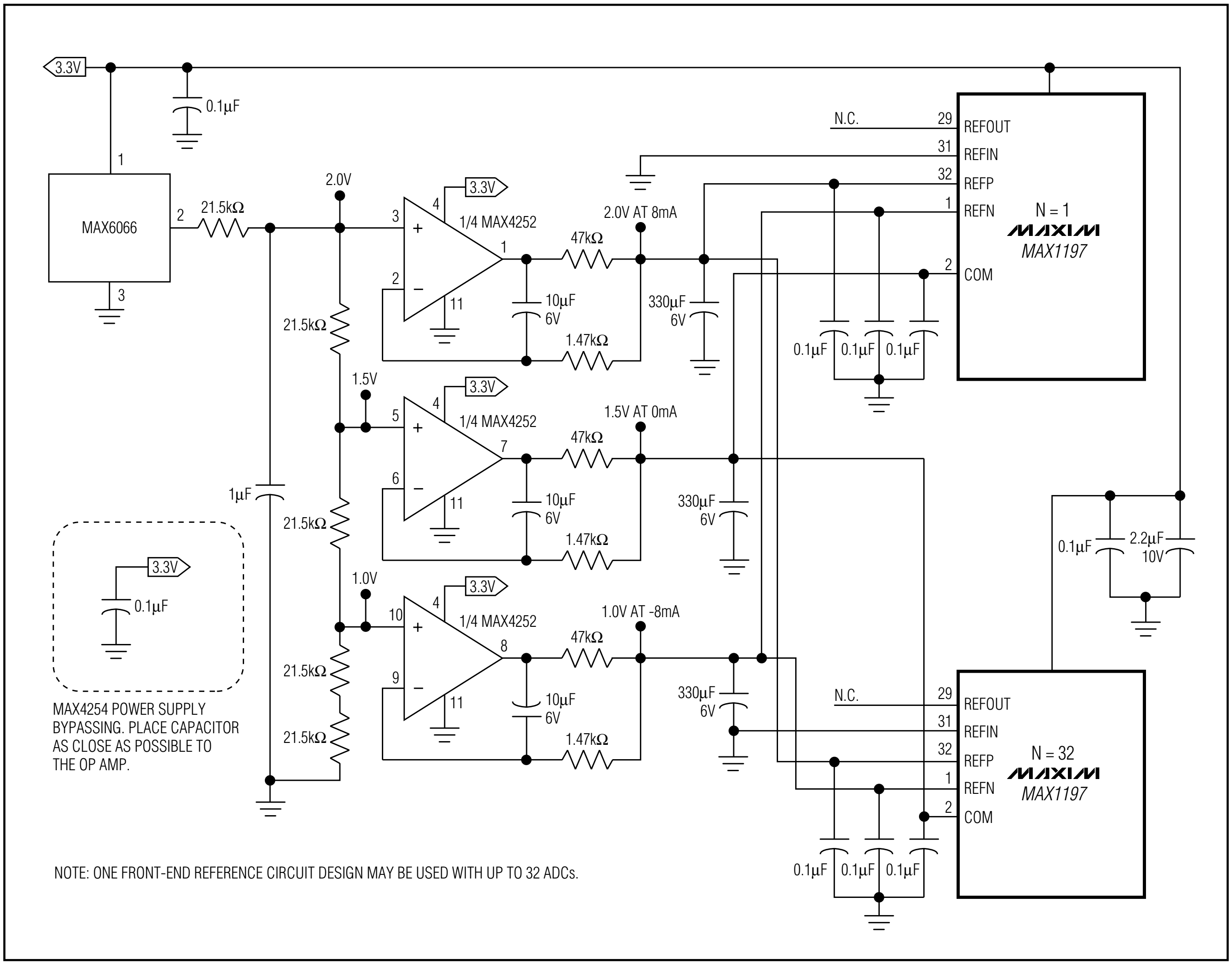


Figure 9. External Unbuffered Reference Drive with MAX4252 and MAX6066

modulation (QAM). Typically found in spread-spectrum-based systems, a QAM signal represents a carrier frequency modulated in both amplitude and phase. At the transmitter, modulating the baseband signal with quadrature outputs, a local oscillator followed by subsequent upconversion can generate the QAM signal. The result is an in-phase (I) and a quadrature (Q) carrier component, where the Q component is 90° phase shifted with respect to the in-phase component. At the receiver, the QAM signal is divided down into its I and Q components, essentially representing the modulation process reversed. Figure 10 displays the demodulation process performed in the analog domain, using the dual matched 3V, 8-bit ADC MAX1197 and the MAX2451 quadrature demodulator to recover and digitize the I and Q baseband signals. Before being digitized by the MAX1197, the mixed-down signal components may be filtered by matched analog filters, such as Nyquist or pulse-shaping filters which remove unwanted images from the mixing process, thereby enhancing the overall signal-to-noise (SNR) performance and minimizing intersymbol interference.

Grounding, Bypassing, and Board Layout

The MAX1197 requires high-speed board layout design techniques. Locate all bypass capacitors as close to the device as possible, preferably on the same side as the ADC, using surface-mount devices for minimum

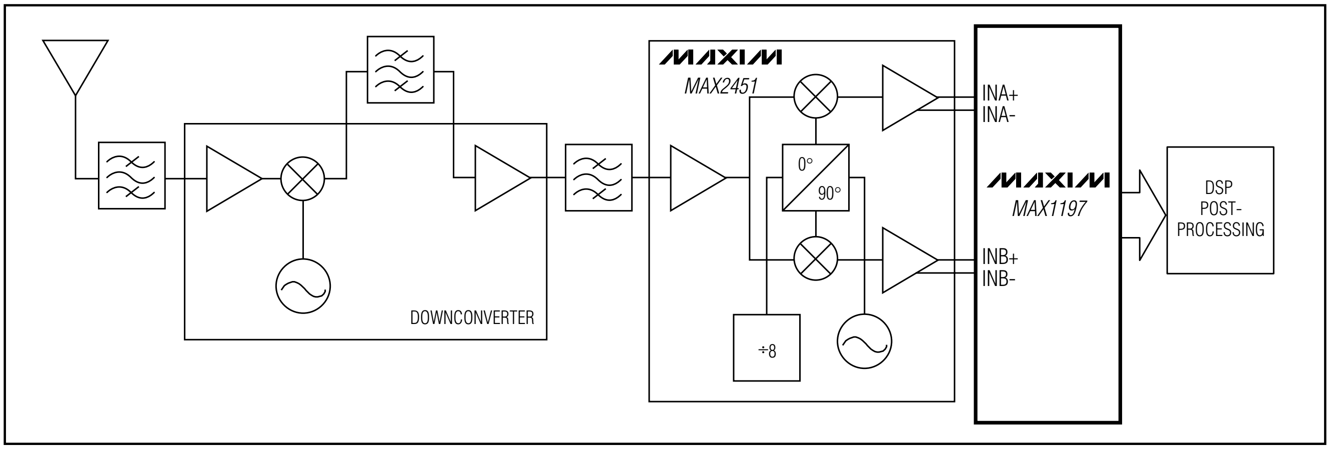


Figure 10. Typical QAM Application Using the MAX1197

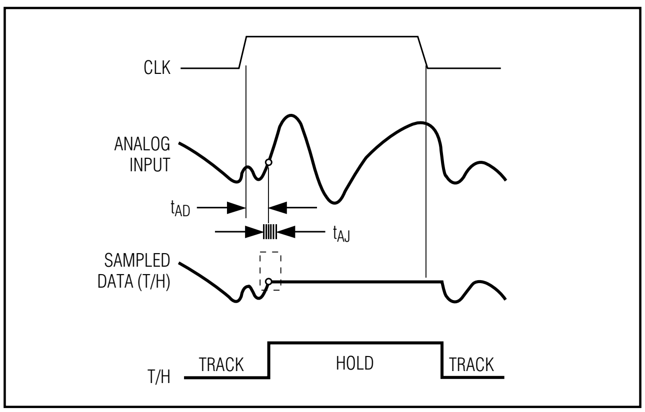


Figure 11. T/H Aperture Timing

inductance. Bypass V_{DD}, REFP, REFN, and COM with two parallel 0.1µF ceramic capacitors and a 2.2µF bipolar capacitor to GND. Follow the same rules to bypass the digital supply (OV_{DD}) to OGND. Multilayer boards with separated ground and power planes produce the highest level of signal integrity. Consider the use of a split ground plane arranged to match the physical location of the analog ground (GND) and the digital output driver ground (OGND) on the ADC's package. The two ground planes should be joined at a single point so the noisy digital ground currents do not interfere with the analog ground plane. The ideal location for this connection can be determined experimentally at a point along the gap between the two ground planes, which produces optimum results. Make this connection with a low-value, surface-mount resistor (1Ω to 5Ω), a ferrite bead, or a direct short.

Alternatively, all ground pins could share the same ground plane, if the ground plane is sufficiently isolated from any noisy, digital systems ground plane (e.g., downstream output buffer or DSP ground plane). Route high-speed digital signal traces away from the sensitive analog traces of either channel. Make sure to isolate the analog input lines to each respective converter to minimize channel-to-channel crosstalk. Keep all signal lines short and free of 90° turns.

Static Parameter Definitions

Integral Nonlinearity

Integral nonlinearity (INL) is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best-straight-line fit or a line drawn between the endpoints of the transfer function, once offset and gain errors have been nullified. The static linearity parameters for the MAX1197 are measured using the best-straight-line-fit method.

Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between an actual step width and the ideal value of 1LSB. A DNL error specification of less than 1LSB guarantees no missing codes and a monotonic transfer function.

Dynamic Parameter Definitions

Aperture Jitter

Figure 11 depicts the aperture jitter (t_{AJ}), which is the sample-to-sample variation in the aperture delay.

Aperture Delay

Aperture delay (t_{AD}) is the time defined between the rising edge of the sampling clock and the instant when an actual sample is taken (Figure 11).

Dual, 8-Bit, 60Msps, 3V, Low-Power ADC with Internal Reference and Parallel Outputs

Signal-to-Noise Ratio

For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization error only and results directly from the ADC's resolution (N-bits):

$$SNR_{dB[max]} = 6.02_{dB} \times N + 1.76_{dB}$$

In reality, there are other noise sources besides quantization noise: thermal noise, reference noise, clock jitter, etc. SNR is computed by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components minus the fundamental, the first five harmonics, and the DC offset.

Signal-to-Noise Plus Distortion

SINAD is computed by taking the ratio of the RMS signal to all spectral components minus the fundamental and the DC offset.

Effective Number of Bits

Effective number of bits (ENOB) specifies the dynamic performance of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. ENOB for a full-scale sinusoidal input waveform is computed from:

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

Total Harmonic Distortion

THD is typically the ratio of the RMS sum of the first four harmonics of the input signal to the fundamental itself. This is expressed as:

$$THD = 20 \times \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2}}{V_1}$$

where V_1 is the fundamental amplitude, and V_2 through V_5 are the amplitudes of the 2nd- through 5th-order harmonics.

Spurious-Free Dynamic Range

Spurious-free dynamic range (SFDR) is the ratio expressed in decibels of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next largest spurious component, excluding DC offset.

Intermodulation Distortion

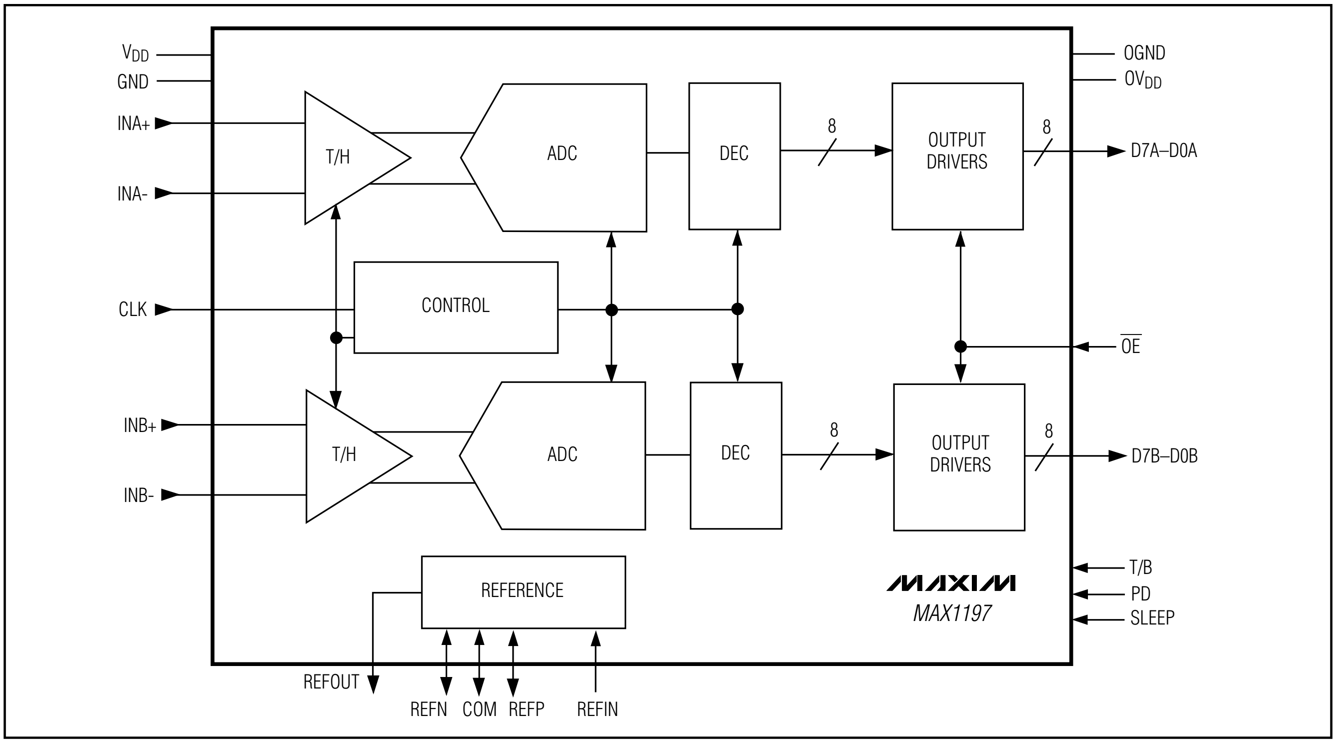
The two-tone intermodulation distortion (IMD) is the ratio expressed in decibels of either input tone to the worst third-order (or higher) intermodulation products. The individual input tone levels are at -7dB full scale and their envelope is at -1dB full scale.

Chip Information

TRANSISTOR COUNT: 11,601

PROCESS: CMOS

Functional Diagram



Pin-Compatible Upgrades (Sampling Speed and Resolution)

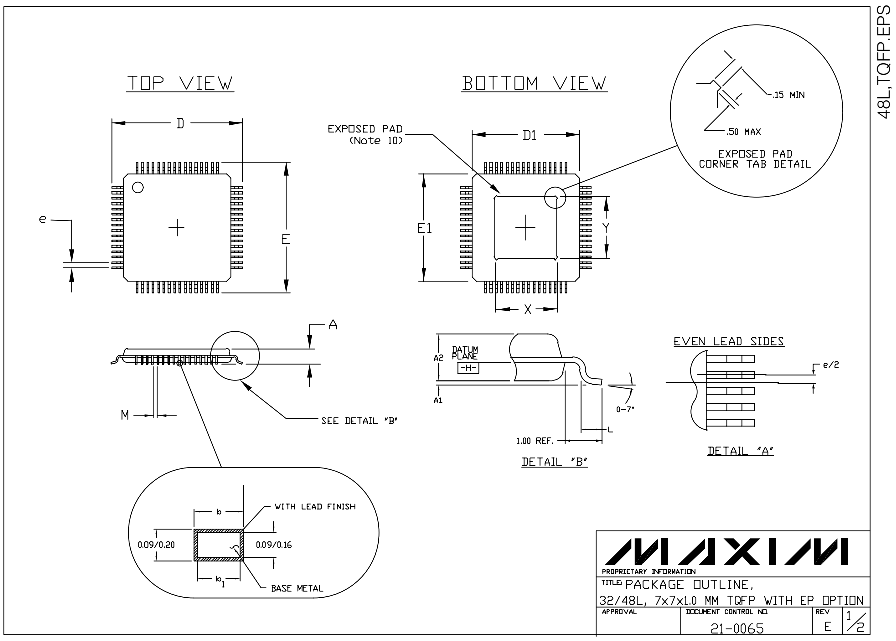
8-BIT PART	10-BIT PART	SAMPLING SPEED (Msps)
MAX1195	MAX1183	40
MAX1197	MAX1182	60
MAX1198	MAX1180	100
MAX1196*	MAX1186	40, multiplexed

*Future product, please contact factory for availability.

Dual, 8-Bit, 60Msps, 3V, Low-Power ADC with Internal Reference and Parallel Outputs

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



NOTES:
1. ALL DIMENSIONS AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE -H- IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. CONTROLLING DIMENSION: MILLIMETER.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136, VARIATIONS AC AND AE.
8. LEADS SHALL BE COPLANAR WITHIN .004 INCH.
9. EXPOSED DIE PAD SHALL BE COPLANAR WITH BOTTOM OF PACKAGE WITHIN 2 MILS (.05 MM).
10. DIMENSIONS X & Y APPLY TO EXPOSED PAD (EP) VERSIONS ONLY. SEE INDIVIDUAL PRODUCT DATASHEET TO DETERMINE IF A PRODUCT USES EXPOSED PAD PACKAGE.

SYMBOL	JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS					
	AC			AE		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	1.20
A_1	0.05	0.10	0.15	0.05	0.10	0.15
A_2	0.95	1.00	1.05	0.95	1.00	1.05
D	9.00 BSC.			9.00 BSC.		
D_1	7.00 BSC.			7.00 BSC.		
E	9.00 BSC.			9.00 BSC.		
E_1	7.00 BSC.			7.00 BSC.		
L	0.45	0.60	0.75	0.45	0.60	0.75
M	0.15	—	—	0.14	—	—
N	32			48		
e	0.80 BSC.			0.50 BSC.		
b	0.30	0.37	0.45	0.17	0.22	0.27
b1	0.30	0.35	0.40	0.17	0.20	0.23
*X	3.20	3.50	3.80	3.70	4.00	4.30
*Y	3.20	3.50	3.80	3.70	4.00	4.30

* EXPOSED PAD (Note 10)

PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, 32/48L, 7x7x1.0 MM TQFP WITH EP OPTION
APPROVAL | DOCUMENT CONTROL NO. 21-0065 | REV E | 2/2

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