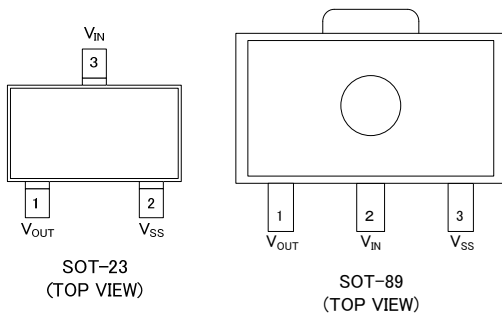


## ■ PIN CONFIGURATION



## ■ PIN ASSIGNMENT

PIN NUMBER		PIN NAME	FUNCTIONS
SOT-23	SOT-89		
3	2	V <sub>IN</sub>	Supply Voltage Input
2	3	V <sub>SS</sub>	Ground
1	1	V <sub>OUT</sub>	Output

## ■ PRODUCT CLASSIFICATION

### ● Ordering Information

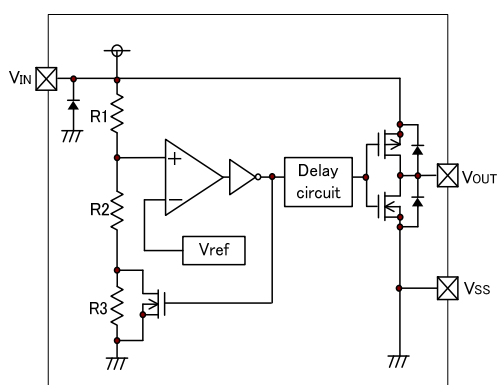
XC61F ①②③④⑤⑥⑦-⑧<sup>(\*)</sup>

DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①	Output Configuration	C	CMOS output
		N	N-ch open drain output
②③	Detect Voltage	16 ~ 60	e.g. 2.5V → ②2 , ③5
			e.g. 3.8V → ②3, ③8
④	Release Output Delay	1	50ms ~ 200ms
		4	80ms ~ 400ms
		5	1ms ~ 50ms
⑤	Detect Accuracy	2	Within ± 2.0%
⑥⑦-⑧ <sup>(*)</sup>	Packages (Order Unit)	MR	SOT-23 (3,000 pcs /Reel)
		MR-G	SOT-23 (3,000 pcs /Reel)
		PR	SOT-89 (1,000 pcs /Reel)
		PR-G	SOT-89 (1,000 pcs /Reel)

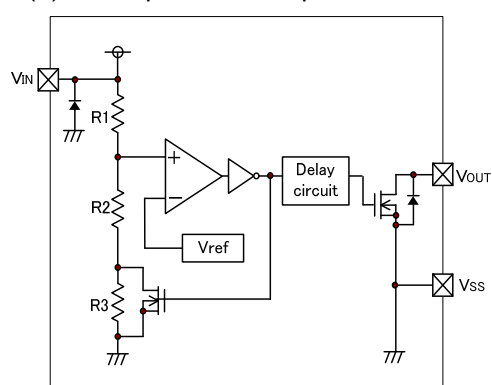
<sup>(\*)</sup> The "-G" suffix denotes Halogen and Antimony free as well as being fully EU RoHS compliant.

## ■ BLOCK DIAGRAMS

(1) CMOS output



(2) N-ch open drain output



## ■ ABSOLUTE MAXIMUM RATINGS

Ta = 25°C

PARAMETER	SYMBOL	RATINGS	UNITS
Input Voltage	V <sub>IN</sub>	V <sub>SS</sub> -0.3~12.0	V
Output Current	I <sub>OUT</sub>	50	mA
Output Voltage	CMOS	V <sub>SS</sub> -0.3 ~ V <sub>IN</sub> + 0.3	V
	N-ch open drain output	V <sub>SS</sub> -0.3 ~ 9	
Power Dissipation	SOT-23	250	mW
	SOT-89	500	
Operating Ambient Temperature	T <sub>opr</sub>	-30~+80	°C
Storage Temperature	T <sub>stg</sub>	-40~+125	°C

## ■ ELECTRICAL CHARACTERISTICS

Ta = 25°C

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT		
Detect Voltage	V <sub>DF</sub>		V <sub>DF(T)</sub> x 0.98	V <sub>DF(T)</sub>	V <sub>DF(T)</sub> x 1.02	V	①		
Hysteresis Width	V <sub>HYS</sub>		V <sub>DF</sub> x 0.02	V <sub>DF</sub> x 0.05	V <sub>DF</sub> x 0.08	V	①		
Supply Current	I <sub>SS</sub>	V <sub>IN</sub> = 1.5V	-	0.9	2.6	μA	②		
		V <sub>IN</sub> = 2.0V	-	1.0	3.0				
		V <sub>IN</sub> = 3.0V	-	1.3	3.4				
		V <sub>IN</sub> = 4.0V	-	1.6	3.8				
		V <sub>IN</sub> = 5.0V	-	2.0	4.2				
Operating Voltage	V <sub>IN</sub>	V <sub>DF</sub> = 1.6V to 6.0V	0.7	-	10.0	V	①		
Output Current	I <sub>OUT</sub>	N-ch V <sub>DS</sub> = 0.5V	V <sub>IN</sub> = 1.0V	1.0	2.2	-	mA	③	
			V <sub>IN</sub> = 2.0V	3.0	7.7	-			
			V <sub>IN</sub> = 3.0V	5.0	10.1	-			
			V <sub>IN</sub> = 4.0V	6.0	11.5	-			
			V <sub>IN</sub> = 5.0V	7.0	13.0	-			
		P-ch V <sub>DS</sub> = 2.1V (CMOS Output) V <sub>IN</sub> = 8.0V	-	-10.0	-2.0	④			
Leak Current	CMOS Output (P-ch)	I <sub>LEAK</sub>	V <sub>IN</sub> = V <sub>DF</sub> x 0.9V, V <sub>OUT</sub> = 0V	-	-0.01	-	μA	③	
	N-ch Open Drain Output		V <sub>IN</sub> = 10.0V, V <sub>OUT</sub> = 10.0V	-	0.01	0.1			
Detect Voltage Temperature Characteristics		ΔV <sub>DF</sub> / (ΔT <sub>opr</sub> · V <sub>DF</sub> )	-30°C ≤ T <sub>opr</sub> ≤ 80°C		-	±100	-	ppm/°C	①
Release Delay Time (V <sub>DR</sub> → V <sub>OUT</sub> inversion)		t <sub>DR</sub>	V <sub>IN</sub> changes from 0.6V to 10V		50	-	200	ms	⑤
			80		400				
			1		50				

V<sub>DF</sub> (T): Setting detect voltage value

Release Voltage: V<sub>DR</sub> = V<sub>DF</sub> + V<sub>HYS</sub>

\* Release Delay Time: 1ms to 50ms & 80ms to 400ms versions are also available.

Note: The power consumption during power-start to output being stable (release operation) is 2 μA greater than it is after that period (completion of release operation) because of delay circuit through current.

## ■ OPERATIONAL EXPLANATION

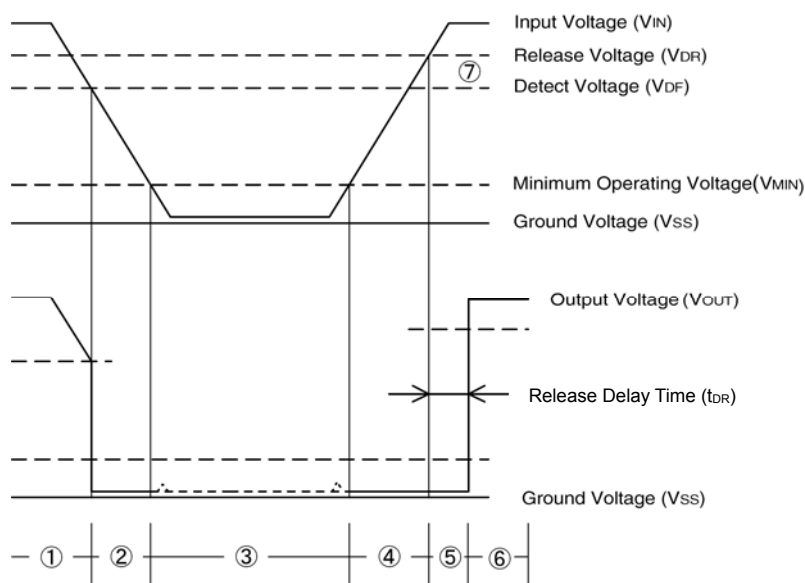
### ● CMOS output

- ① When a voltage higher than the release voltage ( $V_{DR}$ ) is applied to the voltage input pin ( $V_{IN}$ ), the voltage will gradually fall. When a voltage higher than the detect voltage ( $V_{DF}$ ) is applied to  $V_{IN}$ , output ( $V_{OUT}$ ) will be equal to the input at  $V_{IN}$ .  
Note that high impedance exists at  $V_{OUT}$  with the N-ch open drain output configuration. If the pin is pulled up,  $V_{OUT}$  will be equal to the pull up voltage.
- ② When  $V_{IN}$  falls below  $V_{DF}$ ,  $V_{OUT}$  will be equal to the ground voltage ( $V_{SS}$ ) level (detect state). Note that this also applies to N-ch open drain output configurations.
- ③ When  $V_{IN}$  falls to a level below that of the minimum operating voltage ( $V_{MIN}$ ) output will become unstable. Because the output pin is generally pulled up with configurations, output will be equal to pull up voltage.
- ④ When  $V_{IN}$  rises above the  $V_{SS}$  level (excepting levels lower than minimum operating voltage),  $V_{OUT}$  will be equal to  $V_{SS}$  until  $V_{IN}$  reaches the  $V_{DR}$  level.
- ⑤ Although  $V_{IN}$  will rise to a level higher than  $V_{DR}$ ,  $V_{OUT}$  maintains ground voltage level via the delay circuit.
- ⑥ Following transient delay time,  $V_{IN}$  will be output at  $V_{OUT}$ . Note that high impedance exists with the N-ch open drain output configuration and that voltage will be dependent on pull up.

#### Notes:

1. The difference between  $V_{DR}$  and  $V_{DF}$  represents the hysteresis range.
2. Release delay time ( $t_{DR}$ ) represents the time it takes for  $V_{IN}$  to appear at  $V_{OUT}$  once the said voltage has exceeded the  $V_{DR}$  level.

### ● Timing Chart



## ■ DIRECTIONS FOR USE

### ● Notes on Use

1. Please use this IC within the stated absolute maximum ratings. For temporary, transitional voltage drop or voltage rising phenomenon, the IC is liable to malfunction should the ratings be exceeded.
2. When a resistor is connected between the  $V_{IN}$  pin and the power supply with CMOS output configurations, oscillation may occur as a result of voltage drops at  $R_{IN}$  if load current ( $I_{OUT}$ ) exists. It is therefore recommend that no resistor be added. (refer to Oscillation Description (1) below)
3. When a resistor is connected between the  $V_{IN}$  pin and the power supply with CMOS output configurations, irrespective of N-ch output configurations, oscillation may occur as a result of through current at the time of voltage release even if load current ( $I_{OUT}$ ) does not exist. (refer to Oscillation Description (2) below)
4. If a resistor ( $R_{IN}$ ) must be used, then please use with as small a level of input impedance as possible in order to control the occurrences of oscillation as described above. Further, please ensure that  $R_{IN}$  is less than  $10k\Omega$  and that  $C_{IN}$  is more than  $0.1\mu F$ , please test with the actual device. However, N-ch open drain output only. (Figure 1).
5. With a resistor ( $R_{IN}$ ) connected between the  $V_{IN}$  pin and the power supply, the  $V_{IN}$  pin voltage will be getting lower than the power supply voltage as a result of the IC's supply current flowing through the  $V_{IN}$  pin.
6. Depending on circuit's operation, release delay time of this IC can be widely changed due to upper limits or lower limits of operational ambient temperature.
7. Torex places an importance on improving our products and its reliability. However, by any possibility, we would request user fail-safe design and post-aging treatment on system or equipment.

### ● Oscillation Description

#### (1) Oscillation as a result of load current with the CMOS output configuration:

When the voltage applied at power supply, release operations commence and the detector's output voltage increases. Load current ( $I_{OUT}$ ) will flow through  $R_L$ . Because a voltage drop ( $R_{IN} \times I_{OUT}$ ) is produced at the  $R_{IN}$  resistor, located between the power supply and the  $V_{IN}$  pin, the load current will flow via the IC's  $V_{IN}$  pin. The voltage drop will also lead to a fall in the voltage level at the  $V_{IN}$  pin. When the  $V_{IN}$  pin voltage level falls below the detect voltage level, detect operations will commence. Following detect operations, load current flow will cease and since voltage drop at  $R_{IN}$  will disappear, the voltage level at the  $V_{IN}$  pin will rise and release operations will begin over again.

Oscillation may occur with this " release - detect - release " repetition.

Further, this condition will also appear via means of a similar mechanism during detect operations.

#### (2) Oscillation as a result of through current:

Since the XC61F series are CMOS ICs, through current will flow when the IC's internal circuit switching operates (during release and detect operations). Consequently, oscillation is liable to occur during release voltage operations as a result of output current which is influenced by this through current (Figure 3).

Since hysteresis exists during detect operations, oscillation is unlikely to occur.

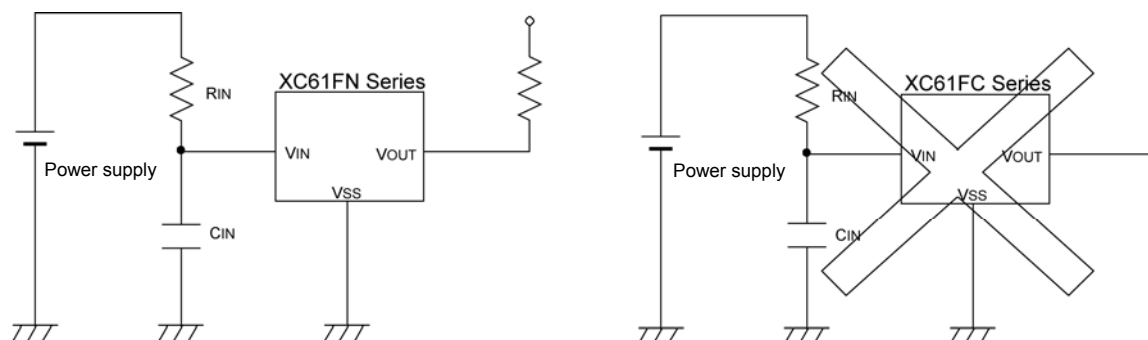


Figure 1. When using an input resistor

## ■ DIRECTIONS FOR USE (Continued)

### ● Oscillation Description (Continued)

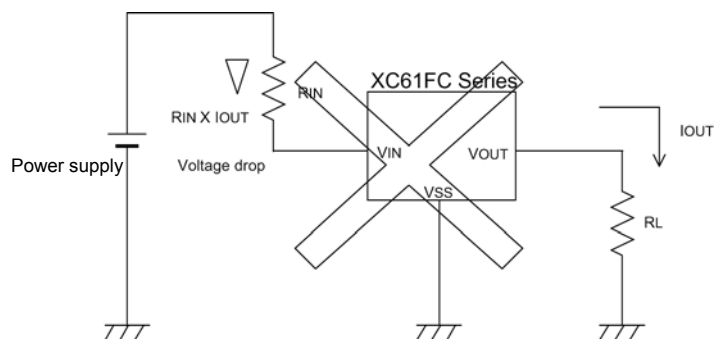


Figure 2. Oscillation in relation to output current

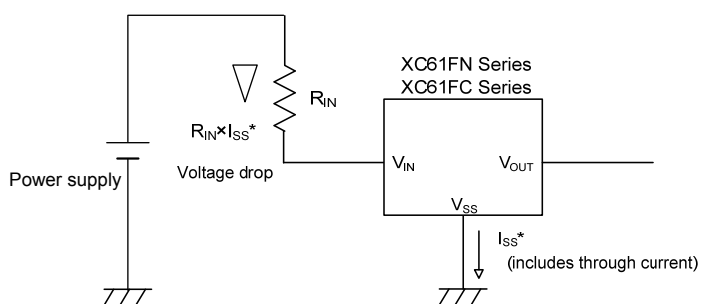
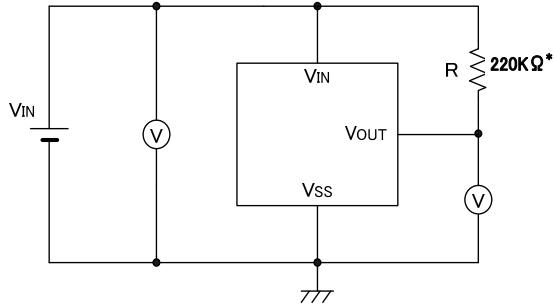


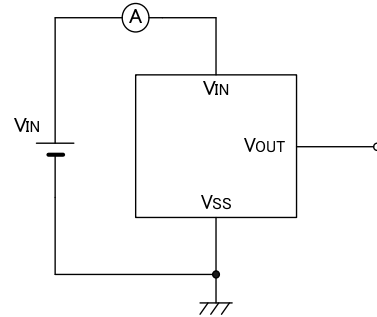
Figure 3. Oscillation in relation to through current

## TEST CIRCUITS

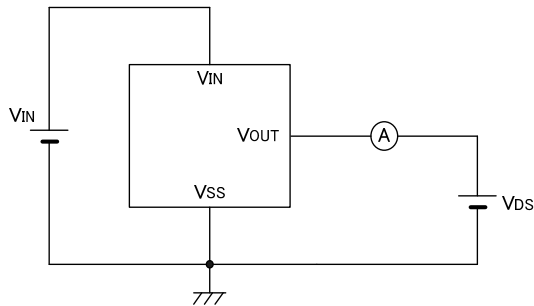
● Circuit ①



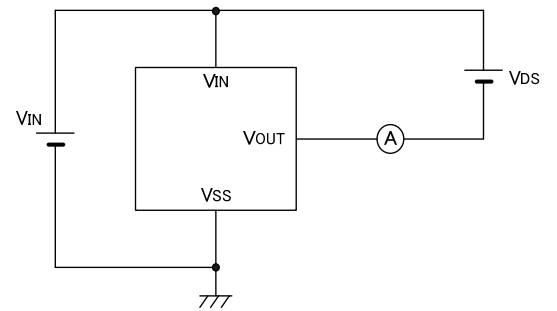
● Circuit ②



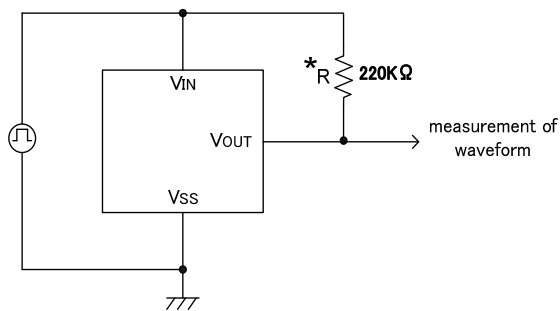
● Circuit ③



● Circuit ④



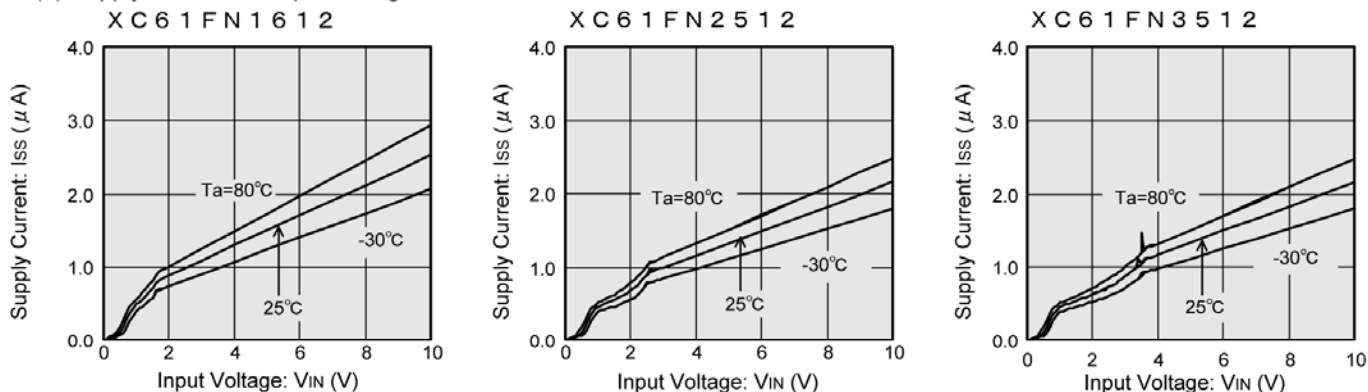
● Circuit ⑤



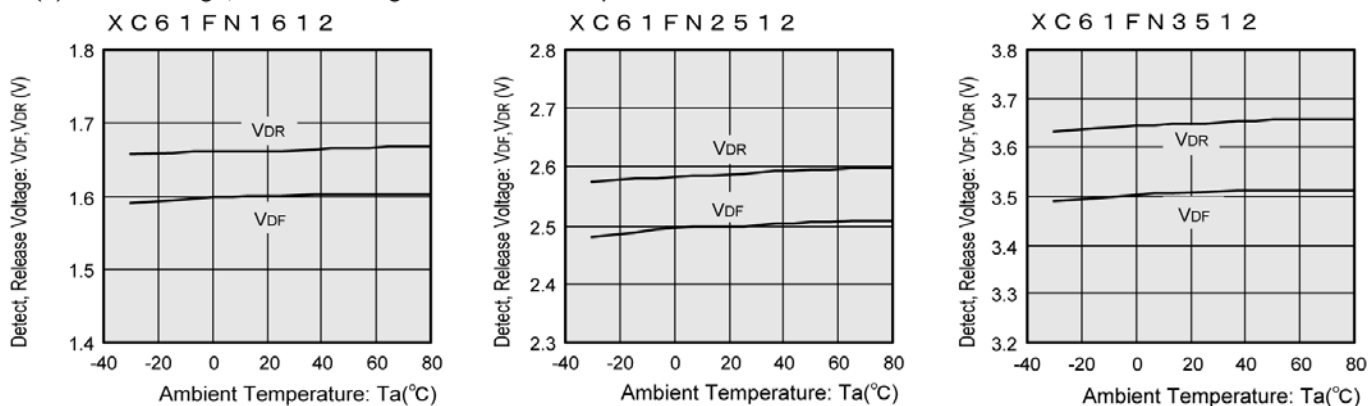
\*Not necessary with CMOS output products.

## TYPICAL PERFORMANCE CHARACTERISTICS

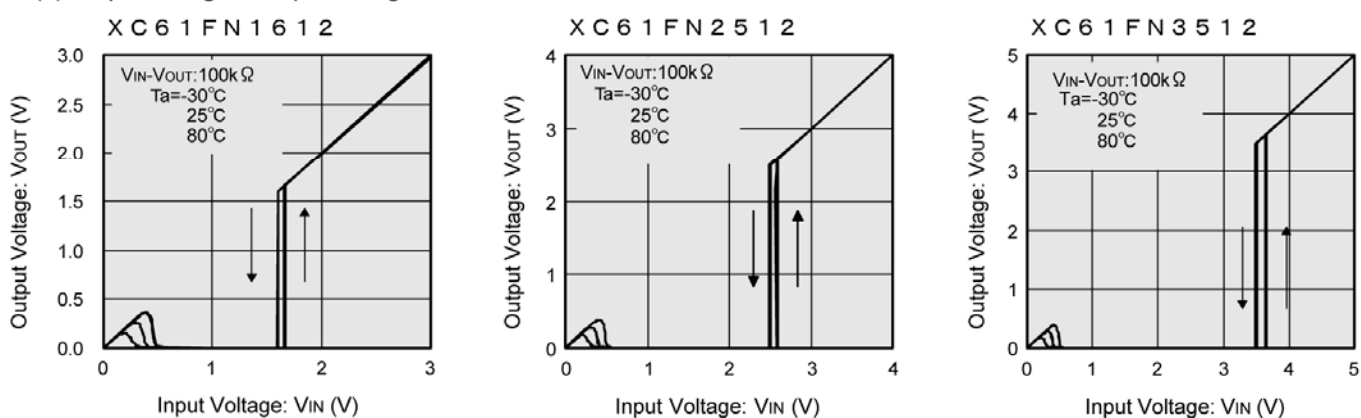
(1) Supply Current vs. Input Voltage



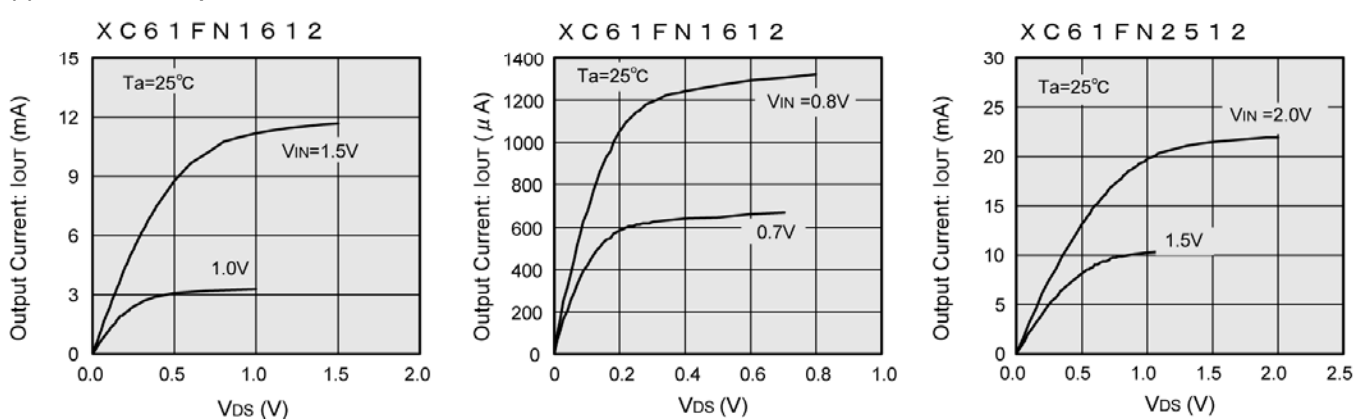
(2) Detect Voltage, Release Voltage vs. Ambient Temperature



(3) Output Voltage vs. Input Voltage



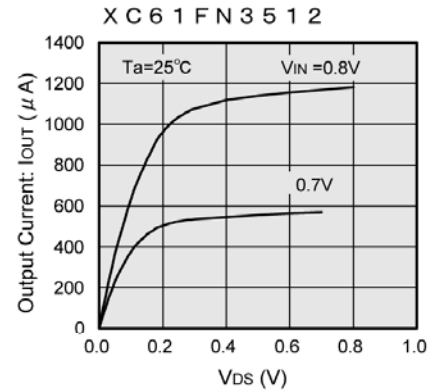
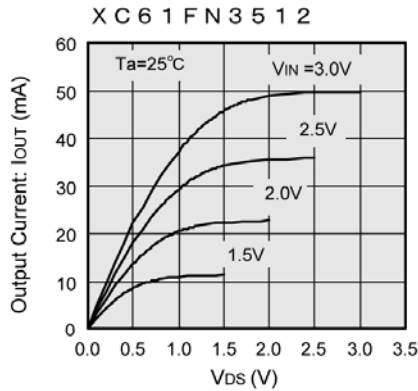
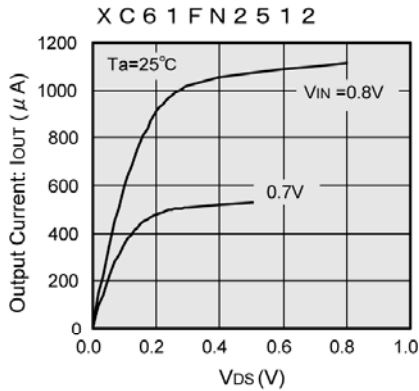
(4) N-ch Driver Output Current vs.  $V_{DS}$



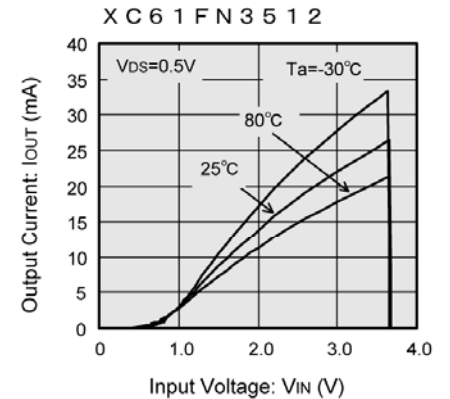
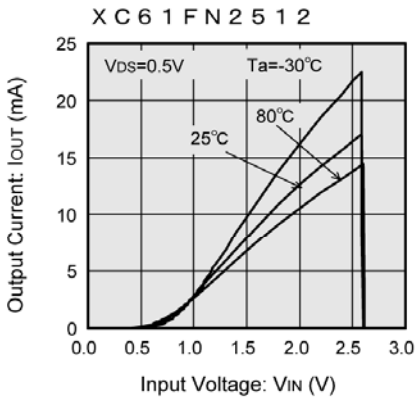
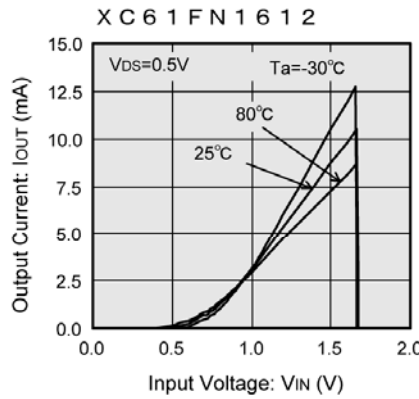


## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

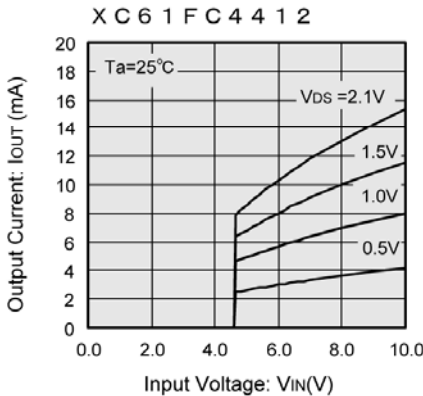
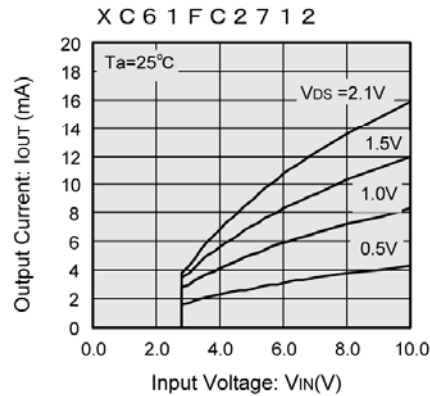
### (4) N-ch Driver Output Current vs. $V_{DS}$ (Continues)



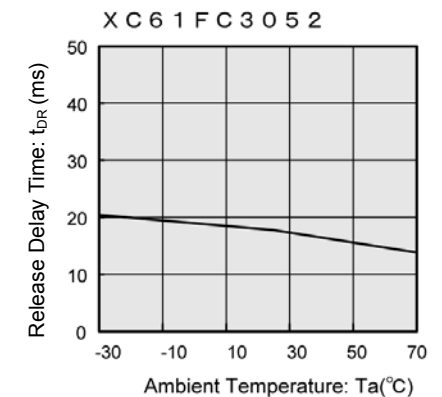
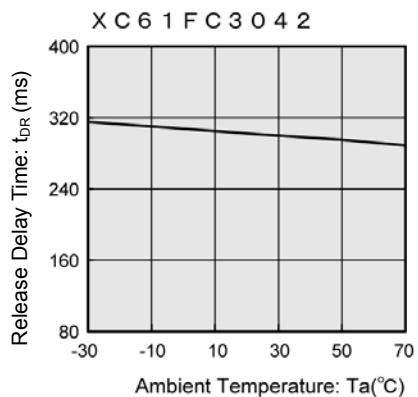
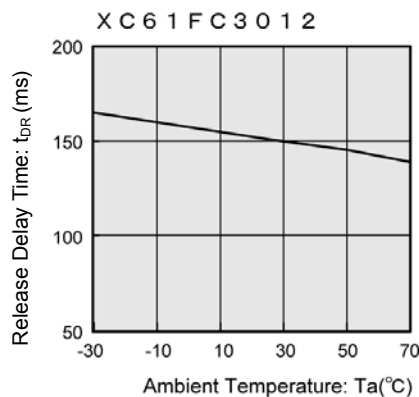
### (5) N-ch Driver Output Current vs. Input Voltage



### (6) P-ch Driver Output Current vs. Input Voltage

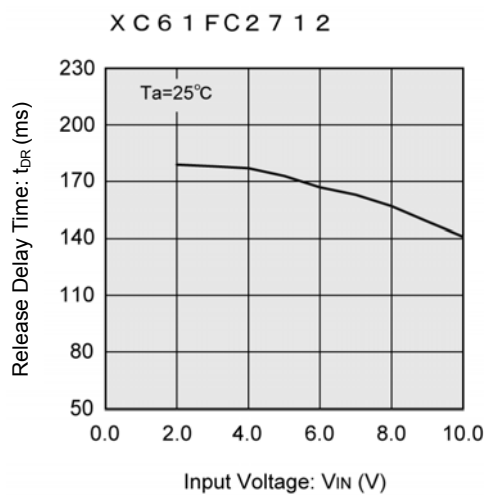


### (7) Release Delay Time vs. Ambient Temperature



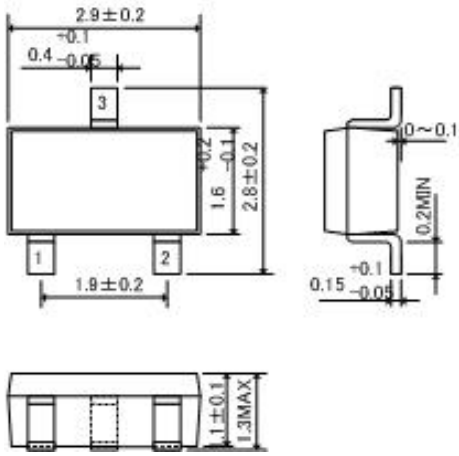
## ■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

### (8) Release Delay Time vs. Input Voltage

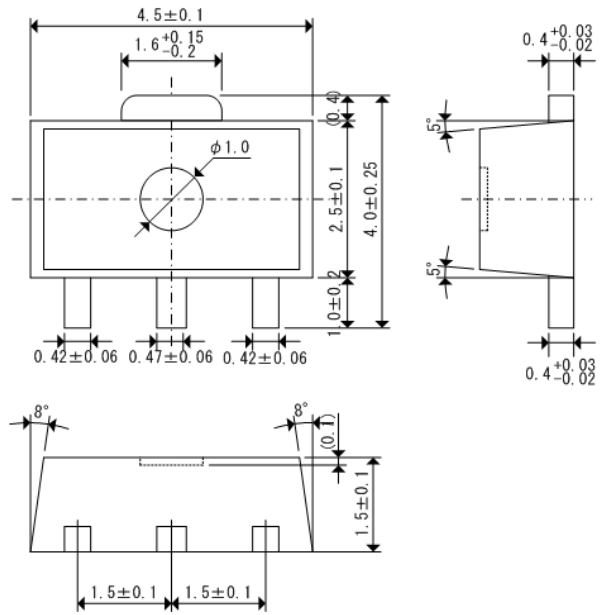


## PACKAGING INFORMATION

### ●SOT-23

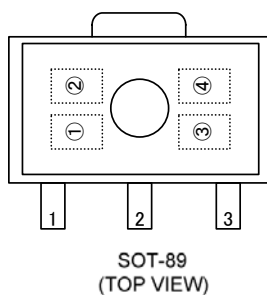
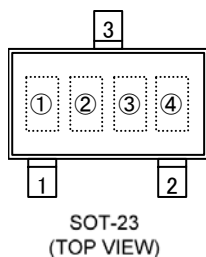


### ●SOT-89



## MARKING RULE

### ● SOT-23, SOT-89



① represents integer of detect voltage and output configuration  
CMOS output (XC61FC series)

MARK	CONFIGURATION	VOLTAGE (V)
A	CMOS	0.x
B	CMOS	1.x
C	CMOS	2.x
D	CMOS	3.x
E	CMOS	4.x
F	CMOS	5.x
H	CMOS	6.x

N-ch open drain output (XC61FN series)

MARK	CONFIGURATION	VOLTAGE (V)
K	N-ch	0.x
L	N-ch	1.x
M	N-ch	2.x
N	N-ch	3.x
P	N-ch	4.x
R	N-ch	5.x
S	N-ch	6.x

② represents decimal number of detect voltage

MARK	VOLTAGE (V)	MARK	VOLTAGE (V)
0	x.0	5	x.5
1	x.1	6	x.6
2	x.2	7	x.7
3	x.3	8	x.8
4	x.4	9	x.9

③ represents delay time

VOLTAGE (V)	DELAY TIME
5	50 ~ 200ms
6	80 ~ 400ms
7	1 ~ 50ms

④ represents assembly lot number (Based on internal standards)

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[XC61FN2642MR-G](#) [XC61FN4542MR-G](#) [XC61FN2112MR-G](#) [XC61FC2352MR-G](#) [XC61FC3012PR-G](#)  
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[XC61FN2712MR-G](#) [XC61FN3512PR-G](#) [XC61FN6012MR-G](#) [XC61FN4052MR-G](#) [XC61FN3712MR-G](#)  
[XC61FC4012MR-G](#) [XC61FN2042MR-G](#) [XC61FN2012MR-G](#) [XC61FN4542PR-G](#) [XC61FN4012PR-G](#)  
[XC61FN3642MR-G](#) [XC61FN2542MR-G](#) [XC61FN3142MR-G](#) [XC61FN2312MR-G](#) [XC61FN2412MR-G](#)  
[XC61FN2212MR-G](#) [XC61FN3512MR-G](#) [XC61FN2012PR-G](#) [XC61FN3012MR-G](#) [XC61FN2552MR-G](#)