

LM317M, NCV317MA, NCV317M

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Input-Output Voltage Differential	V _I -V _O	40	Vdc
Power Dissipation (Package Limitation) (Note 1)			
Plastic Package, T Suffix, Case 221A			
T _A = 25°C	P _D	Internally Limited	
Thermal Resistance, Junction-to-Air	θ _{JA}	70	°C/W
Thermal Resistance, Junction-to-Case	θ _{JC}	5.0	°C/W
Plastic Package, DT Suffix, Case 369C			
T _A = 25°C	P _D	Internally Limited	
Thermal Resistance, Junction-to-Air	θ _{JA}	92	°C/W
Thermal Resistance, Junction-to-Case	θ _{JC}	5.0	°C/W
Plastic Package, ST Suffix, Case 318E			
T _A = 25°C	P _D	Internally Limited	
Thermal Resistance, Junction-to-Air	θ _{JA}	245	°C/W
Thermal Resistance, Junction-to-Case	θ _{JC}	15	°C/W
Maximum Junction Temperature	T _{JMAX}	+150	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Figure 25 provides thermal resistance versus PC board pad size.

ELECTRICAL CHARACTERISTICS (V_I - V_O = 5.0 V; I_O = 0.1 A, T_J = T_{low} to T_{high} (Note 2), unless otherwise noted.)

Characteristics	Figure	Symbol	LM317M/LM317MB/NCV317MB			Unit
			Min	Typ	Max	
Line Regulation (Note 3) (T _A = 25°C, 3.0 V ≤ V _I - V _O ≤ 40 V)	3	Reg _{line}	-	0.01	0.04	%/V
Load Regulation (Note 3)	4	Reg _{load}				
T _A = 25°C, 10 mA ≤ I _O ≤ 0.5 A				5.0	25	mV
V _O ≤ 5.0 V			-	0.1	0.5	% V _O
V _O ≥ 5.0 V						
Adjustment Pin Current	5	I _{Adj}	-	50	100	μA
Adjustment Pin Current Change	3, 4	ΔI _{Adj}	-	0.2	5.0	μA
2.5 V ≤ V _I - V _O ≤ 40 V, 10 mA ≤ I _L ≤ 0.5 A, P _D ≤ P _{max}						
Reference Voltage	5	V _{ref}	1.20	1.25	1.30	V
3.0 V ≤ V _I - V _O ≤ 40 V, 10 mA ≤ I _L ≤ 0.5 A, P _D ≤ P _{max}						
Line Regulation 3.0 V ≤ V _I - V _O ≤ 40 V (Note 3)	3	Reg _{line}	-	0.02	0.07	%/V
Load Regulation 10 mA ≤ I _O ≤ 0.5 A (Note 3)	4	Reg _{load}				
V _O ≤ 5.0 V			-	20	70	mV
V _O ≥ 5.0 V			-	0.3	1.5	% V _O
Temperature Stability (T _{low} ≤ T _J ≤ T _{high})	5	T _S	-	0.7	-	% V _O
Minimum Load Current to Maintain Regulation (V _I - V _O = 40 V)	5	I _{Lmin}	-	3.5	10	mA
Maximum Output Current	5	I _{max}				A
V _I - V _O ≤ 15 V, P _D ≤ P _{max}			0.5	0.9	-	
V _I - V _O = 40 V, P _D ≤ P _{max} , T _A = 25°C			0.15	0.25	-	
RMS Noise, % of V _O (T _A = 25°C, 10 Hz ≤ f ≤ 10 kHz)	-	N	-	0.003	-	% V _O
Ripple Rejection, V _O = 10 V, f = 120 Hz (Note 4)	6	RR				dB
Without C _{Adj}			-	65	-	
C _{Adj} = 10 μF			66	80	-	
Thermal Shutdown (Note 5)	-	-	-	180	-	°C
Long-Term Stability, T _J = T _{high} (Note 6)	5	S	-	0.3	1.0	%/1.0 kHrs.
T _A = 25°C for End-point Measurements						

2. T_{low} to T_{high} = 0° to +125°C for LM317M T_{low} to T_{high} = -40° to +125°C for LM317MB, NCV317MB.

3. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

4. C_{Adj}, when used, is connected between the adjustment pin and ground.

5. Thermal characteristics are not subject to production test.

6. Since Long-Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot-to-lot.

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ELECTRICAL CHARACTERISTICS ($V_I - V_O = 5.0\text{ V}$; $I_O = 0.1\text{ A}$, $T_J = T_{\text{low}}$ to T_{high} (Note 7), unless otherwise noted.)

Characteristics	Figure	Symbol	LM317M/LM317MAB/NCV317MAB			Unit
			Min	Typ	Max	
Line Regulation (Note 8) ($T_A = 25^\circ\text{C}$, $3.0\text{ V} \leq V_I - V_O \leq 40\text{ V}$)	3	Reg_{line}	–	0.01	0.04	%/V
Load Regulation (Note 8) $T_A = 25^\circ\text{C}$, $10\text{ mA} \leq I_O \leq 0.5\text{ A}$ $V_O \leq 5.0\text{ V}$ $V_O \geq 5.0\text{ V}$	4	Reg_{load}	– –	5.0 0.1	25 0.5	mV % V_O
Adjustment Pin Current	5	I_{Adj}	–	50	100	μA
Adjustment Pin Current Change $2.5\text{ V} \leq V_I - V_O \leq 40\text{ V}$, $10\text{ mA} \leq I_L \leq 0.5\text{ A}$, $P_D \leq P_{\text{max}}$	3, 4	ΔI_{Adj}	–	0.2	5.0	μA
Reference Voltage $3.0\text{ V} \leq V_I - V_O \leq 40\text{ V}$, $10\text{ mA} \leq I_L \leq 0.5\text{ A}$, $P_D \leq P_{\text{max}}$	5	V_{ref}	1.225	1.250	1.275	V
Line Regulation (Note 8) $3.0\text{ V} \leq V_I - V_O \leq 40\text{ V}$	3	Reg_{line}	–	0.02	0.07	%/V
Load Regulation (Note 8) $10\text{ mA} \leq I_O \leq 0.5\text{ A}$ $V_O \leq 5.0\text{ V}$ $V_O \geq 5.0\text{ V}$	4	Reg_{load}	– –	20 0.3	70 1.5	mV % V_O
Temperature Stability ($T_{\text{low}} \leq T_J \leq T_{\text{high}}$)	5	T_S	–	0.7	–	% V_O
Minimum Load Current to Maintain Regulation ($V_I - V_O = 40\text{ V}$)	5	I_{Lmin}	–	3.5	10	mA
Maximum Output Current $V_I - V_O \leq 15\text{ V}$, $P_D \leq P_{\text{max}}$ $V_I - V_O = 40\text{ V}$, $P_D \leq P_{\text{max}}$, $T_A = 25^\circ\text{C}$	5	I_{max}	0.5 0.15	0.9 0.25	– –	A
RMS Noise, % of V_O ($T_A = 25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 10\text{ kHz}$)	–	N	–	–	–	% V_O
Ripple Rejection, $V_O = 10\text{ V}$, $f = 120\text{ Hz}$ (Note 9) Without C_{Adj} $C_{\text{Adj}} = 10\text{ }\mu\text{F}$	6	RR	– 66	65 80	– –	dB
Thermal Shutdown (Note 10)	–	–	–	180	–	$^\circ\text{C}$
Long-Term Stability, $T_J = T_{\text{high}}$ (Note 11) $T_A = 25^\circ\text{C}$ for End-point Measurements	5	S	–	0.3	1.0	%/1.0 kHrs.

7. T_{low} to $T_{\text{high}} = 0^\circ$ to $+125^\circ\text{C}$ for LM317MA T_{low} to $T_{\text{high}} = -40^\circ$ to $+125^\circ\text{C}$ for LM317MAB, NCV317MAB.

8. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

9. C_{Adj} , when used, is connected between the adjustment pin and ground.

10. Thermal characteristics are not subject to production test.

11. Since Long-Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot-to-lot.

LM317M, NCV317MA, NCV317M

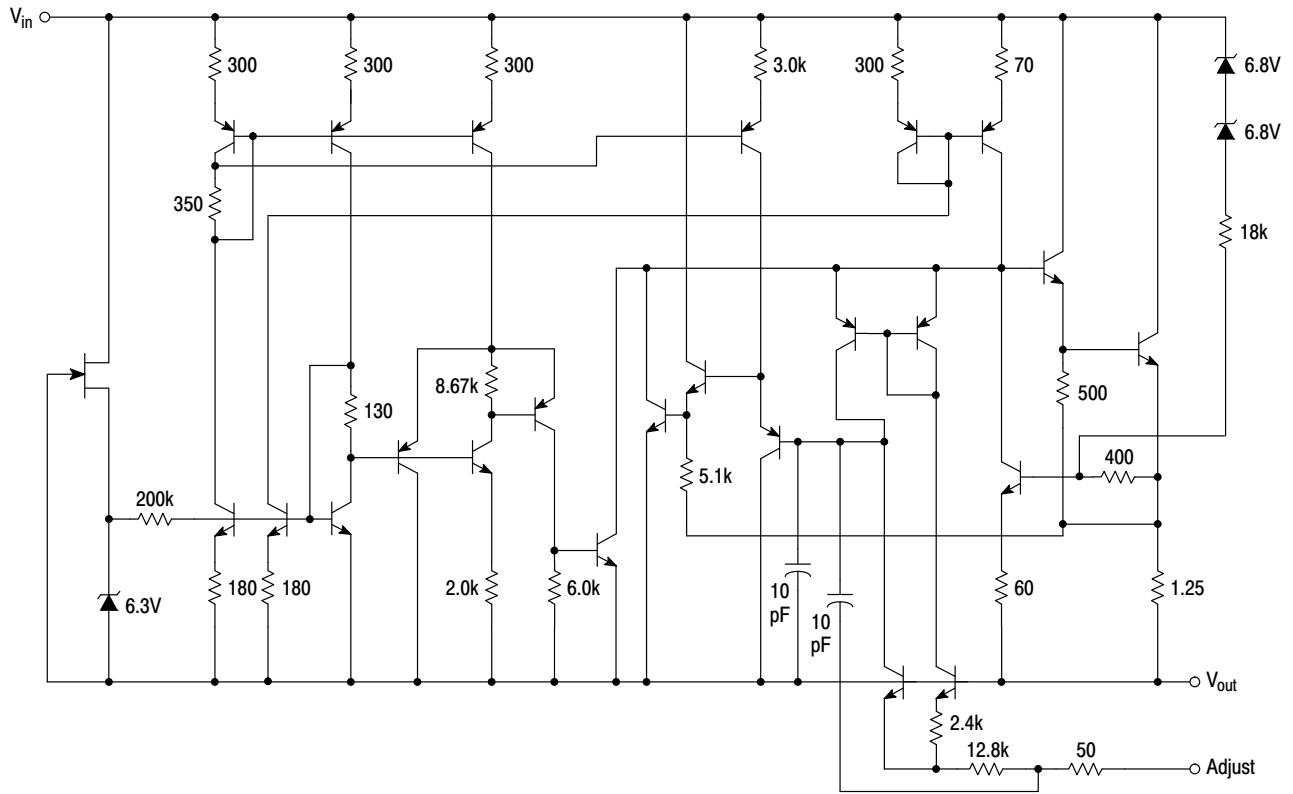


Figure 2. Representative Schematic Diagram

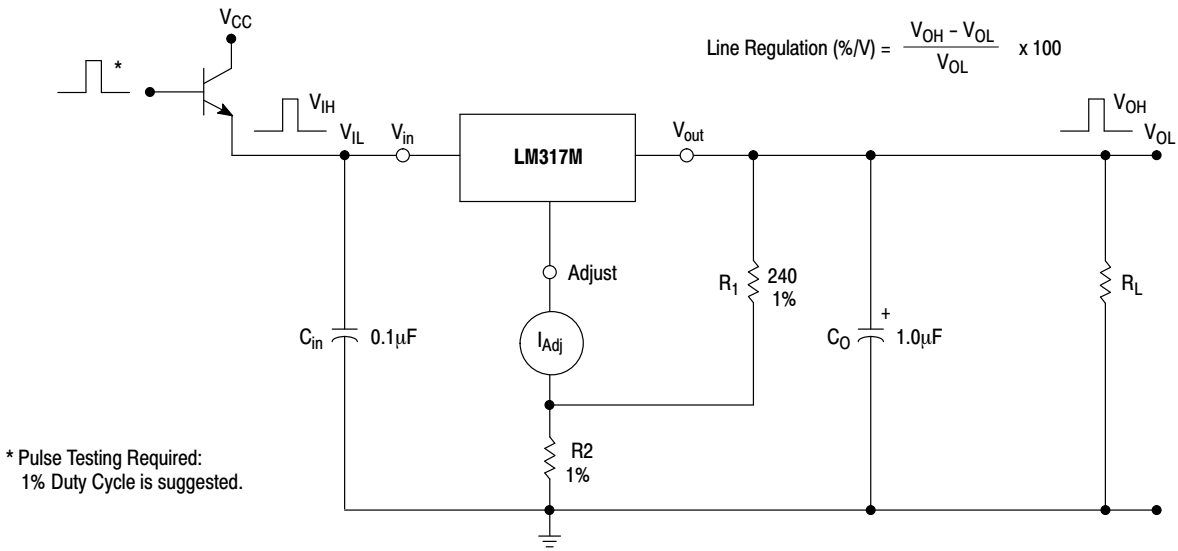
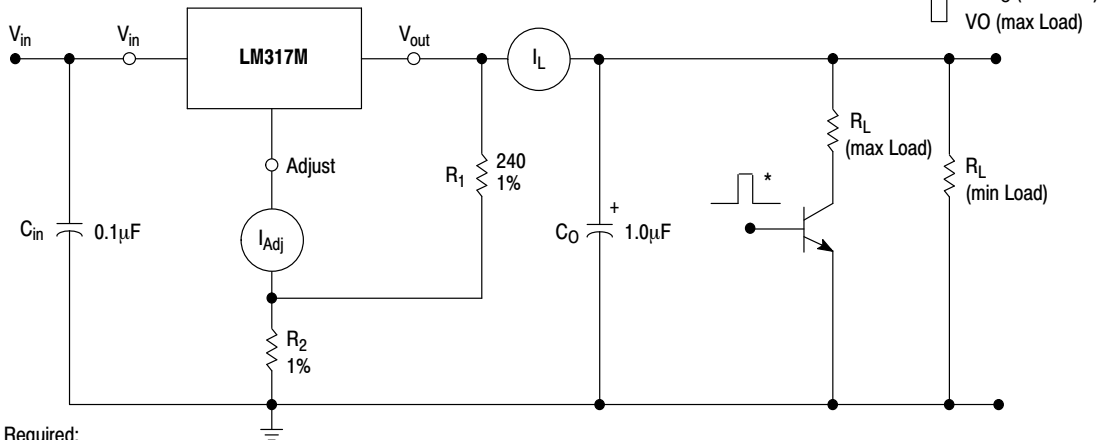


Figure 3. Line Regulation and ΔI_{Adj} /Line Test Circuit

LM317M, NCV317MA, NCV317M

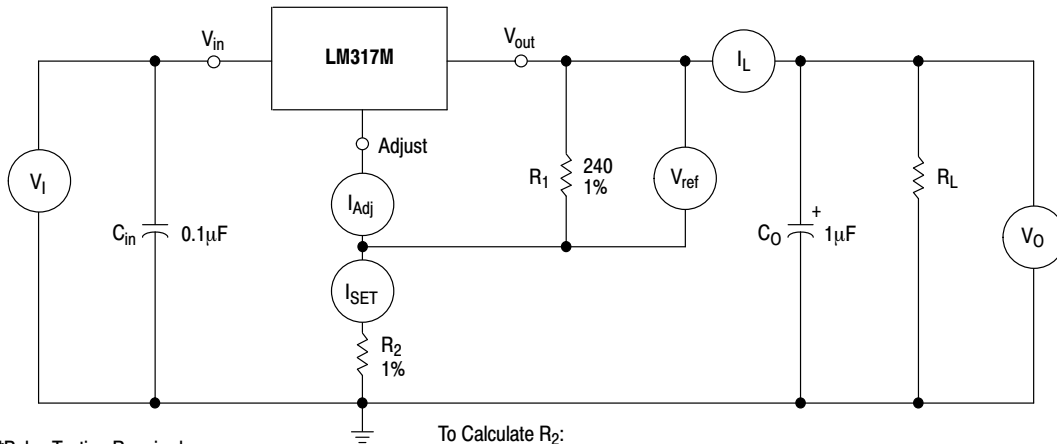
$$\text{Load Regulation (mV)} = V_O (\text{min Load}) - V_O (\text{max Load})$$

$$\text{Load Regulation (\% } V_O) = \frac{V_O (\text{min Load}) - V_O (\text{max Load})}{V_O (\text{min Load})} \times 100$$



* Pulse Testing Required:
1% Duty Cycle is suggested.

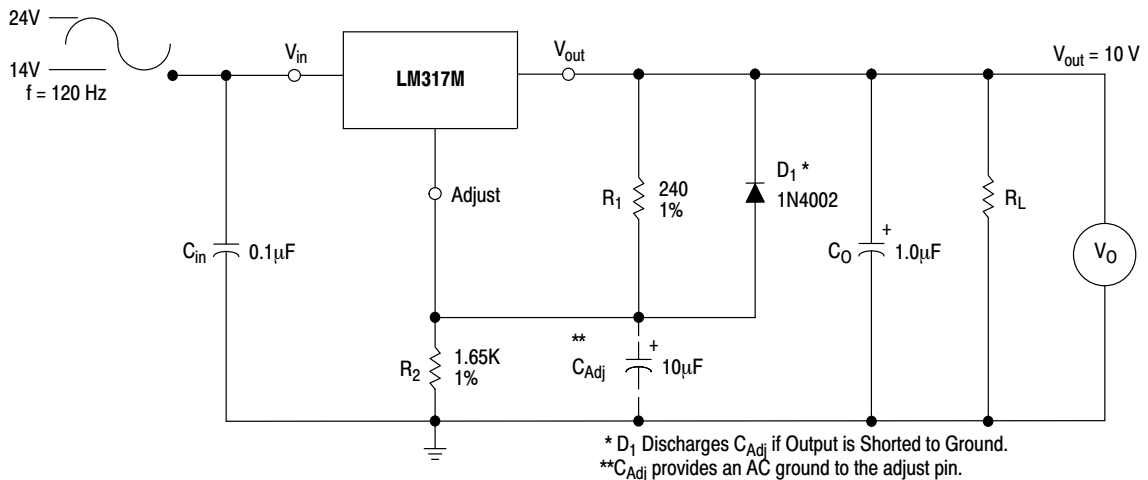
Figure 4. Load Regulation and ΔI_{Adj} /Load Test Circuit



*Pulse Testing Required:
1% Duty Cycle is suggested.

To Calculate R_2 :
 $V_{out} = I_{SET} R_2 + 1.250 \text{ V}$
Assume $I_{SET} = 5.25 \text{ mA}$

Figure 5. Standard Test Circuit



* D_1 Discharges C_{Adj} if Output is Shorted to Ground.
** C_{Adj} provides an AC ground to the adjust pin.

Figure 6. Ripple Rejection Test Circuit

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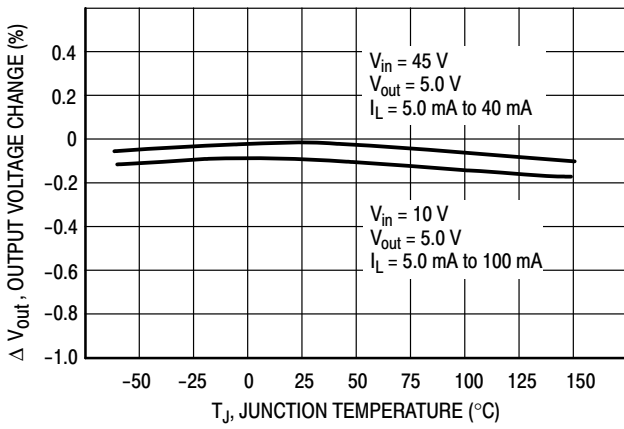


Figure 7. Load Regulation

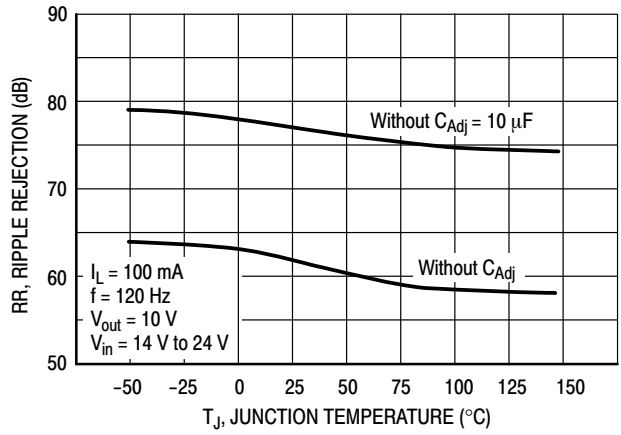


Figure 8. Ripple Rejection

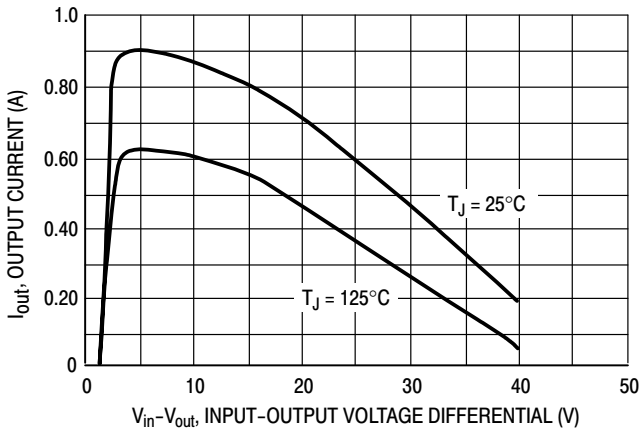


Figure 9. Current Limit

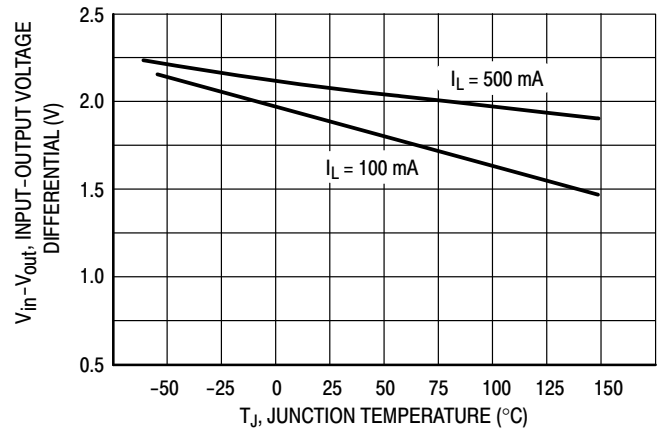


Figure 10. Dropout Voltage

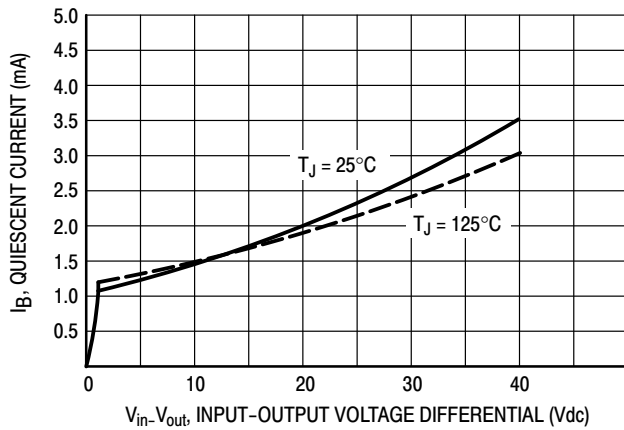


Figure 11. Minimum Operating Current

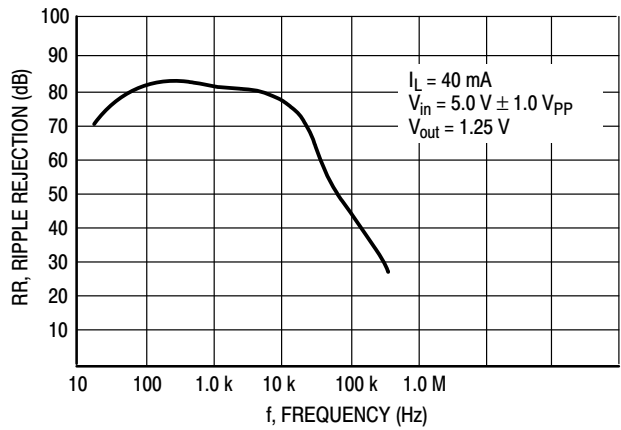


Figure 12. Ripple Rejection versus Frequency

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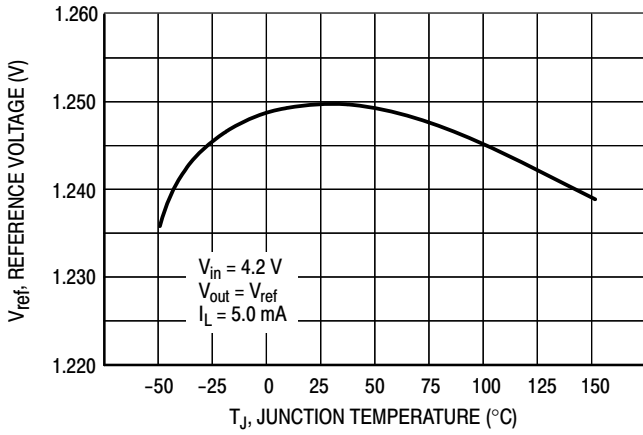


Figure 13. Temperature Stability

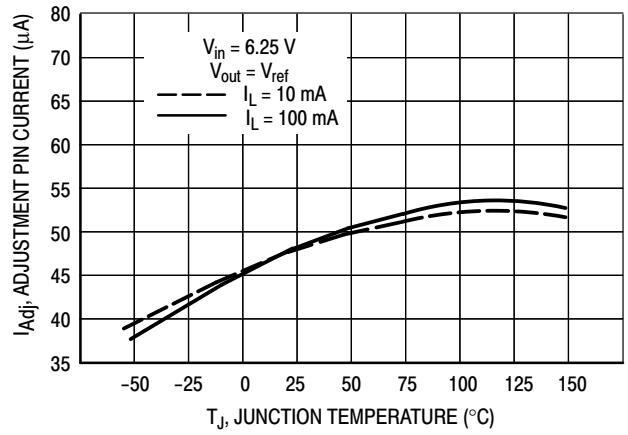


Figure 14. Adjustment Pin Current

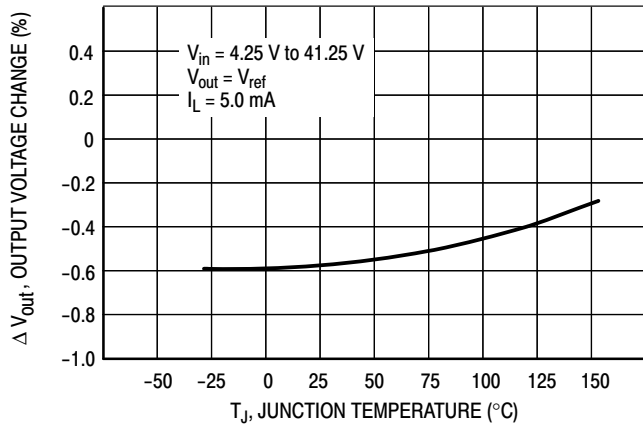


Figure 15. Line Regulation

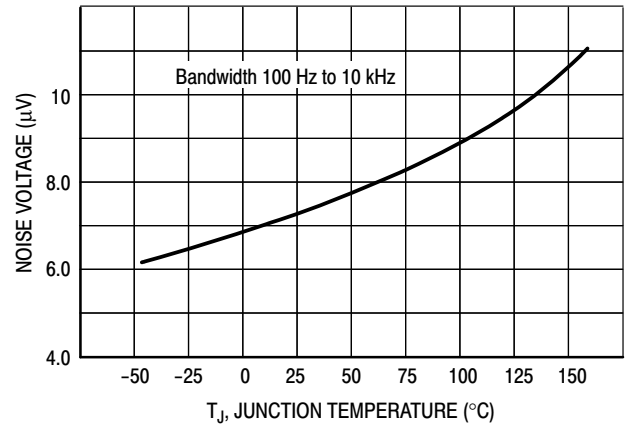


Figure 16. Output Noise

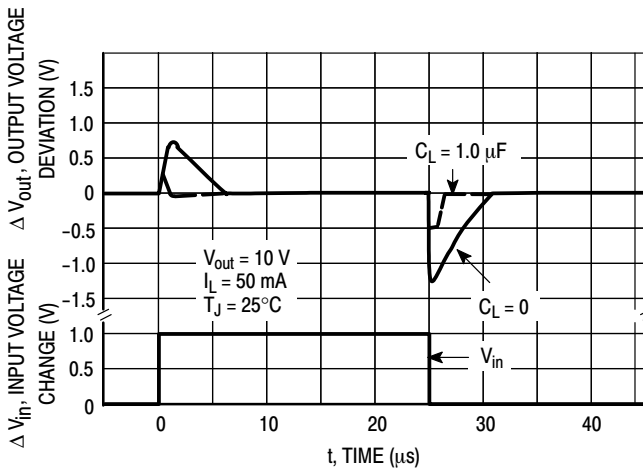


Figure 17. Line Transient Response

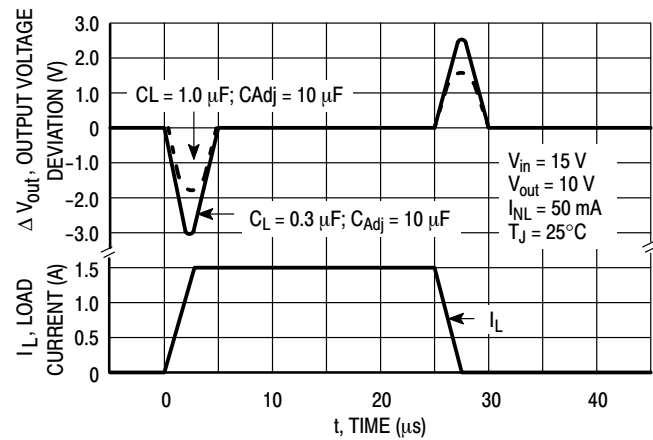


Figure 18. Load Transient Response

APPLICATIONS INFORMATION

Basic Circuit Operation

The LM317M is a three-terminal floating regulator. In operation, the LM317M develops and maintains a nominal 1.25 V reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by R_1 (see Figure 19), and this constant current flows through R_2 to ground. The regulated output voltage is given by:

$$V_{out} = V_{ref} \left(1 + \frac{R_2}{R_1} \right) + I_{Adj} R_2$$

Since the current from the terminal (I_{Adj}) represents an error term in the equation, the LM317M was designed to control I_{Adj} to less than 100 μ A and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM317M is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.

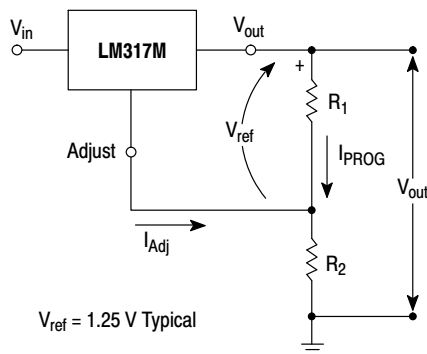


Figure 19. Basic Circuit Configuration

Load Regulation

The LM317M is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R_1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R_2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

External Capacitors

A 0.1 μ F disc or 1.0 μ F tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{Adj}) prevents ripple from being amplified as the output voltage is increased. A 10 μ F capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 V application.

Although the LM317M is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitor (C_O) in the form of a 1.0 μ F tantalum or 25 μ F aluminum electrolytic capacitor on the output swamps this effect and insures stability.

Protection Diodes

When external capacitors are used with any IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 20 shows the LM317M with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values ($C_O > 25 \mu$ F, $C_{Adj} > 5.0 \mu$ F). Diode D_1 prevents C_O from discharging thru the IC during an input short circuit. Diode D_2 protects against capacitor C_{Adj} discharging through the IC during an output short circuit. The combination of diodes D_1 and D_2 prevents C_{Adj} from discharging through the IC during an input short circuit.

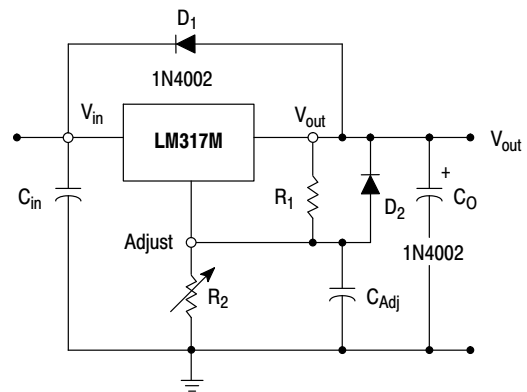


Figure 20. Voltage Regulator with Protection Diodes

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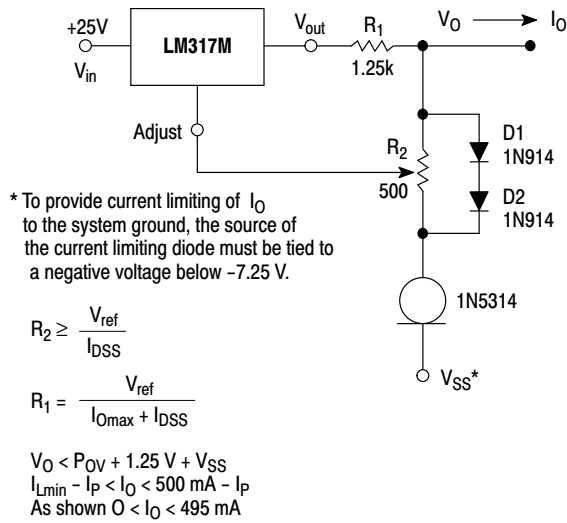
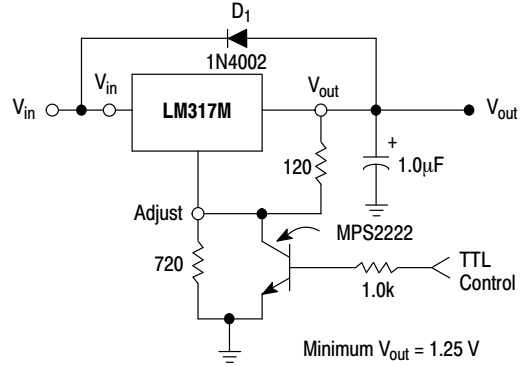


Figure 21. Adjustable Current Limiter



D_1 protects the device during an input short circuit.

Figure 22. 5 V Electronic Shutdown Regulator

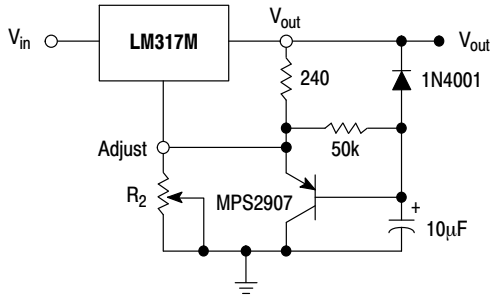


Figure 23. Slow Turn-On Regulator

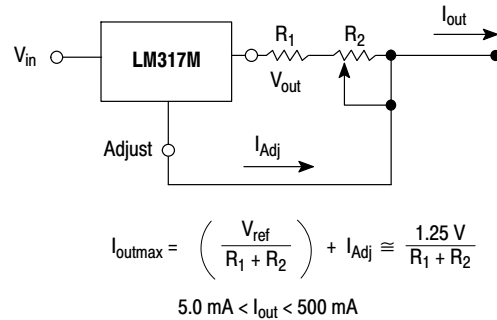


Figure 24. Current Regulator

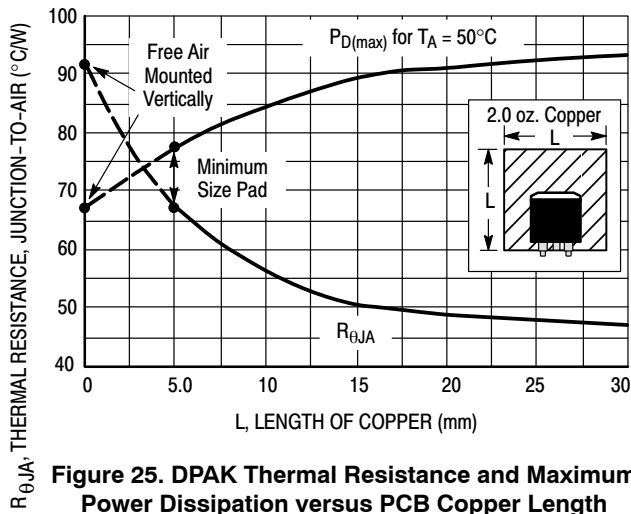


Figure 25. DPAK Thermal Resistance and Maximum Power Dissipation versus PCB Copper Length

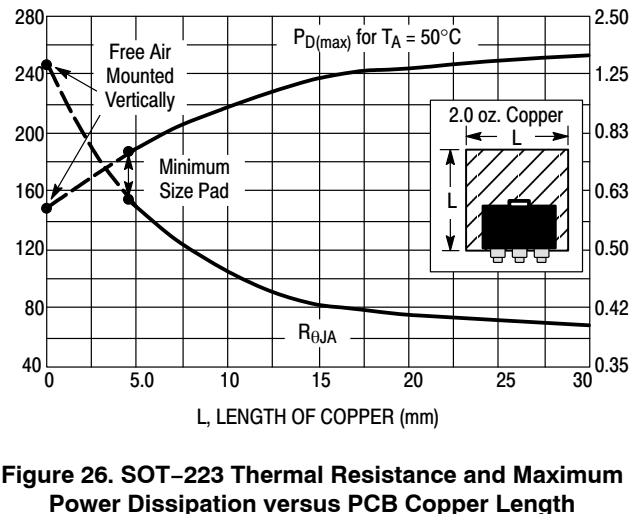


Figure 26. SOT-223 Thermal Resistance and Maximum Power Dissipation versus PCB Copper Length

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ORDERING INFORMATION

Device	Output Voltage Tolerance	Operating Temperature Range	Package	Shipping [†]	
LM317MABDTG	2%	$T_J = -40^{\circ}\text{C}$ to 125°C	DAK (Pb-Free)	75 Units / Rail	
LM317MABDTRKG			DAK (Pb-Free)	2500 / Tape & Reel	
NCV317MABDTRKG*			SOT-223 (Pb-Free)	4000 / Tape & Reel	
NCV317MABSTT3G*			TO-220 (Pb-Free)	50 Units / Rail	
LM317MABTG		$T_J = 0^{\circ}\text{C}$ to 125°C	DAK (Pb-Free)	2500 / Tape & Reel	
LM317MADTRKG			DAK (Pb-Free)	2500 / Tape & Reel	
LM317MBDTG	4%	$T_J = -40^{\circ}\text{C}$ to 125°C	DAK (Pb-Free)	75 Units / Rail	
NCV317MBDTG*			DAK (Pb-Free)	2500 / Tape & Reel	
LM317MBDTRKG			SOT-223 (Pb-Free)	4000 / Tape & Reel	
NCV317MBDTRKG*			TO-220 (Pb-Free)	50 Units / Rail	
LM317MBSTT3G			$T_J = 0^{\circ}\text{C}$ to 125°C	DAK (Pb-Free)	75 Units / Rail
NCV317MBSTT3G*				DAK (Pb-Free)	2500 / Tape & Reel
LM317MBTG		SOT-223 (Pb-Free)		4000 / Tape & Reel	
NCV317MBTG*		TO-220 (Pb-Free)		50 Units / Rail	
LM317MDTG		DAK (Pb-Free)		75 Units / Rail	
LM317MDTRKG		DAK (Pb-Free)		2500 / Tape & Reel	
LM317MSTT3G		SOT-223 (Pb-Free)		4000 / Tape & Reel	
LM317MTG		TO-220 (Pb-Free)		50 Units / Rail	

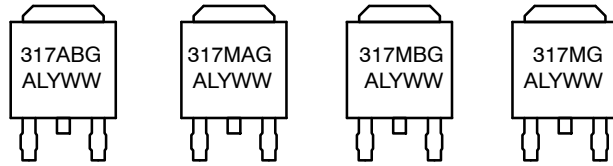
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

*NCV devices: $T_{low} = -40^{\circ}\text{C}$, $T_{high} = +125^{\circ}\text{C}$. Guaranteed by design. NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

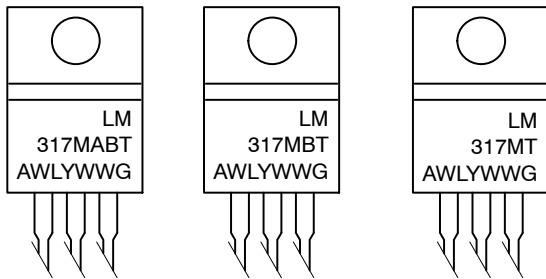
LM317M, NCV317MA, NCV317M

MARKING DIAGRAMS

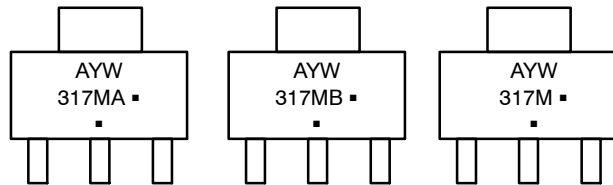
DPAK DT SUFFIX CASE 369C



TO-220 T SUFFIX CASE 221A



SOT-223 ST SUFFIX CASE 318E



A = Assembly Location
L, WL = Wafer Lot
Y = Year
WW, W = Work Week
G or ■ = Pb-Free Package
(Note: Microdot may be in either location)

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1

SOT-223 (TO-261)
CASE 318E-04
ISSUE R

DATE 02 OCT 2018



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

MILLIMETERS			
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
θ	0°	---	10°



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DESCRIPTION:	SOT-223 (TO-261)	PAGE 1 OF 2

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SOT-223 (TO-261)
CASE 318E-04
ISSUE R

DATE 02 OCT 2018

- | | | | | |
|--|---|---|---|---|
| STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR | STYLE 2:
PIN 1. ANODE
2. CATHODE
3. NC
4. CATHODE | STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN | STYLE 4:
PIN 1. SOURCE
2. DRAIN
3. GATE
4. DRAIN | STYLE 5:
PIN 1. DRAIN
2. GATE
3. SOURCE
4. GATE |
| STYLE 6:
PIN 1. RETURN
2. INPUT
3. OUTPUT
4. INPUT | STYLE 7:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2
4. CATHODE | STYLE 8:
CANCELLED | STYLE 9:
PIN 1. INPUT
2. GROUND
3. LOGIC
4. GROUND | STYLE 10:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE |
| STYLE 11:
PIN 1. MT 1
2. MT 2
3. GATE
4. MT 2 | STYLE 12:
PIN 1. INPUT
2. OUTPUT
3. NC
4. OUTPUT | STYLE 13:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR | | |

**GENERIC
 MARKING DIAGRAM***



- A = Assembly Location
- Y = Year
- W = Work Week
- XXXXX = Specific Device Code
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	SOT-223 (TO-261)	PAGE 2 OF 2

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MECHANICAL CASE OUTLINE

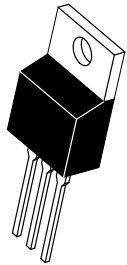
PACKAGE DIMENSIONS

ON Semiconductor®

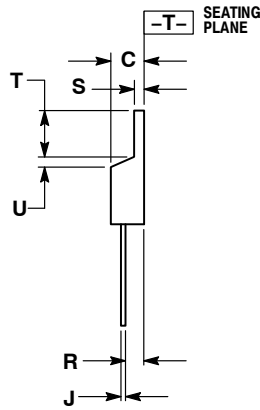
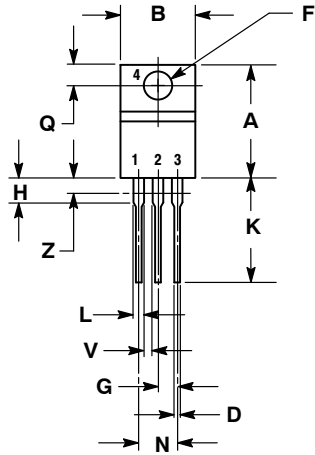


TO-220, SINGLE GAUGE CASE 221AB-01 ISSUE A

DATE 16 NOV 2010



SCALE 1:1



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. PRODUCT SHIPPED PRIOR TO 2008 HAD DIMENSIONS S = 0.045 - 0.055 INCHES (1.143 - 1.397 MM)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.020	0.024	0.508	0.61
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 1:

- PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:

- PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

STYLE 3:

- PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 4:

- PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

STYLE 5:

- PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 6:

- PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 7:

- PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

STYLE 8:

- PIN 1. CATHODE
2. ANODE
3. EXTERNAL TRIP/DELAY
4. ANODE

STYLE 9:

- PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 10:

- PIN 1. GATE
2. SOURCE
3. DRAIN
4. SOURCE

STYLE 11:

- PIN 1. DRAIN
2. SOURCE
3. GATE
4. SOURCE

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DESCRIPTION:	TO-220, SINGLE GAUGE	PAGE 1 OF 1

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1

DPAK (SINGLE GAUGE)

CASE 369C

ISSUE F

DATE 21 JUL 2015



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

GENERIC MARKING DIAGRAM*

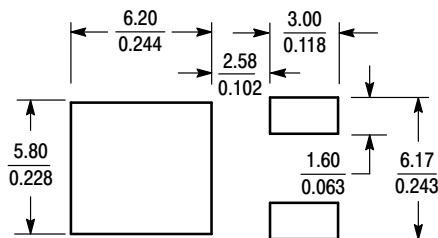


- XXXXXX = Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

- | | | | | |
|--|--|---|---|--|
| <p>STYLE 1:</p> <p>PIN 1. BASE</p> <p>2. COLLECTOR</p> <p>3. EMITTER</p> <p>4. COLLECTOR</p> | <p>STYLE 2:</p> <p>PIN 1. GATE</p> <p>2. DRAIN</p> <p>3. SOURCE</p> <p>4. DRAIN</p> | <p>STYLE 3:</p> <p>PIN 1. ANODE</p> <p>2. CATHODE</p> <p>3. ANODE</p> <p>4. CATHODE</p> | <p>STYLE 4:</p> <p>PIN 1. CATHODE</p> <p>2. ANODE</p> <p>3. GATE</p> <p>4. ANODE</p> | <p>STYLE 5:</p> <p>PIN 1. GATE</p> <p>2. ANODE</p> <p>3. CATHODE</p> <p>4. ANODE</p> |
| <p>STYLE 6:</p> <p>PIN 1. MT1</p> <p>2. MT2</p> <p>3. GATE</p> <p>4. MT2</p> | <p>STYLE 7:</p> <p>PIN 1. GATE</p> <p>2. COLLECTOR</p> <p>3. EMITTER</p> <p>4. COLLECTOR</p> | <p>STYLE 8:</p> <p>PIN 1. N/C</p> <p>2. CATHODE</p> <p>3. ANODE</p> <p>4. CATHODE</p> | <p>STYLE 9:</p> <p>PIN 1. ANODE</p> <p>2. CATHODE</p> <p>3. RESISTOR ADJUST</p> <p>4. CATHODE</p> | <p>STYLE 10:</p> <p>PIN 1. CATHODE</p> <p>2. ANODE</p> <p>3. CATHODE</p> <p>4. ANODE</p> |

SOLDERING FOOTPRINT*



SCALE 3:1 (mm / inches)

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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