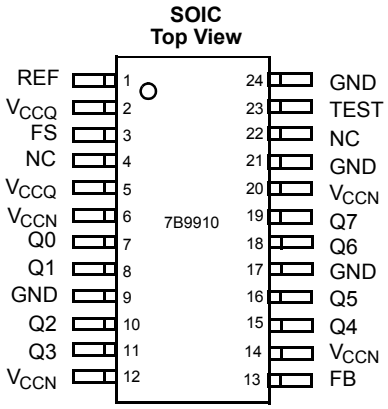
Contents

Pinouts

Figure 1. 24-pin SOIC pinout



Pin Definitions

Signal Name	I/O	Description
REF[1]	I	Reference frequency input. This input supplies the frequency and timing against which all functional variations are measured.
FB	I	PLL feedback input (typically connected to one of the eight outputs).
FS[1, 2, 3]	I	Three level frequency range select. The ranges are described in the switching characteristics tables.
TEST	I	Three level select. See Test Mode.
Q[0..7]	O	Clock outputs.
NC	NC	No connect.
V_{CCN}	PWR	Power supply for output drivers.
V_{CCQ}	PWR	Power supply for internal circuitry.
GND	PWR	Ground.

Test Mode

The TEST input is a three level input. In normal system operation, this pin is connected to ground, allowing the CY7B9910 to operate as described in Block Diagram Description on page 1. For testing purposes, any of the three level inputs can have a removable jumper to ground or be tied LOW through a 100 Ω resistor. This enables an external tester to change the state of these pins.

If the TEST input is forced to its MID or HIGH state, the device operates with its internal phase locked loop disconnected and input levels supplied to REF directly control all outputs. Relative output-to-output functions are the same as in normal mode.

Notes
1. When the FS pin is selected HIGH, the REF input must not transition upon power up until V_{CC} reached 4.3 V.
2. The level to be set on FS is determined by the “normal” operating frequency (f_{NOM}) of the VCO (see Logic Block Diagram). The frequency appearing at the REF and FB inputs are f_{NOM} when the output connected to FB is undivided. The frequency of the REF and FB inputs are f_{NOM} / X when the device is configured for a frequency multiplication by using external division in the feedback path of value X.
3. For all three state inputs, HIGH indicates a connection to V_{CC}, LOW indicates a connection to GND, and MID indicates an open connection. Internal termination circuitry holds an unconnected input to V_{CC} / 2.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage to ground potential .....–0.5 V to +7.0 V

DC input voltage .....–0.5 V to +7.0 V

Output current into outputs (LOW) ..... 64 mA

Static discharge voltage (MIL-STD-883, method 3015) ..... > 2001 V

Latch-up current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0 °C to +70 °C	5 V ± 10%
Industrial	–40 °C to +85 °C	5 V ± 10%

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	CY7B9910		Unit
			Min	Max	
V_{OH}	Output HIGH voltage	V_{CC} = Min, I_{OH} = –16 mA	2.4	–	V
		V_{CC} = Min, I_{OH} = –40 mA	–	–	
V_{OL}	Output LOW voltage	V_{CC} = Min, I_{OL} = 46 mA	–	0.45	V
		V_{CC} = Min, I_{OL} = 46 mA	–	–	
V_{IH}	Input HIGH voltage (REF and FB inputs only)		2.0	V_{CC}	V
V_{IL}	Input LOW voltage (REF and FB inputs only)		–0.5	0.8	V
V_{IHH}	Three level input HIGH voltage (Test, FS)[4]	Min ≤ V_{CC} ≤ Max	V_{CC} – 1	V_{CC}	V
V_{IMM}	Three level input MID voltage (Test, FS)[4]	Min ≤ V_{CC} ≤ Max	(V_{CC}/2) – 0.5	(V_{CC}/2) + 0.5	V
V_{ILL}	Three level input LOW voltage (Test, FS)[4]	Min ≤ V_{CC} ≤ Max	0.0	1.0	V

Note

4. These inputs are normally wired to V_{CC}, GND, or left unconnected (actual threshold voltages vary as a percentage of V_{CC}). Internal termination resistors hold unconnected inputs at V_{CC} / 2. If these inputs are switched, the function and timing of the outputs may glitch and the PLL may require an additional t_{LOCK} time before all datasheet limits are achieved.

Electrical Characteristics *(continued)*

Over the Operating Range

Parameter	Description	Test Conditions		CY7B9910 Min	CY7B9910 Max	Unit
I_{IH}	Input HIGH leakage current (REF and FB inputs only)	V_{CC} = Max, V_{IN} = Max		–	10	µA
I_{IL}	Input LOW leakage current (REF and FB inputs only)	V_{CC} = Max, V_{IN} = 0.4 V		–500	–	µA
I_{IHH}	Input HIGH current (Test, FS)	$V_{IN} = V_{CC}$		–	200	µA
I_{IMM}	Input MID current (Test, FS)	$V_{IN} = V_{CC} / 2$		–50	50	µA
I_{ILL}	Input LOW current (Test, FS)	V_{IN} = GND		–	–200	µA
I_{OS}	Output short circuit current[5]	V_{CC} = Max, V_{OUT} = GND (25 °C only)		–	–250	mA
I_{CCQ}	Operating current used by internal circuitry	$V_{CCN} = V_{CCQ}$ = Max All input selects open	Commercial	–	85	mA
			Industrial	–	90	
I_{CCN}	Output buffer current per output pair[6]	$V_{CCN} = V_{CCQ}$ = Max I_{OUT} = 0 mA Input selects open, f_{MAX}		–	14	mA
PD	Power dissipation per output pair[7]	$V_{CCN} = V_{CCQ}$ = Max I_{OUT} = 0 mA Input selects open, f_{MAX}		–	78	mW

Notes

5. Tested one output at a time, output shorted for less than one second, less than 10% duty cycle. Room temperature only.
6. Total output current per output pair is approximated by the following expression that includes device current plus load current:
   CY7B9910:
   ICCN = [(4 + 0.11 F) + [((835 – 3 F) / Z) + (.0022 FC)] N] x 1.1

   Where
   F = frequency in MHz
   C = capacitive load in pF
   Z = line impedance in ohms
   N = number of loaded outputs; 0, 1, or 2
   FC = F × C.
7. Total power dissipation per output pair is approximated by the following expression that includes device power dissipation plus power dissipation due to the load circuit:
   CY7B9910:
   PD = [(22 + 0.61 F) + [((1550 – 2.7 F) / Z) + (.0125 FC)] N] x 1.1
   See note 3 for variable definition.
8. CMOS output buffer current and power dissipation specified at 50 MHz reference frequency.

Capacitance

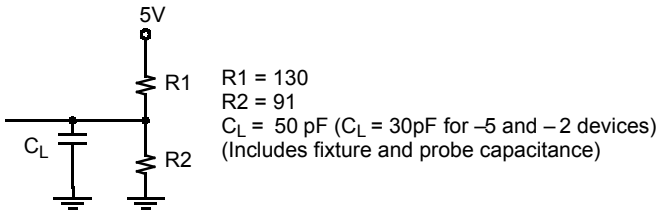
Parameter [9, 10]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 5.0 V	10	pF

Thermal Resistance

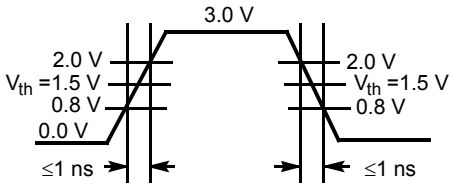
Parameter [10]	Description	Test Conditions	24-pin SOIC Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, according to EIA/JESD51.	64	°C/W
Θ_{JC}	Thermal resistance (junction to case)		28	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



TTL AC Test Load (CY7B9910)



TTL Input Test Waveform (CY7B9910)

Notes
9. Applies to REF and FB inputs only.
10. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics

Over the Operating Range

Parameter [11]	Description		CY7B9910-5			Unit
			Min	Typ	Max	
f_{NOM}	Operating clock frequency in MHz	FS = LOW[12, 13]	15	–	30	MHz
		FS = MID[12, 13]	25	–	50	
		FS = HIGH[12, 13, 14]	40	–	80	
t_{RPWH}	REF pulse width HIGH		5.0	–	–	ns
t_{RPWL}	REF pulse width LOW		5.0	–	–	ns
t_{SKEW}	Zero output skew (All outputs)[16, 17]		–	0.25	0.5	ns
t_{DEV}	Device-to-device skew[18, 19]		–	–	1.0	ns
t_{PD}	Propagation delay, REF rise to FB rise		–0.5	0.0	+0.5	ns
t_{ODCV}	Output duty cycle variation[20]		–1.0	0.0	+1.0	ns
t_{ORISE}	Output rise time[21, 22]		0.15	1.0	1.5	ns
t_{OFALL}	Output fall time[21, 22]		0.15	1.0	1.5	ns
t_{LOCK}	PLL lock time[23]		–	–	0.5	ms
t_{JR}	Cycle-to-cycle output jitter	Peak-to-peak[18]	–	–	200	ps
		RMS[18]	–	–	25	ps

Notes

11. Test measurement levels for the CY7B9910 is TTL level (1.5 V to 1.5 V). Test conditions assume signal transition times of 2 ns or less and output loading as shown in the AC Test Loads and Waveforms unless otherwise specified.
12. For all three state inputs, HIGH indicates a connection to V_{CC}, LOW indicates a connection to GND, and MID indicates an open connection. Internal termination circuitry holds an unconnected input to V_{CC} / 2.
13. The level to be set on FS is determined by the “normal” operating frequency (f_{NOM}) of the VCO (see Logic Block Diagram). The frequency appearing at the REF and FB inputs are f_{NOM} when the output connected to FB is undivided. The frequency of the REF and FB inputs are f_{NOM} / X when the device is configured for a frequency multiplication by using external division in the feedback path of value X.
14. When the FS pin is selected HIGH, the REF input must not transition upon power up until V_{CC} reached 4.3 V.
15.
16. t_{SKEW} is defined as the time between the earliest and the latest output transition among all outputs when all are loaded with 50 pF and terminated with 50 Ω to 2.06 V (CY7B9910)
17. t_{SKEW} is defined as the skew between outputs.
18. Guaranteed by statistical correlation. Tested initially and after any design or process changes that may affect these parameters.
19. t_{DEV} is the output-to-output skew between any two outputs on separate devices operating under the same conditions (V_{CC}, ambient temperature, air flow, and so on).
20. t_{ODCV} is the deviation of the output from a 50% duty cycle.
21. Specified with outputs loaded with 30 pF for the CY7B9910–2 and –5 devices and 50 pF for the CY7B9910–7 devices. Devices are terminated through 50 Ω to 2.06 V (CY7B9910)
22. t_{ORISE} and t_{OFALL} measured between 0.8 V and 2.0 V for the CY7B9910
23. t_{LOCK} is the time that is required before synchronization is achieved. This specification is valid only after V_{CC} is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until t_{PD} is within specified limits.

AC Timing Diagrams

Figure 3. AC Timing Diagrams

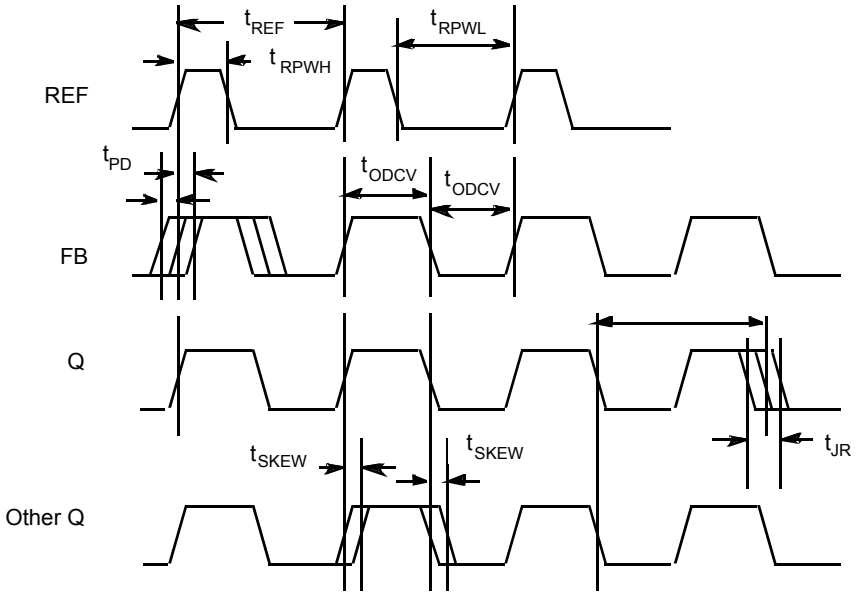
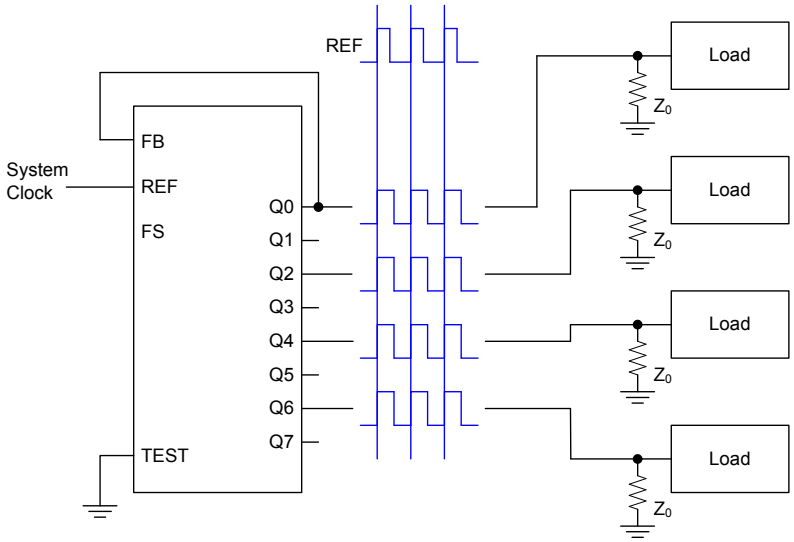


Figure 4. Zero Skew and Zero Delay Clock Driver

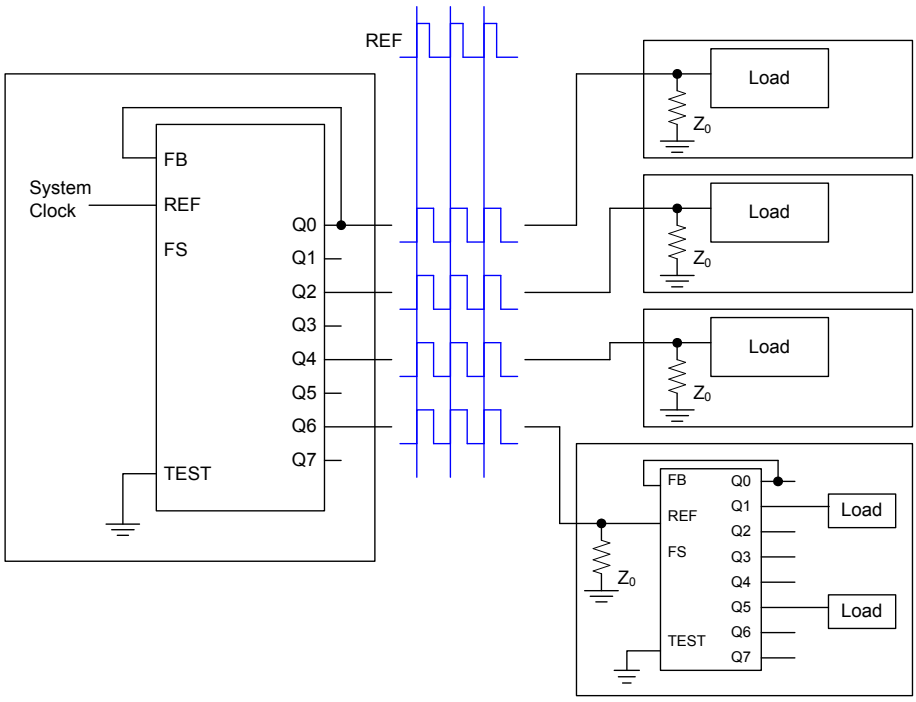


Operational Mode Descriptions

Figure 4 on page 8 shows the device configured as a zero skew clock buffer. In this mode the CY7B9910 is used as the basis for a low skew clock distribution tree. The outputs are aligned and may each drive a terminated transmission line to an independent load. The FB input is tied to any output and the operating frequency range is selected with the FS pin. The low skew specification, coupled with the ability to drive terminated transmission lines (with impedances as low as 50 ohms), enables efficient printed circuit board design.

Figure 3 on page 8 shows the CY7B9910 connected in series to construct a zero skew clock distribution tree between boards. Cascaded clock buffers accumulates low frequency jitter because of the non-ideal filtering characteristics of the PLL filter. Do not connect more than two clock buffers in series.

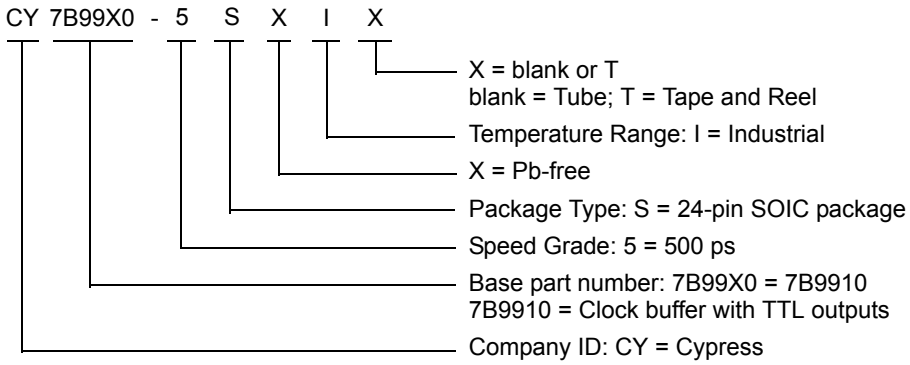
Figure 5. Board-to-Board Clock Distribution



Ordering Information

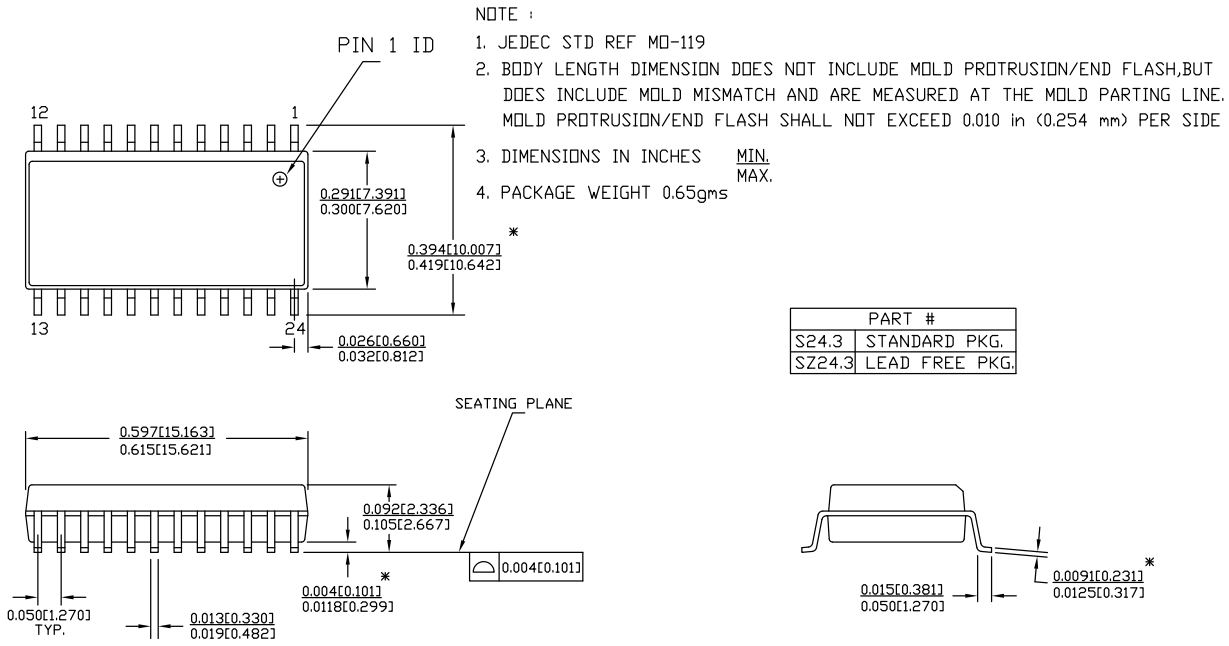
Accuracy (ps)	Ordering Code	Package Type	Operating Range
Pb-free			
500	CY7B9910-5SXI	24-pin Small Outline IC	Industrial, –40 °C to +85 °C
	CY7B9910-5SXIT	24-pin Small Outline IC – Tape and Reel	Industrial, –40 °C to +85 °C

Ordering Code Definitions



Package Diagram

Figure 6. 24-pin SOIC (0.615 × 0.300 × 0.0932 Inches) Package Outline, 51-85025



Acronyms

Acronym	Description
FB	Feedback
PLL	Phase-Locked Loop
SOIC	Small-Outline Integrated Circuit
VCO	Voltage Controlled Oscillator

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kΩ	kilohm
MHz	megahertz
µA	microampere
mA	milliampere
ms	millisecond
mW	milliwatt
ns	nanosecond
Ω	ohm
ppm	parts per million
%	percent
pF	picofarad
ps	picosecond
V	volt

Document History Page

Document Title: CY7B9910, Low Skew Clock Buffer Document Number: 38-07135				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	110244	SZV	10/28/01	Change from Specification number: 38-00437 to 38-07135.
*A	1199925	DPF / AESA	See ECN	Updated Ordering Information: Added Pb-free parts in Ordering Information. Added Note “Not recommended for the new design” and referred the same note in CY7B9920-2SC, CY7B9910-7SI, CY7B9920-7SC, CY7B9920-7SI.
*B	1353343	AESA	See ECN	Change status from Preliminary to Final.
*C	2750166	TSAI	08/10/09	Post to external web.
*D	2761988	CXQ	09/10/09	Updated Test Mode: Fixed typo (Replaced 100 W resistor with 100 Ω resistor). Updated Ordering Information: Referred Note “Not recommended for new designs” in CY7B9910-2SC, CY7B9910-2SCT, CY7B9910-5SC, CY7B9910-5SCT, CY7B9920-5SC, CY7B9920-5SCT, CY7B9920-5SI, CY7B9910-7SC. Fixed incorrect instances (Replaced “Pb” with “Pin”).
*E	2896073	CXQ	03/19/10	Updated Ordering Information: Removed inactive parts. Updated Package Diagram.
*F	3010397	KVM	08/18/2010	Added Ordering Code Definitions.
*G	3047620	BASH	10/07/2010	Updated Ordering Information: Removed pruned parts. Removed associated tables.
*H	4163293	CINM	10/17/2013	Updated Package Diagram: spec 51-85025 – Changed revision from *D to *E. Updated to new template. Completing Sunset Review.
*I	4416541	AJU	06/23/2014	Updated Ordering Information: No change in part numbers. Removed the Note “Not recommended for new design. New designs should use Pb-free devices.” and its reference in “CY7B9920-5SI”. Added “Not Recommended for New Designs” against the MPN “CY7B9920-5SI”. Updated Package Diagram: spec 51-85025 – Changed revision from *E to *F.
*J	4570101	AJU	11/14/2014	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end.
*K	5270360	PSR	05/13/2016	Updated Electrical Characteristics: Updated Note 6 (Replaced “FC = F < C” with “FC = F × C”). Added Thermal Resistance. Updated to new template.
*L	5493470	XHT	11/04/2016	Updated Document Title to read as “CY7B9910, Low Skew Clock Buffer”. Removed CY7B9920 part related information in all instances across the document. Updated Ordering Information: Updated part numbers. Updated to new template. Completing Sunset Review.
*M	5975902	AESATMP9	11/24/2017	Updated logo and copyright.

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