Quad, Rail-to-Rail, Fault-Protected, SPST Analog Switches

ABSOLUTE MAXIMUM RATINGS

(Voltages Referenced to GND)
V+ .....-0.3V to +44.0V
V- .....-44.0V to +0.3V
V+ to V-.....-0.3V to +44.0V
COM_, IN_ (Note 1) .....(V- - 0.3V) to (V+ + 0.3V)
NC_, NO_ (Note 2).....(V+ - 36V) to (V- + 36V)
NC_, NO_ to COM_ .....-36V to +36V
Continuous Current into Any Terminal.....±30mA
Peak Current into Any Terminal
(pulsed at 1ms, 10% duty cycle).....±50mA

Continuous Power Dissipation (T_A = +70°C) (Note 2)
Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
Narrow SO (derate 8.70mW/°C above +70°C) 696mW
TSSOP (derate 9.4mW/°C above +70°C) 754.7mW
CERDIP (derate 10.00mW/°C above +70°C).....800mW
Operating Temperature Ranges
MAX451_C_ E .....0°C to +70°C
MAX451_E_ E .....-40°C to +85°C
MAX451_MJE .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: COM_ and IN_ pins are not fault protected. Signals on COM_ or IN_ exceeding V+ or V- are clamped by internal diodes. Limit forward diode current to maximum current rating.

Note 2: NC_ and NO_ pins are fault protected. Signals on NC_ or NO_ exceeding -36V to +36V may damage the device. These limits apply with power applied to V+ or V-, or ±40V with V+ = V- = 0.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = +15V, V- = -15V, GND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 3)	MAX	UNITS
ANALOG SWITCH							
Fault-Protected Analog Signal Range	$V_{NO\_}$, $V_{NC\_}$	Applies with power on or off (Note 2)	C, E, M	-36		36	V
Fault-Free Analog Signal Range	$V_{NO\_}$, $V_{NC\_}$	Applies with power on or off (Note 2)	C, E, M	V-		V+	V
Non-Protected Analog Signal Range (COM_ Output)	$V_{COM\_}$	Applies with power on or off (Note 1)	C, E, M	V- - 0.3		V+ + 0.3	V
COM_ -NO_ or COM_ -NC_ On-Resistance	R_{ON}	$V_{COM\_}$ = ±10V, $I_{COM\_}$ = 1mA	+25°C		125	160	Ω
			C, E			200	
			M			250	
COM_ -NO_ or COM_ -NC_ On-Resistance Match Between Channels (Note 4)	ΔR_{ON}	$V_{COM\_}$ = ±10V, $I_{COM\_}$ = 1mA	+25°C		3	6	Ω
			C, E			10	
			M			15	
NO_ or NC_ Off Leakage Current (Note 5)	$I_{NO\_(OFF)}$, $I_{NC\_(OFF)}$	$V_{COM\_}$ = ±14V; $V_{NO\_}$, V_{COM} = ∓14V	+25°C	-0.5	0.01	0.5	nA
			C, E	-10		10	
			M	-200		200	
COM_ Off Leakage Current (Note 5)	$I_{COM\_(OFF)}$	$V_{COM\_}$ = ±14V; $V_{NO\_}$, V_{COM} = ∓14V	+25°C	-0.5	0.01	0.5	nA
			C, E	-10		10	
			M	-200		200	
COM_ On Leakage Current (Note 5)	$I_{COM\_(ON)}$	$V_{COM\_}$ = ±14V	+25°C	-0.5	0.01	0.5	nA
			C, E	-20		20	
			M	-400		400	

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = +15V, V- = -15V, GND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 3)	MAX	UNITS
FAULT (V+ = +15V, V- = -15V, unless otherwise noted.)							
COM_ Output Leakage Current, Supplies On	$I_{COM\_}$	$V_{NO\_}$ or $V_{NC\_}$ = ±33V	+25°C	-10		10	nA
			C, E	-200		200	
			M	-1		1	µA
NO_ or NC_ Off Input Leakage Current, Supplies On	$I_{NO\_}$, $I_{NC\_}$	$V_{NO\_}$ or $V_{NC\_}$ = ±25V, $V_{COM\_}$ = ∓ 10V	+25°C	-20		20	nA
			C, E	-200		200	
			M	-10		10	µA
NO_ or NC_ Input Leakage Current, Supplies Off	$I_{NO\_}$, $I_{NC\_}$	$V_{NO\_}$ or $V_{NC\_}$ = ±40V, V+ = 0, V- = 0	+25°C	-20	0.1	20	nA
			C, E	-200		200	
			M	-10		10	µA
COM_ On Output Current, Supplies On	$I_{COM\_}$	$V_{NO\_}$ or $V_{NC\_}$ = 33V	+25°C	8	11	13	mA
		$V_{NO\_}$ or $V_{NC\_}$ = -33V		-12	-10	-7	
COM_ On Output Resistance, Supplies On	$R_{COM\_}$	$V_{NO\_}$ or $V_{NC\_}$ = ±33V	+25°C		1	2.5	kΩ
			C, E, M			3	
LOGIC INPUT							
IN_ Input Logic Threshold High	V_{IN_H}		C, E, M		1.9	2.4	V
IN_ Input Logic Threshold Low	V_{IN_L}		C, E, M	0.8	1.9		V
IN_ Input Current Logic High or Low	$I_{INH\_}$, I_{INL}	$V_{IN\_}$ = 0.8V or 2.4V	+25°C	-1	0.03	1	µA
			C, E, M	-5		5	
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	$V_{COM\_}$ = ±10V, $R_{L\_}$ = 2kΩ, Figure 2	+25°C		350	500	ns
			C, E			600	
			M			900	
Turn-Off Time	t_{OFF}	$V_{COM\_}$ = ±10V, $R_{L\_}$ = 2kΩ, Figure 2	+25°C		200	400	ns
			C, E			500	
			M			750	
Break-Before-Make Time Delay (MAX4513 Only)	t_{BBM}	$V_{COM\_}$ = ±10V, $R_{L\_}$ = 2kΩ, Figure 3	+25°C	50	100		ns
Charge Injection (Note 6)	Q	C_L = 1.0nF, $V_{NO\_}$ = 0, R_S = 0Ω, Figure 4	+25°C		1.5	5	pC
NO_ or NC_ Off-Capacitance	$C_{N\_(OFF)}$	f = 1MHz, Figure 5	+25°C		10		pF
COM_ Off-Capacitance	$C_{COM\_(OFF)}$	f = 1MHz, Figure 5	+25°C		5		pF
COM_ On-Capacitance	$C_{COM\_(ON)}$	f = 1MHz, Figure 5	+25°C		10		pF
Off Isolation (Note 7)	VC_{ISO}	R_L = 50Ω, C_L = 15pF, $V_{N\_}$ = $1V_{RMS}$, f = 1MHz, Figure 6	+25°C		-62		dB
Channel-to-Channel Crosstalk (Note 9)	V_{CT}	R_L = 50Ω, C_L = 15pF, $V_{N\_}$ = $1V_{RMS}$, f = 1MHz, Figure 6	+25°C		-66		dB

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = +15V, V- = -15V, GND = 0V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 3)	MAX	UNITS
POWER SUPPLY							
Power-Supply Range	V+, V-		C,E, M	±4.5		±18	V
V+ Supply Current	I+	All $V_{IN\_}$ = 0 or 5V	+25°C		280	400	µA
			C, E, M			600	
V- Supply Current	I-	All $V_{IN\_}$ = 0 or 5V	+25°C		90	200	µA
			C, E, M			300	
GND Supply Current	I_{GND}	All $V_{IN\_}$ = 0 or 15V	+25°C	-1	0.01	1	µA
			C, E, M			10	
		All $V_{IN\_}$ = 5V	+25°C		150	250	µA
			C, E, M			450	

ELECTRICAL CHARACTERISTICS—Single +12V Supply

(V+ = +10.8V to +13.2V, V- = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 3)	MAX	UNITS
ANALOG SWITCH							
Fault-Protected Analog Signal Range	$V_{NO\_}$, $V_{NC\_}$	Applies with power on or off (Note 2)	C, E, M	-36		36	V
Fault-Free Analog Signal Range	$V_{NO\_}$, $V_{NC\_}$	Applies with power on or off (Note 2)	C, E, M	0		V+	V
Non-Protected Analog Signal Range (COM_ Output)	$V_{COM\_}$	Applies with power on or off (Note 1)	C, E, M	-0.3		V+ + 0.3	V
COM_ -NO_ or COM_ -NC_ On-Resistance	R_{ON}	V+ = 12V, $V_{COM\_}$ = 10V, $I_{COM\_}$ = 1mA	+25°C		260	390	Ω
			C, E			450	
			M			525	
COM_ -NO_ or COM_ -NC_ On-Resistance Match Between Channels (Note 4)	ΔR_{ON}	V+ = 12V, $V_{COM\_}$ = 10V, $I_{COM\_}$ = 1mA	+25°C		4	10	Ω
			C, E			20	
			M			30	
NO_ or NC_ Off Leakage Current (Notes 5, 9)	$I_{ON\_(OFF)}$, $I_{NC\_(OFF)}$	V+ = 12V; $V_{COM\_}$ = 10V; $V_{NO\_}$, V_{NC} = 0 or 12V	+25°C	-0.5	0.01	0.5	nA
			C, E	-10		10	
			M	-200		200	
COM_ Off Leakage Current (Notes 5, 9)	$I_{COM\_(OFF)}$	V+ = 12V; $V_{COM\_}$ = 0; $V_{NO\_}$, $V_{NC\_}$ = 12V	+25°C	-0.5	0.01	0.5	nA
			C, E	-10		10	
			M	-200		200	
COM_ On Leakage Current (Notes 5, 9)	$I_{COM\_(ON)}$	V+ = 12V, $V_{COM\_}$ = 10V or 12V	+25°C	-0.5	0.01	0.5	nA
			C, E	-20		20	
			M	-400		400	
FAULT							
COM_ Output Leakage Current, Supply On	$I_{COM\_}$	$V_{NO\_}$ or $V_{NC\_}$ = ±30V, V+ = 12V	+25°C	-10		10	nA
			C, E	-200		200	
			M	-1		1	µA
NO_ or NC_ Off Input Leakage Current, Supply On	$I_{NO\_}$, $I_{NC\_}$	$V_{NO\_}$ or $V_{NC\_}$ = ±25V, $V_{COM\_}$ = 0, V+ = 12V	+25°C	-20		20	nA
			C, E	-200		200	
			M	-10		10	µA
NO_ or NC_ Input Leakage Current, Supply Off	$I_{NO\_}$, $I_{NC\_}$	$V_{NO\_}$ or $V_{NC\_}$ = ±40V, V+ = 0, V- = 0	+25°C	-20	0.1	20	nA
			C, E	-200		200	
			M	-10		10	µA
COM_ Output Current, Supply On	$I_{COM\_}$	$V_{NO\_}$ or $V_{NC\_}$ = 25V, V+ = 12V	+25°C	2	3	5	mA
COM_ Output Resistance, Supply On	$R_{COM\_}$	$V_{NO\_}$ or $V_{NC\_}$ = 10V V+ = 12V	+25°C		2.4	5	kΩ

Quad, Rail-to-Rail, Fault-Protected, SPST Analog Switches

ELECTRICAL CHARACTERISTICS—Single +12V Supply (continued)

(V+ = +10.8V to +13.2V, V- = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 3)	MAX	UNITS
LOGIC INPUT							
IN_ Input Logic Threshold High	V_{IN_H}		C, E, M		1.8	2.4	V
IN_ Input Logic Threshold Low	V_{IN_L}		C, E, M	0.8	1.8		V
IN_ Input Current Logic High or Low	I_{IN_H}, I_{IN_L}	$V_{IN\_}$ = 0.8V or 2.4V	+25°C	-1	0.03	1	µA
			C, E, M	-5		5	
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	$V_{COM\_}$ = 10V, $R_{L\_}$ = 2kΩ, Figure 2	+25°C		500	1000	ns
			C, E, M			1500	
Turn-Off Time	t_{OFF}	$V_{COM\_}$ = 10V, $R_{L\_}$ = 2kΩ, Figure 2	+25°C		400	900	ns
			C, E, M			1200	
Break-Before-Make Time Delay (MAX4513 Only)	t_{BBM}	$V_{COM\_}$ = 10V, $R_{L\_}$ = 2kΩ, Figure 3	+25°C	50	100		ns
Charge Injection (Note 6)	Q	C_L = 1.0nF, $V_{NO\_}$ = 0, R_S = 0Ω, Figure 4	+25°C		1	5	pC
NO_ or NC_ Off Capacitance	$C_{N\_(OFF)}$	f = 1MHz, Figure 5	+25°C		9		pF
COM_ Off Capacitance	$C_{COM\_(OFF)}$	$V_{COM\_}$ = GND, f = 1MHz, Figure 5	+25°C		9		pF
COM_ On Capacitance	$C_{COM\_(ON)}$	$V_{COM\_}$ = $V_{NO\_}$ = GND, f = 1MHz, Figure 5	+25°C		22		pF
Off Isolation (Note 7)	V_{ISO}	R_L = 50Ω, C_L = 15pF, $V_{N\_}$ = $1V_{RMS}$, f = 1MHz, Figure 6	+25°C		-62		dB
Channel-to-Channel Crosstalk (Note 8)	V_{CT}	R_L = 50Ω, C_L = 15pF, $V_{N\_}$ = $1V_{RMS}$, f = 1MHz, Figure 5	+25°C		-65		dB
POWER SUPPLY							
Power-Supply Range	V+		C,E, M	9		36	V
V+ Supply Current	I+	All $V_{IN\_}$ = 0 or 5V	+25°C		150	300	µA
			C, E, M			450	
V- and GND Supply Current	I_{GND}	All $V_{IN\_}$ = 0 or 12V	+25°C		50	100	µA
			C, E, M			200	
		All $V_{IN\_}$ = 5V	+25°C		150	300	
			C, E, M			450	

Note 1: COM_ and IN_ pins are not fault protected. Signals on COM_ or IN_ exceeding V+ or V- are clamped by internal diodes. Limit forward diode current to maximum current rating.

Note 2: NC_ and NO_ pins are fault protected. Signals on NC_ or NO_ exceeding -36V to +36V may damage the device. These limits apply with power applied to V+ or V-, or ±40V with V+ = V- = 0.

Note 3: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

Note 4: $\Delta R_{ON} = \Delta R_{ON(MAX)} - \Delta R_{ON(MIN)}$.

Note 5: Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at T_A = +25°C.

Note 6: Guaranteed by design.

Note 7: Off isolation = 20 log10 [$V_{COM\_}$ / ($V_{NC\_}$ or $V_{NO\_}$)], $V_{COM\_}$ = output, $V_{NC\_}$ or $V_{NO\_}$ = input to off switch.

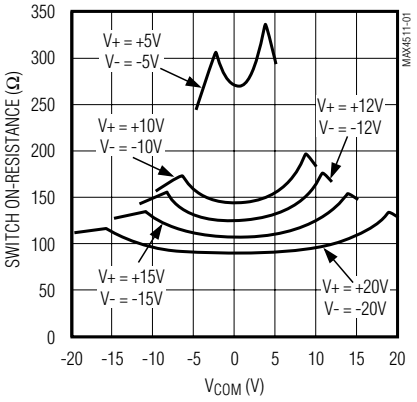
Note 8: Between any two switches.

Note 9: Leakage testing for single-supply operation is guaranteed by testing with dual supplies.

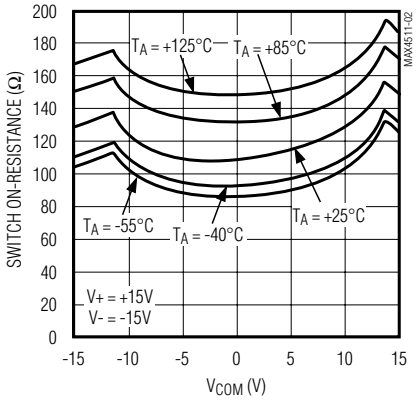
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

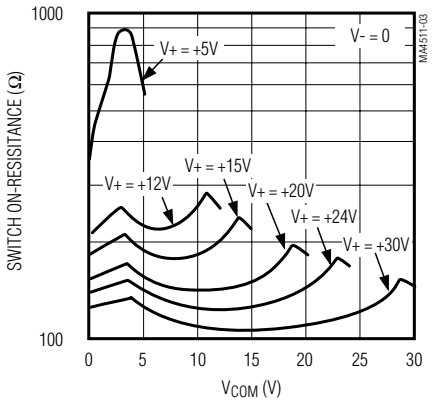
SWITCH ON-RESISTANCE vs. V_{COM} (DUAL SUPPLIES)



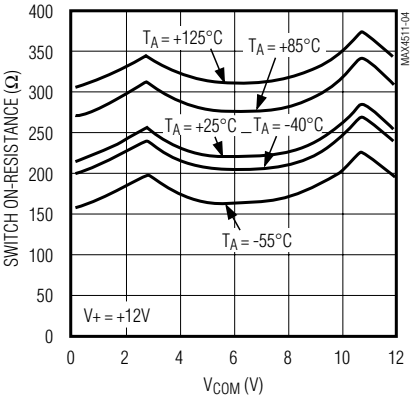
SWITCH ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (DUAL SUPPLIES)



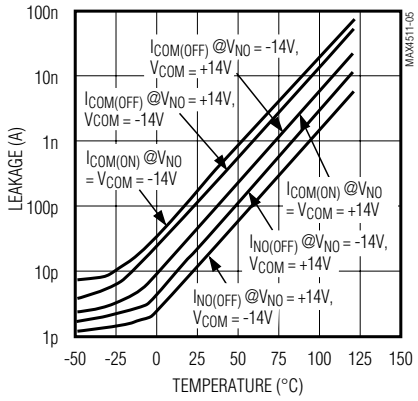
SWITCH ON-RESISTANCE vs. V_{COM} (SINGLE SUPPLY)



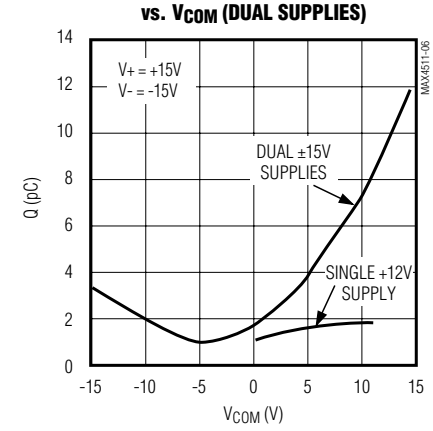
SWITCH ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (SINGLE SUPPLY)



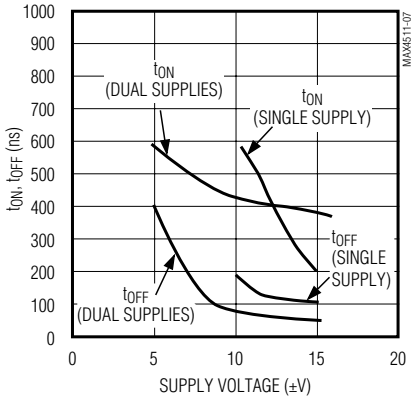
$I_{D(ON)}$, $I_{S(OFF)}$, AND $I_{D(OFF)}$ LEAKAGES vs. TEMPERATURE



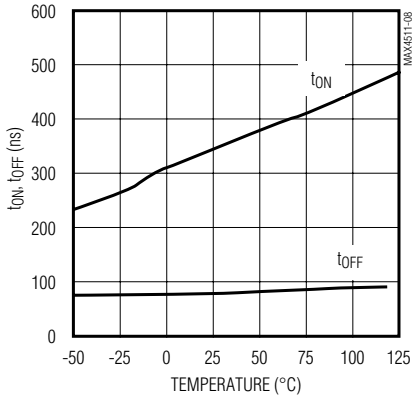
CHARGE INJECTION vs. V_{COM} (DUAL SUPPLIES)



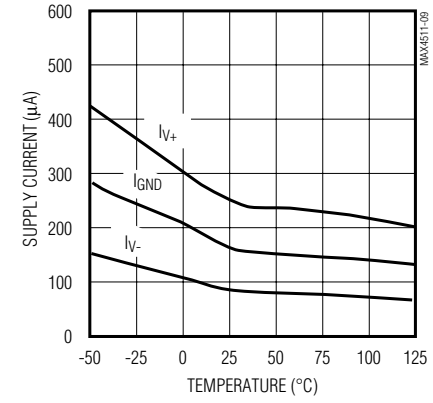
ON AND OFF TIMES vs. SUPPLY VOLTAGE



ON AND OFF TIMES vs. TEMPERATURE



POWER-SUPPLY CURRENT vs. TEMPERATURE

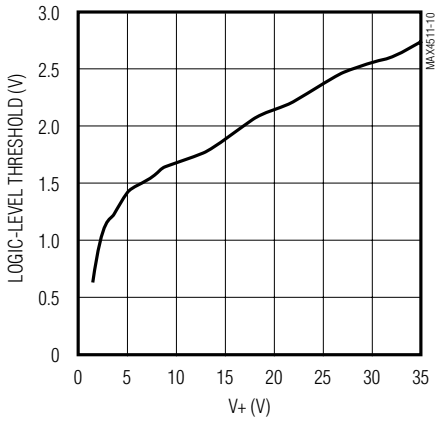


Quad, Rail-to-Rail, Fault-Protected, SPST Analog Switches

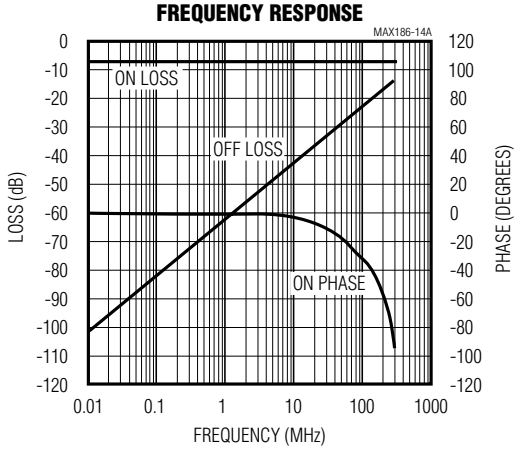
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

LOGIC-LEVEL THRESHOLD vs. V+



FREQUENCY RESPONSE



Pin Description

PIN	NAME	FUNCTION
1, 16, 9, 8	IN1–IN4	Logic Control Digital Inputs
2, 15, 10, 7	COM1–COM4	Analog Switch Common* Terminals
3, 14, 11, 6	NO1–NO4 or NC1–NC4	Analog Switch Fault-Protected Normally Open* or Normally Closed* Terminals
4	V-	Negative Analog Supply Voltage Input. Connect to GND for single-supply operation.
5	GND	Ground. Connect to digital ground. (Analog signals have no ground reference.)
12	N.C.	No Connection—not internally connected
13	V+	Positive Analog and Digital Supply-Voltage Input. Internally connected to substrate.

**As long as the voltage on NO_ or NC_ does not exceed V+ or V-, NO_ (or NC_) and COM_ pins are identical and interchangeable. Either may be considered as an input or output; signals pass equally well in either direction.*

Detailed Description

Overview of Traditional Fault-Protected Switches

The MAX4511/MAX4512/MAX4513 are fault-protected CMOS analog switches with unusual operation and construction. Traditional fault-protected switches are constructed by three series FETs. This produces good off characteristics, but fairly high on-resistance when the signals are within about 3V of each supply rail. As the voltage on one side of the switch approaches within about 3V of either supply rail (a fault condition), the switch impedance becomes higher, limiting the output signal range (on the protected side of the switch) to approximately 3V less than the appropriate polarity supply voltage.

During a fault condition, the output current that flows from the protected side of the switch into its load comes from the fault source on the other side of the switch. If the switch is open or the load is extremely high impedance, the input current will be very low. If the switch is on and the load is low impedance, enough current will flow from the source to maintain the load voltage at 3V less than the supply.

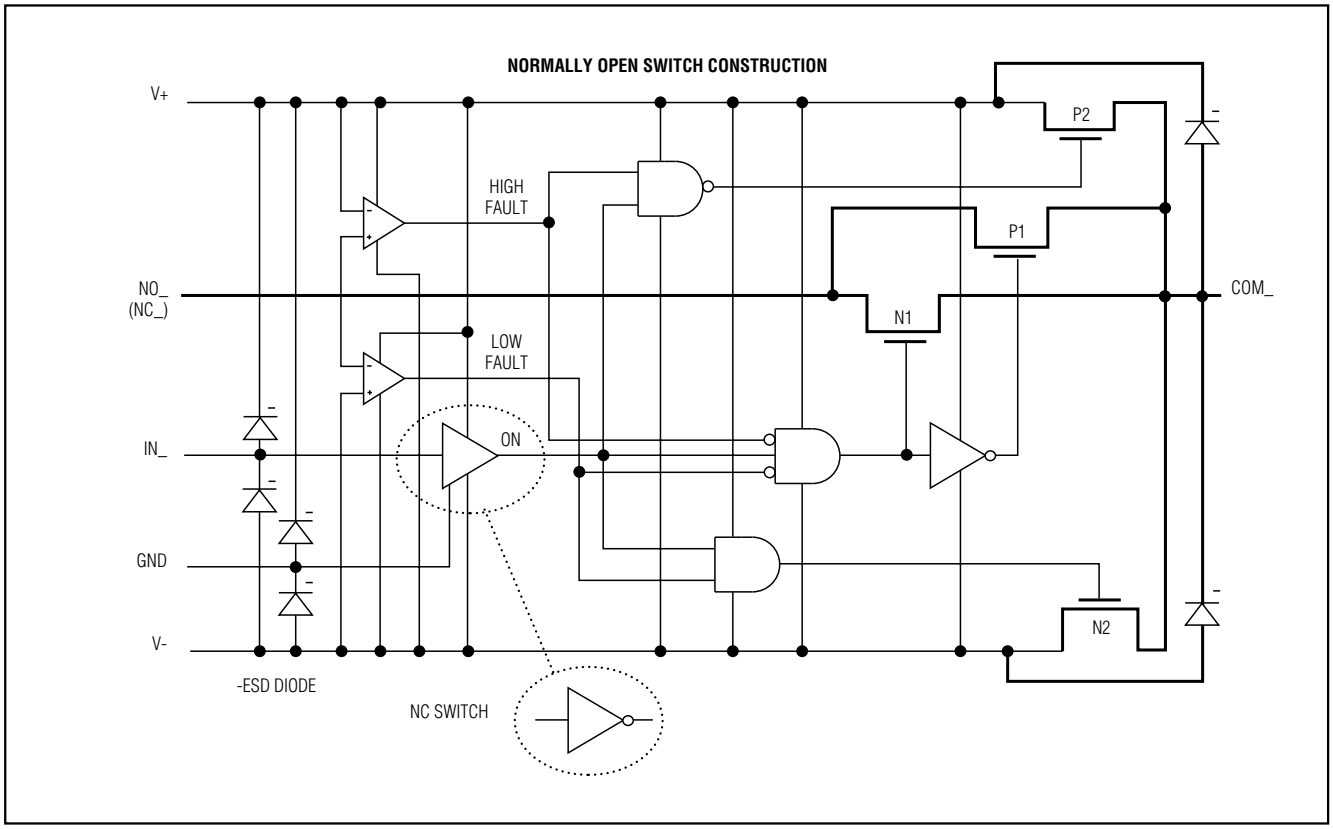


Figure 1. Block Diagram

Overview of MAX4511/MAX4512/MAX4513

The MAX4511/MAX4512/MAX4513 differ considerably from traditional fault-protection switches, with several advantages. First, they are constructed with two parallel FETs, allowing very low on-resistance when the switch is on. Second, they allow signals on the NC_ or NO_ pins that are within or slightly beyond the supply rails to be passed through the switch to the COM terminal, allowing rail-to-rail signal operation. Third, when a signal on NC_ or NO_ exceeds the supply rails by about 50mV (a fault condition), the voltage on COM_ is limited to the appropriate polarity supply voltage. Operation is identical for both fault polarities. The fault-protection extends to ±36V from GND.

During a fault condition, the NO_ or NC_ input pin becomes high impedance regardless of the switch state or load resistance. If the switch is on, the COM_ output current is furnished from the V+ or V- pin by "booster" FETs connected to each supply pin. These FETs can typically source or sink up to 10mA.

When power is removed, the fault protection is still in effect. In this case, the NO_ or NC_ terminals are a virtual open circuit. The fault can be up to ±40V.

The COM_ pins are not fault protected; they act as normal CMOS switch pins. If a voltage source is connected to any COM_ pin, it should be limited to the supply voltages. Exceeding the supply voltage will cause high currents to flow through the ESD protection diodes, possibly damaging the device (see *Absolute Maximum Ratings*).

Pin Compatibility

These switches have identical pinouts to common non-fault-protected CMOS switches. Care should be exercised in considering them for direct replacements in existing printed circuit boards, however, since only the NO_ and NC_ pins of each switch are fault protected.

Internal Construction

Internal construction is shown in Figure 1, with the analog signal paths shown in bold. A single normally open

(NO) switch is shown; the normally closed (NC) configuration is identical except the logic-level translator becomes an inverter. The analog switch is formed by the parallel combination of N-channel FET N1 and P-channel FET P1, which are driven on and off simultaneously according to the input fault condition and the logic-level state.

Normal Operation

Two comparators continuously compare the voltage on the NO_ (or NC_) pin with V+ and V-. When the signal on NO_ or NC_ is between V+ and V- the switch acts normally, with FETs N1 and P1 turning on and off in response to IN_ signals. The parallel combination of N1 and P1 forms a low-value resistor between NO_ (or NC_) and COM_ so that signals pass equally well in either direction.

Positive Fault Condition

When the signal on NO_ (or NC_) exceeds V+ by about 50mV, the high-fault comparator output is high, turning off FETs N1 and P1. This makes the NO_ (or NC_) pin high impedance regardless of the switch state. If the switch state is “off”, all FETs are turned off and both NO_ (or NC_) and COM_ are high impedance. If the switch state is “on”, FET P2 is turned on, sourcing current from V+ to COM_.

Negative Fault Condition

When the signal on NO_ (or NC_) exceeds V- by about 50mV, the low-fault comparator output is high, turning off FETs N1 and P1. This makes the NO_ (or NC_) pin high impedance regardless of the switch state. If the switch state is “off,” all FETs are turned off and both NO_ (or NC_) and COM_ are high impedance. If the switch state is “on,” FET N2 is turned on, sinking current from COM_ to V-.

Transient Fault Response and Recovery

When a fast rise-time and fall-time transient on IN_ exceeds V+ or V-, the output (COM_) follows the input (IN_) to the supply rail with only a few nanoseconds delay. This delay is due to the switch on-resistance and circuit capacitance to ground. When the input transient returns to within the supply rails, however, there is a longer output recovery time delay. For positive faults, the recovery time is typically 3.5µs. For negative faults, the recovery time is typically 1.3µs. These values depend on the COM_ output resistance and capacitance, and are not production tested or guaranteed. The delays are not dependent on the fault amplitude. Higher COM_ output resistance and capacitance increase recovery times.

COM_ and IN_ Pins

FETs N2 and P2 can source about ±10mA from V+ or V- to the COM_ pin in the fault condition. Ensure that if the COM_ pin is connected to a low-resistance load, the absolute maximum current rating of 30mA is never exceeded, both in normal and fault conditions.

The GND, COM_, and IN_ pins do not have fault protection. Reverse ESD-protection diodes are internally connected between GND, COM_, IN_ and both V+ and V-. If a signal on GND, COM_, or IN_ exceeds V+ or V- by more than 300mV, one of these diodes will conduct heavily. During normal operation these reverse-biased ESD diodes leak a few nanoamps of current to V+ and V-.

Fault-Protection Voltage and Power Off

The maximum fault voltage on the NC_ or NO_ pins is ±36V with power applied and ±40V with power off.

Failure Modes

The MAX4511/MAX4512/MAX4513 are not lightning arrestors or surge protectors.

Exceeding the fault-protection voltage limits on NO_ or NC_, even for very short periods, can cause the device to fail. The failure modes may not be obvious, and failure in one switch may or may not affect other switches in the same package.

Ground

There is no connection between the analog signal paths and GND. The analog signal paths consist of an N-channel and P-channel MOSFET with their sources and drains paralleled and their gates driven out of phase to V+ and V- by the logic-level translators.

V+ and GND power the internal logic and logic-level translators and set the input logic thresholds. The logic-level translators convert the logic levels to switched V+ and V- signals to drive the gates of the analog switches. This drive signal is the only connection between the power supplies and the analog signals. GND, IN_, and COM_ have ESD-protection diodes to V+ and V-.

IN_ Logic-Level Thresholds

The logic-level thresholds are CMOS and TTL compatible when V+ is +15V. As V+ is raised the threshold increases slightly, and when V+ reaches 25V the level threshold is about 2.8V—above the TTL output high level minimum of 2.4V, but still compatible with CMOS outputs (see *Typical Operating Characteristics*).

Increasing V- has no effect on the logic-level thresholds, but it does increase the gate-drive voltage to the signal FETs, reducing their on-resistance.

Bipolar Supplies

The MAX4511/MAX4512/MAX4513 operate with bipolar supplies between ±4.5V and ±18V. The V+ and V- supplies need not be symmetrical, but their difference can not exceed the absolute maximum rating of 44V.

Single Supply

The MAX4511/MAX4512/MAX4513 operate from a single supply between +9V and +36V when V- is connected to GND.

High-Frequency Performance

In 50Ω systems, signal response is reasonably flat up to 50MHz (see *Typical Operating Characteristics*). Above 20MHz, the on-response has several minor peaks that are highly layout dependent. The problem with high-frequency operation is not turning the switch on, but turning it off. The off-state switch acts like a capacitor and passes higher frequencies with less attenuation. At 10MHz, off isolation is about -42dB in 50Ω systems, becoming worse (approximately 20dB per decade) as frequency increases. Higher circuit impedances also make off isolation worse. Adjacent channel attenuation is about 3dB above that of a bare IC socket and is due entirely to capacitive coupling.

Test Circuits/Timing Diagrams

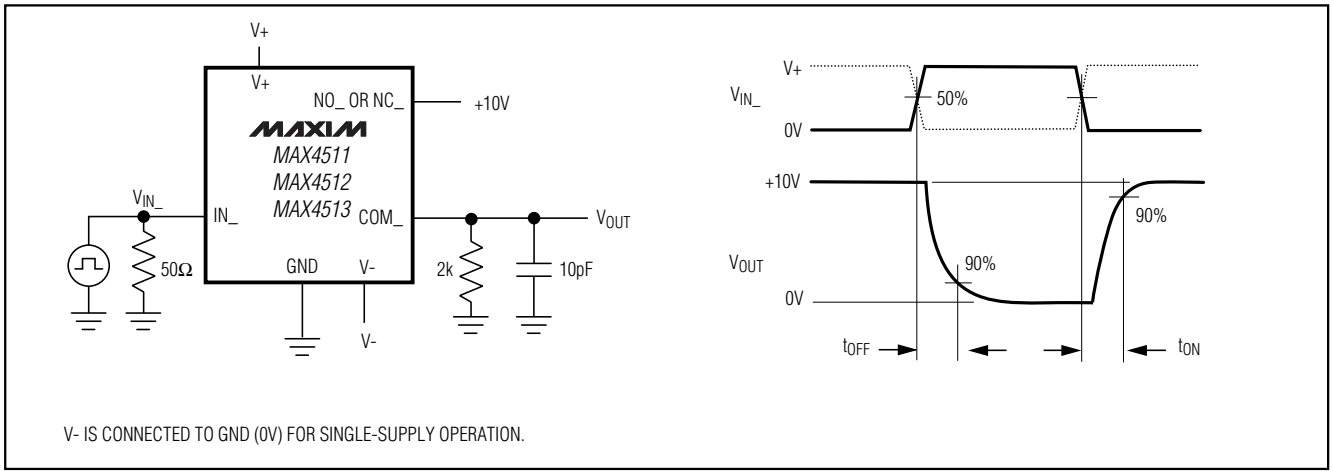


Figure 2. Switch Turn-On/Turn-Off Times

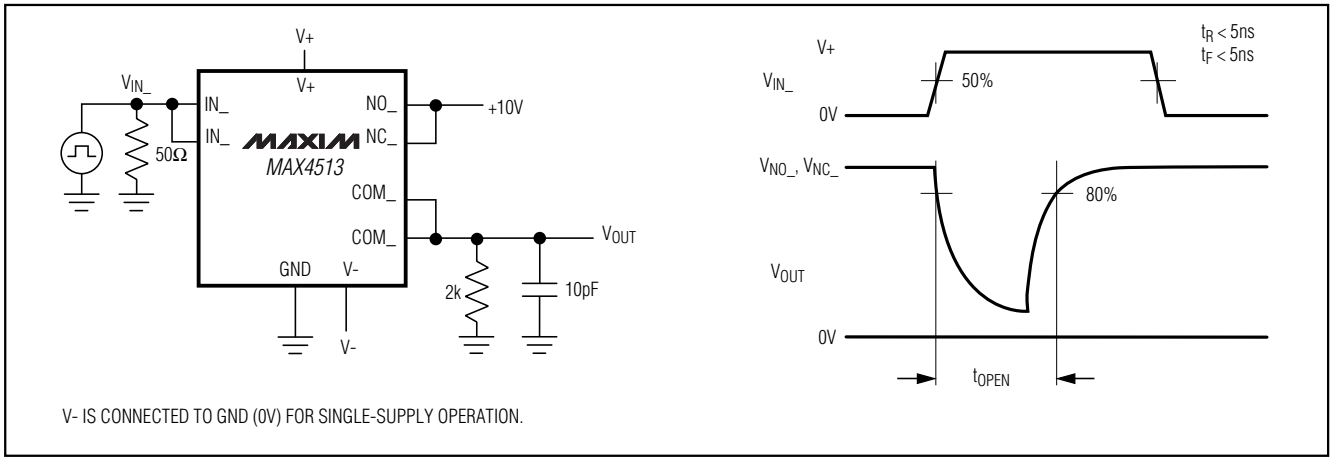


Figure 3. MAX4513 Break-Before-Make Interval

Quad, Rail-to-Rail, Fault-Protected, SPST Analog Switches

Test Circuits/Timing Diagrams (continued)

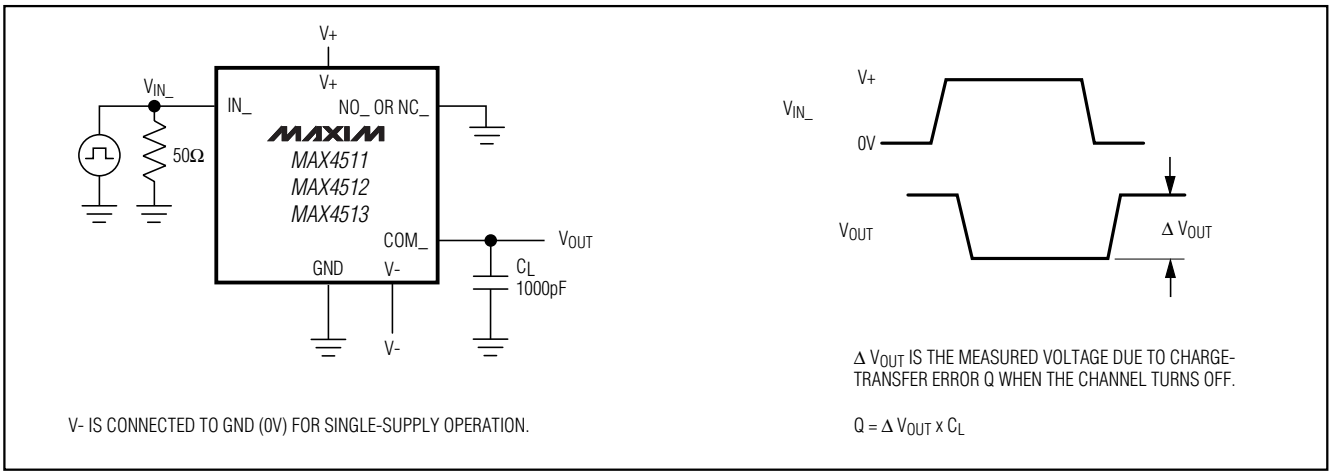


Figure 4. Charge Injection

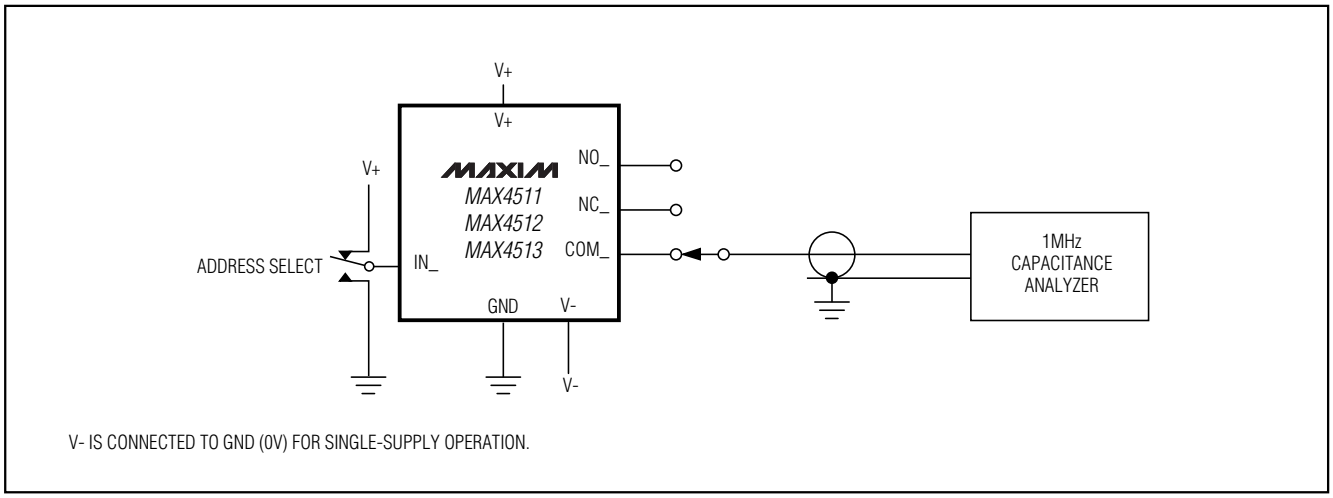
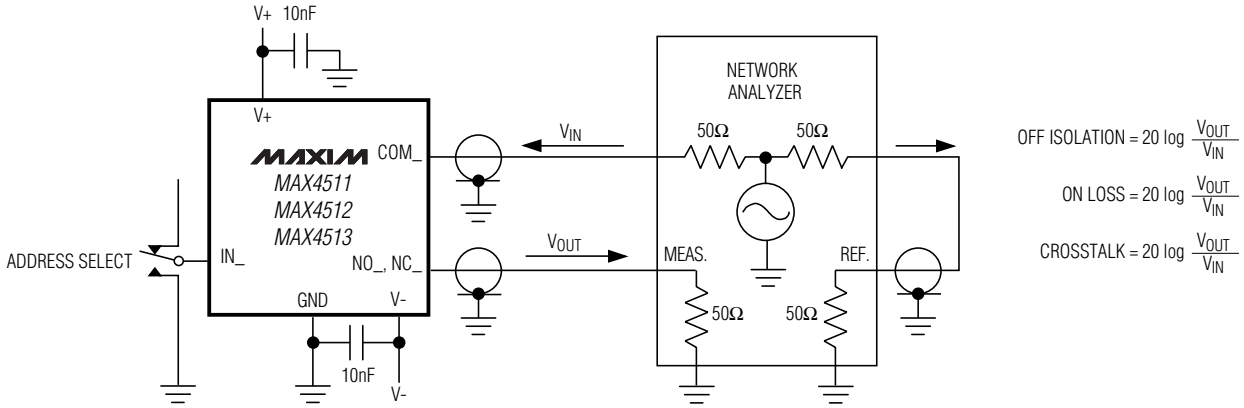


Figure 5. COM_, NO_, NC_ Capacitance

Test Circuits/Timing Diagrams (continued)

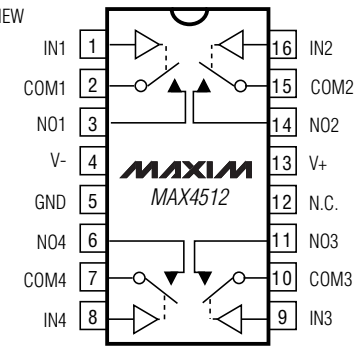


MEASUREMENTS ARE STANDARDIZED AGAINST SHORT AT SOCKET TERMINALS.
OFF ISOLATION IS MEASURED BETWEEN COM_ AND "OFF" NO_ OR NC_ TERMINALS.
ON LOSS IS MEASURED BETWEEN COM_ AND "ON" NO_ OR NC_ TERMINALS.
CROSSTALK IS MEASURED BETWEEN COM_ TERMINALS WITH ALL SWITCHES ON.
SIGNAL DIRECTION THROUGH SWITCH IS REVERSED; WORST VALUES ARE RECORDED.
V- IS CONNECTED TO GND (0V) FOR SINGLE-SUPPLY OPERATION.

Figure 6. Frequency Response, Off Isolation, and Crosstalk

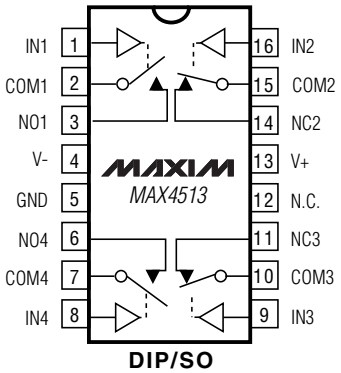
Pin Configurations/Functional Diagrams/Truth Tables (continued)

TOP VIEW



DIP/SO

MAX4512	
LOGIC	**SWITCH**
0	OFF
1	ON



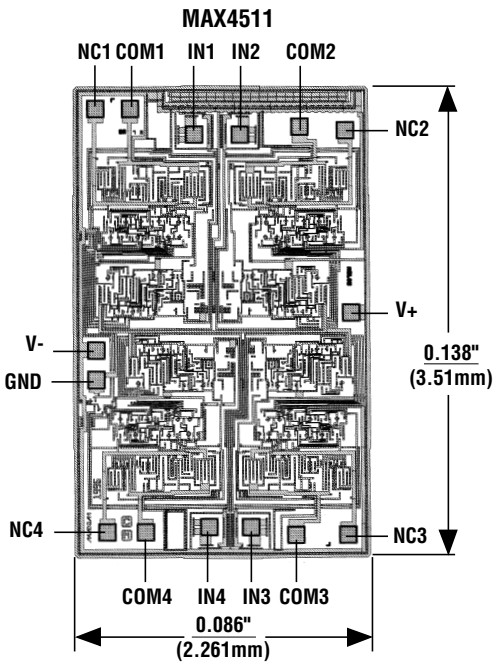
DIP/SO

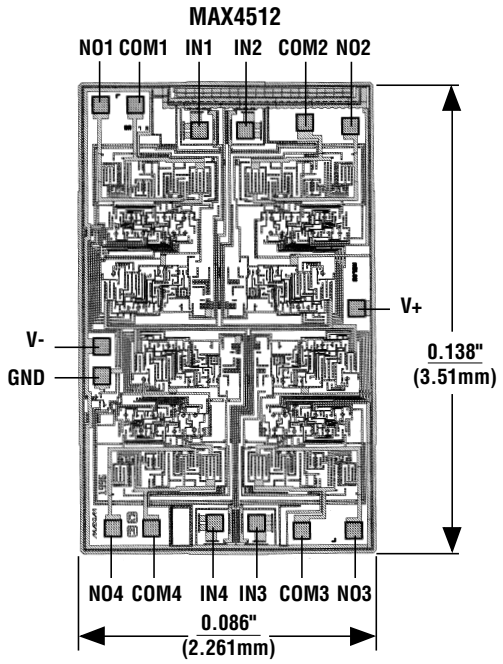
MAX4513		
LOGIC	**SWITCHES 1, 4**	**SWITCHES 2, 3**
0	OFF	ON
1	ON	OFF

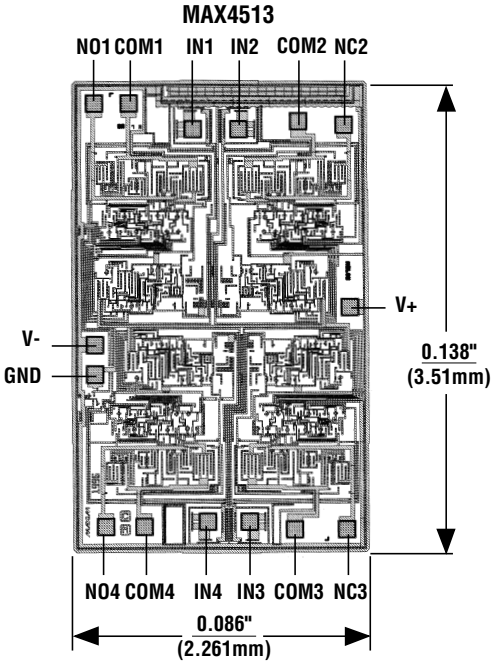
N.C. = NOT CONNECTED
SWITCHES SHOWN FOR LOGIC "0" INPUT.
ALL SWITCHES ARE OFF WITH POWER REMOVED.

Quad, Rail-to-Rail, Fault-Protected, SPST Analog Switches

Chip Topographies







TRANSISTOR COUNT: 139
SUBSTRATE CONNECTED TO: V+

Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE
MAX4512CPE	0°C to +70°C	16 Plastic DIP
MAX4512CSE	0°C to +70°C	16 Narrow SO
MAX4512CUE	0°C to +70°C	16 TSSOP
MAX4512C/D	0°C to +70°C	Dice*
MAX4512EPE	-40°C to +85°C	16 Plastic DIP
MAX4512ESE	-40°C to +85°C	16 Narrow SO
MAX4512EUE	-40°C to +85°C	16 TSSOP
MAX4512MJE	-55°C to +125°C	16 CERDIP
MAX4513CPE	0°C to +70°C	16 Plastic DIP
MAX4513CSE	0°C to +70°C	16 Narrow SO
MAX4513CUE	0°C to +70°C	16 TSSOP
MAX4513C/D	0°C to +70°C	Dice*
MAX4513EPE	-40°C to +85°C	16 Plastic DIP
MAX4513ESE	-40°C to +85°C	16 Narrow SO
MAX4513EUE	-40°C to +85°C	16 TSSOP
MAX4513MJE	-55°C to +125°C	16 CERDIP

** Contact factory for dice specifications.*

Package Information

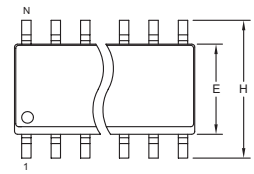
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

SOICN .EPS

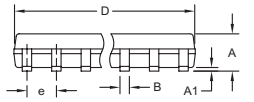
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27

VARIATIONS:

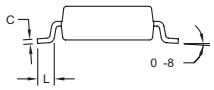
	INCHES		MILLIMETERS			
DIM	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	AA
D	0.337	0.344	8.55	8.75	14	AB
D	0.386	0.394	9.80	10.00	16	AC



TOP VIEW



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

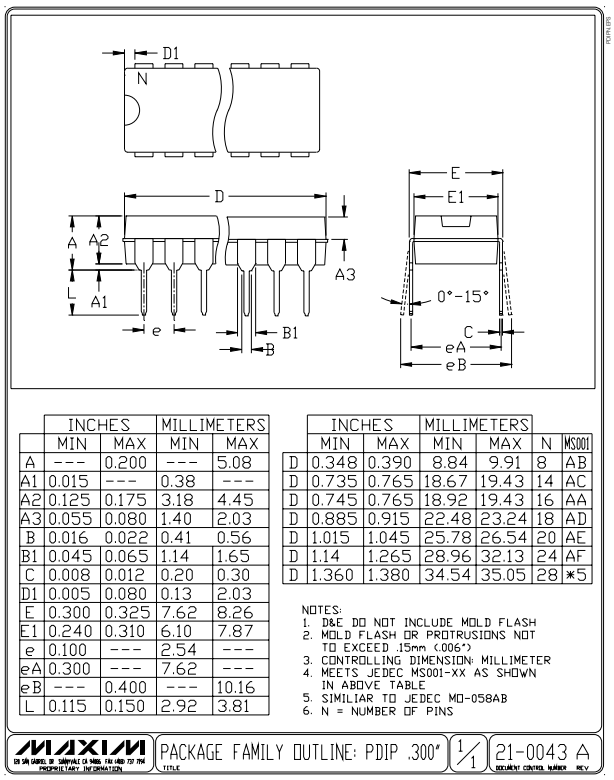
TITLE: PACKAGE OUTLINE, .150" SOIC

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0041	B	1/1

Quad, Rail-to-Rail, Fault-Protected, SPST Analog Switches

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

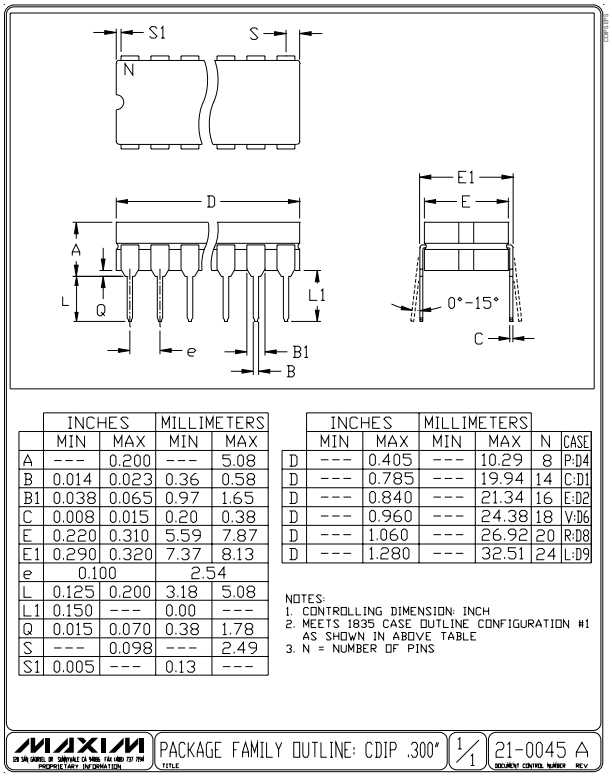


	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.200	---	5.08
A1	0.015	---	0.38	---
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	---	2.54	---
eA	0.300	---	7.62	---
eB	---	0.400	---	10.16
L	0.115	0.150	2.92	3.81

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS001
D	0.348	0.390	8.84	9.91	8	AB
D	0.735	0.765	18.67	19.43	14	AC
D	0.745	0.765	18.92	19.43	16	AA
D	0.885	0.915	22.48	23.24	18	AD
D	1.015	1.045	25.78	26.54	20	AE
D	1.14	1.265	28.96	32.13	24	AF
D	1.360	1.380	34.54	35.05	28	*5

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
5. SIMILIAR TO JEDEC MO-058AB
6. N = NUMBER OF PINS

MAXIM | PACKAGE FAMILY OUTLINE: PDIP .300" | 1/1 | 21-0043 A



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.200	---	5.08
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100		2.54	
L	0.125	0.200	3.18	5.08
L1	0.150	---	0.00	---
Q	0.015	0.070	0.38	1.78
S	---	0.098	---	2.49
S1	0.005	---	0.13	---

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	CASE
D	---	0.405	---	10.29	8	P:D4
D	---	0.785	---	19.94	14	C:D1
D	---	0.840	---	21.34	16	E:D2
D	---	0.960	---	24.38	18	V:D6
D	---	1.060	---	26.92	20	R:D8
D	---	1.280	---	32.51	24	L:D9

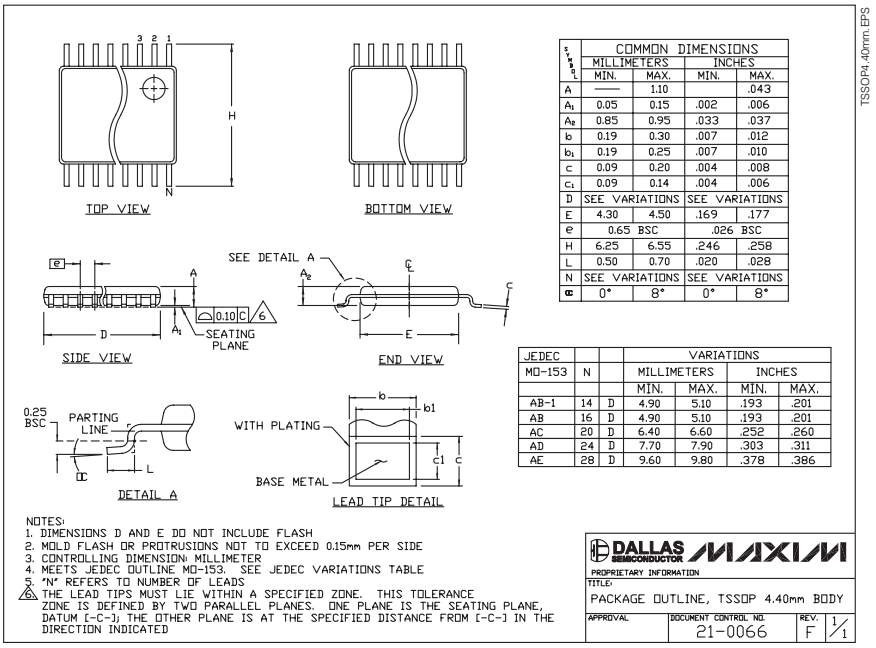
NOTES:
1. CONTROLLING DIMENSION: INCH
2. MEETS 1835 CASE OUTLINE CONFIGURATION #1 AS SHOWN IN ABOVE TABLE
3. N = NUMBER OF PINS

MAXIM | PACKAGE FAMILY OUTLINE: CDIP .300" | 1/1 | 21-0045 A

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

TSSOP4.40mm.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	——	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY
APPROVAL | DOCUMENT CONTROL NO. 21-0066 | REV. F | 1/1

Mouser Electronics

Authorized Distributor

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