Low-Cost, Triple, 8-Bit Voltage-Output DACs with Serial Interface

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ..... -0.3V, +6V
V_{SS} to GND ..... -6V, +0.3V
V_{DD} to V_{SS} ..... -0.3V, +12V
Digital Inputs and Outputs to GND..... -0.3V, (V_{DD} + 0.3V)
REFAB ..... (V_{SS} - 0.3V), (V_{DD} + 0.3V)
OUTA, OUTB (Note 1).....V_{SS}, V_{DD}
OUTC.....-0.3V, (V_{DD} + 0.3V)
REFC.....-0.3V, (V_{DD} + 0.3V)

Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 10.00mW/°C above +70°C) 800mW
SO (derate 8.33mW/°C above +70°C).....667mW
CERDIP (derate 9.09mW/°C above +70°C).....727mW
Operating Temperature Ranges
MAX51_C_ _ .....0°C to +70°C
MAX51_E_ _.....-40°C to +85°C
MAX51_MJD .....-55°C to +125°C
Storage Temperature Range.....-65°C to +165°C
Lead Temperature (soldering, 10sec) .....+300°C

Note 1: The outputs may be shorted to V_{DD}, V_{SS}, or GND if the package power dissipation is not exceeded. Typical short-circuit current to GND is 50mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +4.5V to +5.5V for MAX512, V_{DD} = +2.7V to +3.6V for MAX513, V_{SS} = GND = 0V, REFAB = REFC = V_{DD}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE						
Resolution	N		8			Bits
Differential Nonlinearity	DNL	Guaranteed monotonic			±1	LSB
Integral Nonlinearity	INL	DAC A/B (Note 2)			±1.5	LSB
		DAC C			±1	
Total Unadjusted Error	TUE	(Note 2)		±1		LSB
Zero-Code Temperature Coefficient		DAC A/B		100		µV/°C
		DAC C		5		
Power-Supply Rejection Ratio	PSRR	MAX512, 4.5V ≤ V_{DD} ≤ 5.5V, REFAB = REFC = 4.096V		0.01		%/%
		MAX513, 2.7V ≤ V_{DD} ≤ 3.6V, REFAB = REFC = 2.4V		0.015		
REFERENCE INPUTS						
Reference Input Voltage Range		REFAB	V_{SS}		V_{DD}	V
		REFC	GND		V_{DD}	
Reference Input Capacitance				25		pF
Reference Input Resistance	R_{REF}	REFAB (Note 3)	8			kΩ
		REFC (Note 3)	12			
Reference Input Resistance (shutdown mode)		REFAB, REFC		2		MΩ

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +4.5V to +5.5V for MAX512, V_{DD} = +2.7V to +3.6V for MAX513, V_{SS} = GND = 0V, REFAB = REFC = V_{DD}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DAC OUTPUTS							
Output Voltage Range				0		REF_	V
Capacitive Load		DAC A		0.10			µF
		DAC B		0.01			
		DAC C		0			
Output Resistance		DAC A			0.050		kΩ
		DAC B			0.500		
		DAC C			24		
DIGITAL INPUTS							
Input High Voltage	V_{IH}			(0.7)(V_{DD})			V
Input Low Voltage	V_{IL}					(0.3)(V_{DD})	V
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}			0.1	±10	µA
Input Capacitance	C_{IN}	(Notes 4, 5)				10	pF
DIGITAL OUTPUT							
Output High Voltage	V_{OH}	I_{SOURCE} ≤ 1.6mA		V_{DD} - 0.4			V
Output Low Voltage	V_{OL}	I_{SINK} ≤ 1.6mA				0.4	V
DYNAMIC PERFORMANCE							
Voltage-Output Slew Rate	SR	C_L = 0.1µF (DAC A), C_L = 0.01µF (DAC B)			0.1		V/µs
Voltage-Output Settling Time		To ±½LSB	C_L = 0.1µF (DAC A)		70		µs
			C_L = 0.01µF (DAC B)		70		
			C_L = 0.1nF (DAC C)		35		
Digital Feedthrough and Crosstalk		All 0s to all 1s			10		nV-s
POWER SUPPLIES							
Positive Supply Voltage Range	V_{DD}	MAX512		4.5		5.5	V
		MAX513		2.7		3.6	
Negative Supply Voltage Range (Note 6)	V_{SS}	MAX512		-5.5		-4.5	V
		MAX513		-3.6		-2.7	
Positive Supply Current	I_{DD}	All inputs = 0V	MAX512 (V_{DD} = 5.5V)		1.3	2.8	mA
			MAX513 (V_{DD} = 3.6V)		0.9	2.5	
Negative Supply Current	I_{SS}	All inputs = 0V, V_{SS} = -5.5V			-1.3		mA
Shutdown Supply Current					0.1		µA

Note 2: Digital code from 24 through 232 are due to swing limitations of output amplifiers on DAC A and DAC B. See *Typical Operating Characteristics*.

Note 3: Reference input resistance is code dependent. The lowest input resistance occurs at code 55hex. Refer to the reference input section in the *Detailed Description*.

Note 4: Guaranteed by design. Not production tested.

Note 5: Input capacitance is code dependent. The highest capacitance occurs at code 00hex.

Note 6: For single-supply mode, tie V_{SS} to GND.

TIMING CHARACTERISTICS (Note 4)

(V_{DD} = +4.5V to +5.5V for MAX512, V_{DD} = +2.7V to +3.6V for MAX513, V_{SS} = GND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

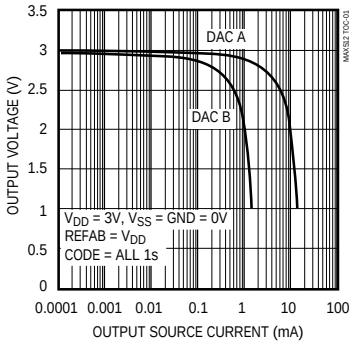
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SERIAL INTERFACE TIMING						
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		150			ns
SCLK Rise to $\overline{CS}$ Rise Setup Time	t_{CSH}		150			ns
DIN to SCLK Rise Setup Time	t_{DS}		50			ns
DIN to SCLK Rise Hold Time	t_{DH}		50			ns
SCLK Pulse Width High	t_{CH}		100			ns
SCLK Pulse Width Low	t_{CL}		100			ns
Output Delay LOUT	t_{OD}	C_L = 100pF			150	ns
$\overline{CS}$ Pulse Width High	t_{CSPWH}		200			ns

Note 4: Guaranteed by design. Not production tested.

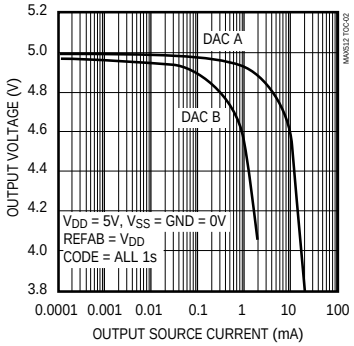
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

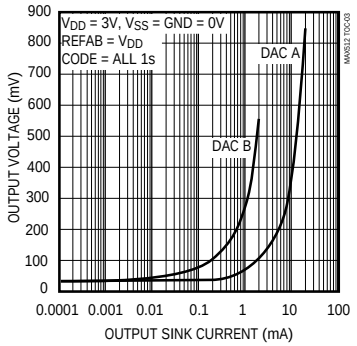
OUTPUT VOLTAGE vs. OUTPUT SOURCE CURRENT (V_{DD} = 3V)



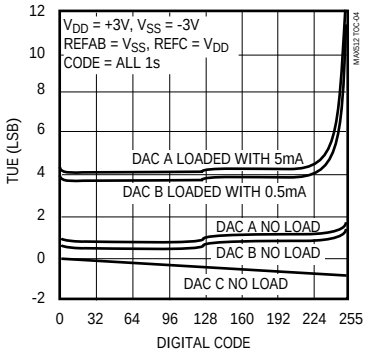
OUTPUT VOLTAGE vs. OUTPUT SOURCE CURRENT (V_{DD} = 5V)



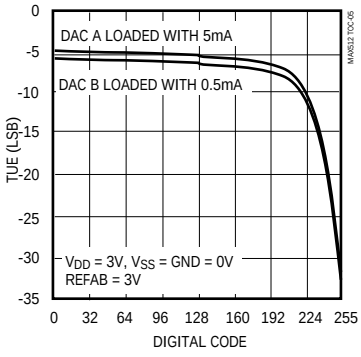
OUTPUT VOLTAGE vs. OUTPUT SINK CURRENT



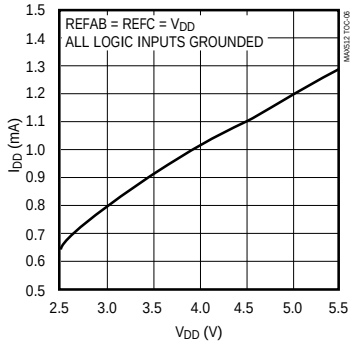
TOTAL UNADJUSTED ERROR vs. DIGITAL CODE (Dual Supplies)



TOTAL UNADJUSTED ERROR vs. DIGITAL CODE (Single Supply)



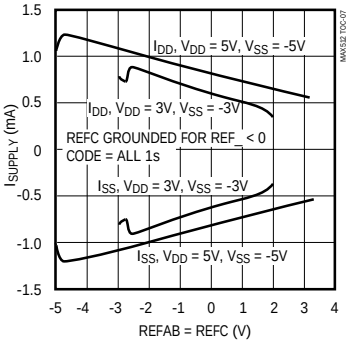
POSITIVE SUPPLY CURRENT vs. SUPPLY VOLTAGE



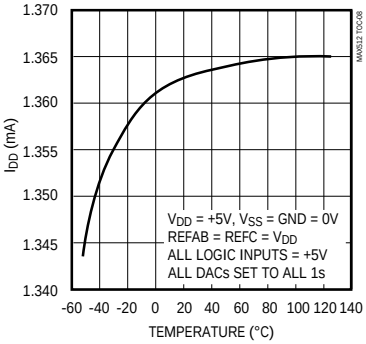
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

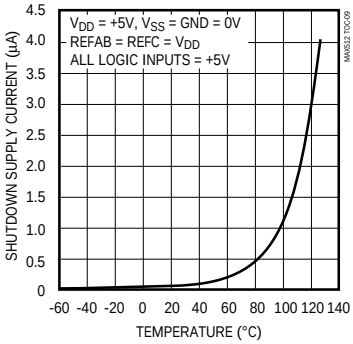
SUPPLY CURRENT vs. REFERENCE VOLTAGE



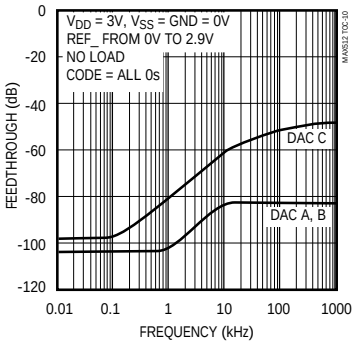
POSITIVE SUPPLY CURRENT vs. TEMPERATURE



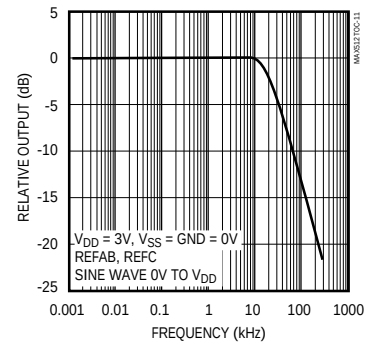
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



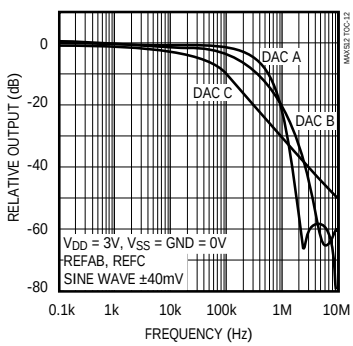
REFERENCE FEEDTHROUGH vs. FREQUENCY



REFERENCE LARGE-SIGNAL FREQUENCY RESPONSE



REFERENCE SMALL-SIGNAL FREQUENCY RESPONSE

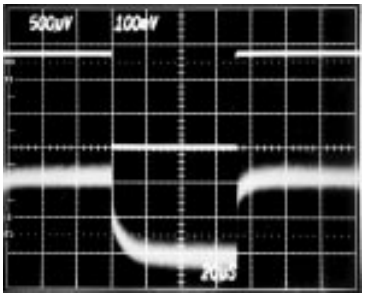


Low-Cost, Triple, 8-Bit Voltage Output DACs with Serial Interface

Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

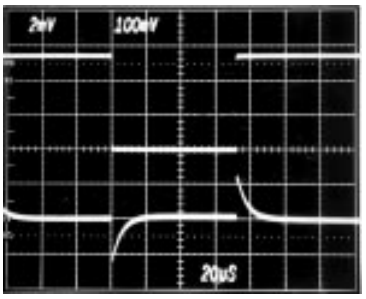
LINE-TRANSIENT RESPONSE (OUTA)



20µs/div

REFAB = 2.56V, NO LOAD, CODE = ALL 1s
A : V_{DD}, 100mV/div
B : OUTA, 500µV/div

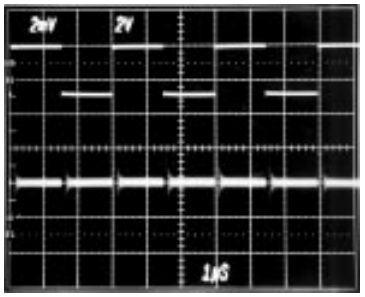
LINE-TRANSIENT RESPONSE (OUTC)



20µs/div

REFC = 2.56V, NO LOAD, CODE = ALL 1s
A : V_{DD}, 100mV/div
B : OUTC, 2mV/div

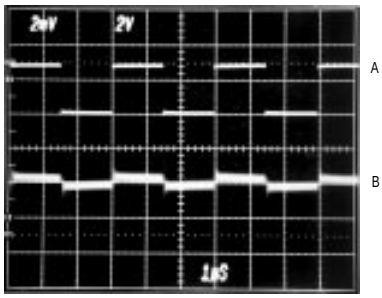
CLOCK FEEDTHROUGH (OUTA)



1µs/div

V_{SS} = 0V, $\overline{CS}$ = HIGH
A: SCLK, 333kHz, 0V TO 2.9V, 2V/div
B: OUTA, 2mV/div

CLOCK FEEDTHROUGH (OUTC)



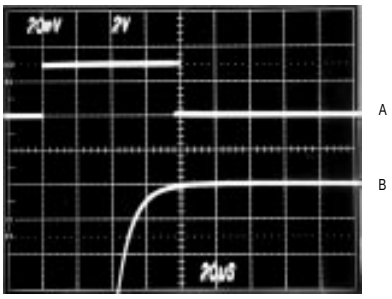
1µs/div

V_{SS} = 0V, $\overline{CS}$ = HIGH
A: SCLK, 333kHz, 0V TO 2.9V, 2V/div
B: OUTC, 2mV/div

Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

POSITIVE SETTLING TIME (DAC A)

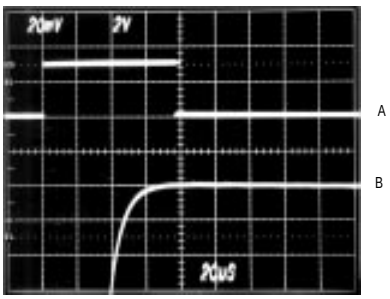


20µs/div

V_{DD} = 3V, V_{SS} = 0V, REFAB = V_{DD}, R_L = 1kΩ, C_L = 0.1µF
ALL BITS OFF TO ALL BITS ON

A: $\overline{CS}$, 2V/div
B: OUTA, 20mV/div

POSITIVE SETTLING TIME (DAC B)

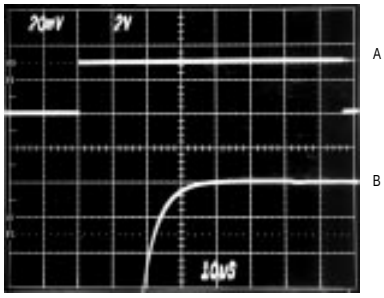


20µs/div

V_{DD} = 3V, V_{SS} = 0V, REFAB = V_{DD}, R_L = 10kΩ, C_L = 0.01µF
ALL BITS OFF TO ALL BITS ON

A: $\overline{CS}$, 2V/div
B: OUTB, 20mV/div

POSITIVE SETTLING TIME (DAC C)

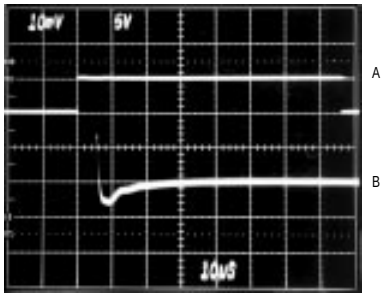


10µs/div

V_{DD} = 3V, V_{SS} = 0V, REFC = V_{DD}, R_L = ∞, C_L = 122pF
ALL BITS OFF TO ALL BITS ON

A: $\overline{CS}$, 2V/div
B: OUTC, 20mV/div

POSITIVE SETTLING TIME WITH DUAL SUPPLIES



10µs/div

V_{DD} = 5V, V_{SS} = -5V, REFAB = 2.56V, R_L = 1kΩ, C_L = 0.1µF
ALL BITS OFF TO ALL BITS ON

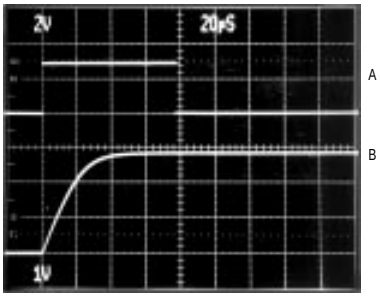
A: $\overline{CS}$, 5V/div
B: OUTA, 10mV/div

Low-Cost, Triple, 8-Bit Voltage-Output DACs with Serial Interface

Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

TIME EXITING SHUTDOWN MODE



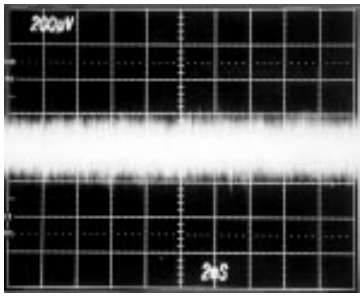
20µs/div

V_{DD} = 3V, V_{SS} = 0V, REFAB = V_{DD}, R_L = 1kΩ, C_L = 0.1µF
DAC LOADED WITH ALL 1s

A: $\overline{CS}$, 2V/div

B: OUTA, 1V/div

OUTPUT VOLTAGE NOISE DC TO 1MHz



OUTA, 200µV/div

2ms/div

DIGITAL CODE = 80, REFAB = V_{DD}, NO LOAD

Pin Description

PIN	NAME	FUNCTION
1	DIN	Serial Data Input of the 16-bit shift register. Data is clocked into the register on the rising edge of SCLK.
2	$\overline{CS}$	Chip Select (active low). Enables data to be shifted into the 16-bit shift register. Programming commands are executed at the rising edge of $\overline{CS}$.
3	SCLK	Serial Clock Input. Data is clocked in on the rising edge of SCLK.
4	$\overline{RESET}$	Asynchronous reset input (active low). Clears all registers to their default state (FFhex for DAC A and DAC B registers); all other registers are reset to 0 (including the input shift register).
5	V_{DD}	Positive Power Supply (2.7V to 5.5V). Bypass with 0.22µF to GND.
6	GND	Ground
7	V_{SS}	Negative Power Supply 0V or (-1.5V to -5.5V). Tie to GND for single supply operation. If a negative supply is applied, bypass with 0.22µF to GND.
8	OUTA	DAC A Output Voltage (Buffered). Resets to full scale. **Connect 0.1µF capacitor or greater to GND.**
9	OUTB	DAC B Output Voltage (Buffered). Resets to full scale. **Connect 0.01µF capacitor or greater to GND.**
10	OUTC	DAC C Output Voltage (Unbuffered). Resets to zero.
11	REFC	DAC C Reference Voltage
12	REFAB	DAC A/B Reference Voltage
13	I.C.	Internally connected. Do not make connections to this pin.
14	LOUT	Logic Output (latched)

Detailed Description

Analog Section

The MAX512/MAX513 contain three 8-bit, voltage-output, digital-to-analog converters (DACs). The DACs are "inverted" R-2R ladder networks using complementary switches that convert 8-bit digital inputs into equivalent analog output voltages in proportion to the applied reference voltages.

The MAX512/MAX513 have two reference inputs: one is shared by DAC A and DAC B and the other is used by DAC C. These inputs allow different full-scale output voltages and different output voltage polarities for the DAC pair A/B and DAC C.

The MAX512/MAX513 include output buffer amplifiers for DACs A and B and input logic for simple microprocessor (µP) and CMOS interfaces.

The MAX512/MAX513 operate in either single-supply or dual-supply mode, as determined by V_{SS}. If V_{SS} is within approximately -0.5V of GND, single-supply mode is assumed. If V_{SS} is below -1.5V, the devices are in dual-supply mode.

Reference Inputs and DAC Output Range

The voltage at REF_ sets the full-scale output of the DACs. The input impedance of the REF_ inputs is code dependent. The lowest value, approximately 12kΩ for REFC (8kΩ for REFAB), occurs when the input code is 01010101 (55hex). The maximum value of infinity occurs when the input code is zero.

In shutdown mode, the selected DAC output is set to zero while the value stored in the DAC register remains unchanged. This removes the load from the reference input to save power. Bringing the MAX512/MAX513 out of shutdown mode restores the DAC output voltage. Because the input resistance at REF_ is code dependent, the DAC's reference sources should have an output impedance of no more than 5Ω. The input capacitance at the REF_ pins is also code dependent and typically does not exceed 25pF.

The reference voltage on REFAB can range anywhere between the supply rails. In dual-supply mode, a positive reference input voltage on REFAB should be less than (V_{DD} - 1.5V) to avoid saturating the buffer amplifiers. The reference voltage includes the negative supply rail. See the *Output Buffer Amplifier* section for more information. The REFC input accepts positive voltages up to V_{DD} and should not be forced below ground.

The absolute difference between any reference voltage and GND should not exceed 6V.

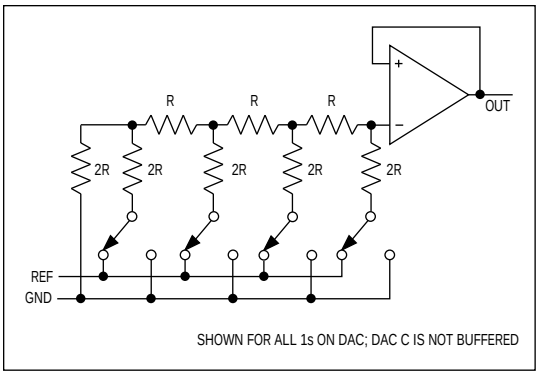


Figure 1. DAC Simplified Circuit Diagram

Output Buffer Amplifiers (DAC A / DAC B)

DAC A and DAC B voltage outputs are internally buffered. The buffer amplifiers have a rail-to-rail (V_{SS} to V_{DD}) output voltage range.

In single-supply mode, the DAC outputs A and B are internally divided by two and the buffer is set to a gain of two, eliminating the need for a buffer input voltage range to the positive supply rail.

In dual-supply mode, the DAC outputs are not attenuated and the buffer is set to unity gain.

Although only necessary for negative output voltages, the dual-supply mode may be used even if the desired DAC output voltage is positive. Possible errors associated with the divide-by-two attenuator and gain-of-two buffers in single-supply mode are eliminated in dual-supply mode. In this case, do not use reference voltages higher than (V_{DD} - 1.5V).

DAC A's output amplifier can source and sink up to 5mA of current (0.5mA for DAC B buffer). See the Total Unadjusted Error vs. Digital Code graph in the *Typical Operating Characteristics* for dual and single supplies. The amplifier is unity-gain stable with a capacitive load of 0.05µF (0.01µF for DAC B buffer) or greater. The slew rate is limited by the load capacitor and is typically 0.1V/µs with a 0.1µF load (0.01µF for DAC B buffer).

Unbuffered Output (DAC C)

The output of DAC C is unbuffered and has a typical output impedance of 24kΩ. It can be used to drive a high-impedance load, such as an op amp or comparator, and has 35µs typical settling time to 1/2LSB with a single 3V supply. Use DAC C if a quick dynamic response is required.

Low-Cost, Triple, 8-Bit Voltage-Output DACs with Serial Interface

Shutdown Mode

When programmed to shutdown mode, the outputs of DAC A and B go into a high-impedance state. Virtually no current flows into or out of the buffer amplifiers in that state. The output of DAC C goes to 0V when shut down. In shutdown mode, the REF_ inputs are high impedance (2MΩ typ) to conserve current drain from the system reference; therefore, the system reference does not have to be powered down. The logic output LOUT remains active in shutdown.

Coming out of shutdown, the DAC outputs return to the values kept in the registers. The recovery time is equivalent to the DAC settling time.

Reset

The $\overline{RESET}$ input is active low. When asserted ($\overline{RESET}$ = 0), DACs A and B are set to full scale (FFhex) and active, while DAC C is set to zero code (00hex) and active. The 16-bit serial register is cleared to 0000hex. LOUT is reset to zero.

Serial Interface

An active-low chip select ($\overline{CS}$) enables the shift register to receive data from the serial data input. Data is clocked into the shift register on every rising edge of the serial clock signal (SCLK). The clock frequency can be as high as 5MHz.

Data is sent MSB first and can be transmitted in one 16-bit word. The write cycle can be interrupted at any time when $\overline{CS}$ is kept active (low) to allow, for example, two 8-bit-wide transfers. After clocking all 16 bits into the input shift register, the rising edge of $\overline{CS}$ updates the DAC outputs, the shutdown status, and the status of the logic output. Because of their single buffered structure, DACs cannot be simultaneously updated to different digital values.

Table 1. Input Shift Register

DATA BITS	B0*	DAC Data Bit 0 (LSB)
	B1	DAC Data Bit 1
	B2	DAC Data Bit 2
	B3	DAC Data Bit 3
	B4	DAC Data Bit 4
	B5	DAC Data Bit 5
	B6	DAC Data Bit 6
	B7	DAC Data Bit 7 (MSB)
CONTROL BITS	LA	Load Reg DAC A, Active High
	LB	Load Reg DAC B, Active High
	LC	Load Reg DAC C, Active High
	SA	Shut Down DAC A, Active High
	SB	Shut Down DAC B, Active High
	SC	Shut Down DAC C, Active High
	Q1	Logic Output
	Q2**	Uncommitted Bit

* Clocked in last.
**Clocked in first.

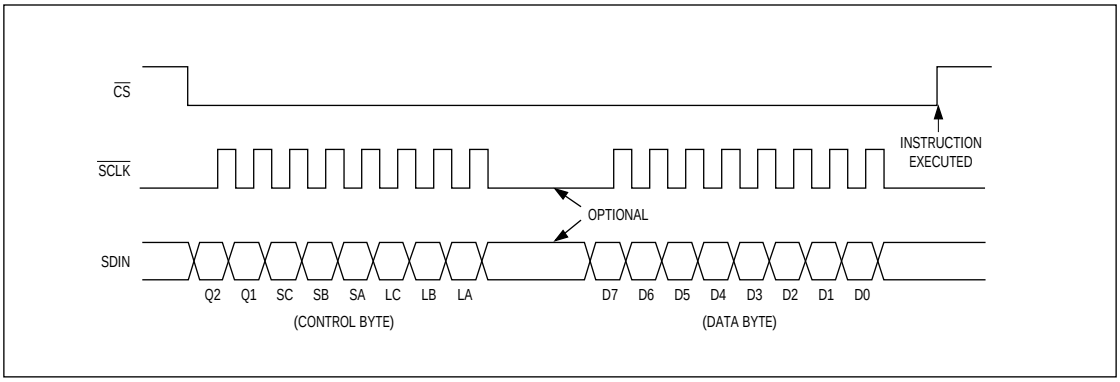


Figure 2. MAX512/MAX513 3-Wire Serial-Interface Timing Diagram

Table 2. Serial-Interface Programming Commands

CONTROL								DATA								FUNCTION
								MSB							LSB	
Q2	Q1	SC	SB	SA	LC	LB	LA	B7	B6	B5	B4	B3	B2	B1	B0	
*	*	*	*	*	0	0	0	X	X	X	X	X	X	X	X	No Operation to DAC Registers
*	*	*	*	*	1	0	0	8-Bit DAC Data								Load Register to DAC C
*	*	*	*	*	0	1	0	8-Bit DAC Data								Load Register to DAC B
*	*	*	*	*	0	0	1	8-Bit DAC Data								Load Register to DAC A
*	*	*	*	*	1	1	1	8-Bit DAC Data								Load All DAC Registers
*	*	0	0	0	*	*	*	X	X	X	X	X	X	X	X	All DACs Active
*	*	1	0	0	*	*	*	X	X	X	X	X	X	X	X	Shut Down DAC C
*	*	0	1	0	*	*	*	X	X	X	X	X	X	X	X	Shut Down DAC B
*	*	0	0	1	*	*	*	X	X	X	X	X	X	X	X	Shut Down DAC A
*	*	1	1	1	*	*	*	X	X	X	X	X	X	X	X	Shut Down All DACs
X	0	*	*	*	*	*	*	X	X	X	X	X	X	X	X	Reset LOUT
X	1	*	*	*	*	*	*	X	X	X	X	X	X	X	X	Set LOUT

X *Don't care.*

* *Not shown for clarity. The functions of loading and shutting down the DACs and programming the logic can be combined in a single command.*

Serial-Input Data Format and Control Codes

Table 2 lists the serial-input data format. The 16-bit input word consists of an 8-bit control byte and an 8-bit data byte. The 8-bit control byte is not decoded internally. Every control bit performs one function. Data is clocked in starting with Q2 (uncommitted bit), followed by the remaining control bits and the data byte. The LSB of the data byte (B0) is the last bit clocked into the shift register (Figure 2).

Example of a 16-bit input word:

Loaded in First															Loaded in Last
Q2	Q1	SC	SB	SA	LC	LB	LA	B7	B6	B5	B4	B3	B2	B1	B0
X	0	1	0	0	0	1	1	1	0	0	0	0	0	0	0

The example above performs the following functions:

- 80hex (128 decimal) loaded into DAC registers A and B.
- Content of the DAC C register remains unchanged.
- DAC A and DAC B are active.
- DAC C is shut down.
- LOUT is reset to 0.

Digital Inputs

The digital inputs are compatible with CMOS logic. Supply current increases slightly when toggling the logic inputs through the transition zone between $(0.3)(V_{DD})$ and $(0.7)(V_{DD})$.

Digital Output

The latched digital output (LOUT) has a 1.6mA source capability while maintaining a (V_{DD} - 0.4V) output level. With a 1.6mA sink current, the output voltage is guaranteed to be no more than 0.4V. The output can be used for digital auxiliary control. Please note that the digital output remains fully active during shutdown mode.

Microprocessor Interfacing

The MAX512/MAX513 serial interface is compatible with Microwire, SPI, and QSPI. For SPI and QSPI, clear the CPOL and CPHA bits (CPOL = 0 and CPHA = 0). CPOL = 0 sets the inactive state of clock to zero and CPHA = 0 changes data at the falling edge of SCLK. This setting allows both SPI and QSPI to run at full clock speeds (0.5MHz and 4MHz, respectively). If a serial port is not available on your µP, three bits of a parallel port can be used to emulate a serial port by bit manipulation. Minimize digital feedthrough at the voltage outputs by operating the serial clock only when necessary.

Low-Cost, Triple, 8-Bit Voltage-Output DACs with Serial Interface

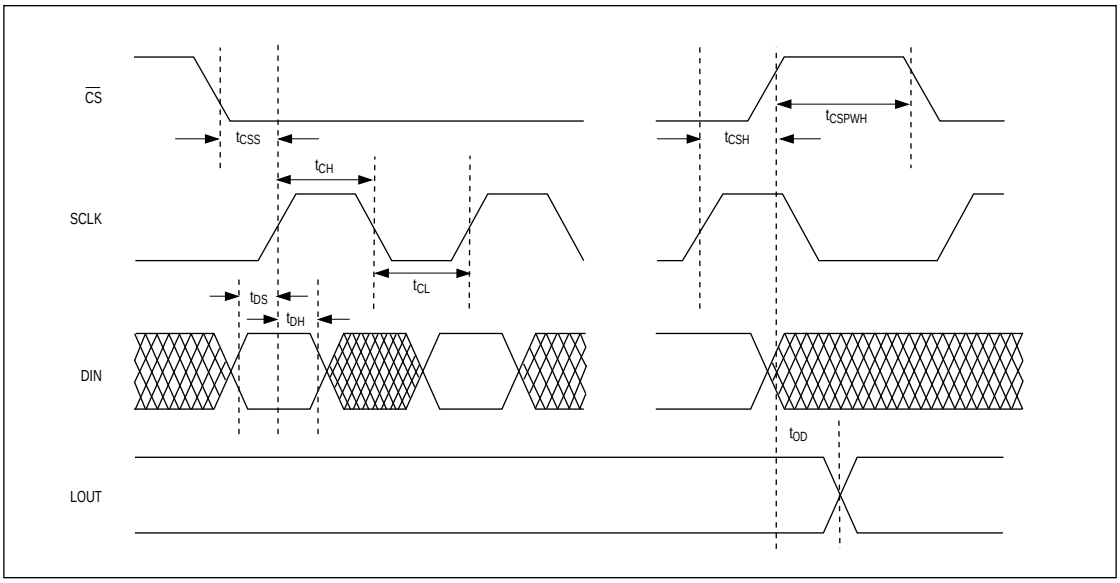


Figure 3. MAX512/MAX513 Detailed Serial-Interface Timing Diagram

Applications Information

Power-Supply and Reference Operating Ranges

The MAX512 is fully specified to operate with V_{DD} = 5V ±10% and V_{SS} = GND = 0V. The MAX513 is specified for single-supply operation with V_{DD} ranging from 2.7V to 3.6V, covering all commonly used supply voltages in 3V systems. The MAX512/MAX513 can also be used with a negative supply ranging from -1.5V to -5.5V. Using a negative supply typically improves zero-code error and settling time (as shown in the *Typical Operating Characteristics* graphs).

The two separate reference inputs for the DAC pair A/B and the unbuffered output C allow different full-scale output voltages and, if a negative supply is used, also allow different polarity. In dual-supply mode, REFAB can vary from V_{SS} to (V_{DD} - 1.5V). In single-supply mode, the specified range for REFAB is 0V to V_{DD}. REFC can range from GND to V_{DD}. Do not force REFC below ground.

Power-supply sequencing is not critical. If a negative supply is used, make sure V_{SS} is never more than 0.3V above ground. Do not apply signals to the digital inputs until the device is powered-up. If this is not possible, add current-limiting resistors to the digital inputs.

Power-Supply Bypassing and Ground Management

In single-supply operation (V_{SS} = GND), GND and V_{SS} should be connected to the highest quality ground available. Bypass V_{DD} with a 0.1µF to 0.22µF capacitor to GND. For dual-supply operation, bypass V_{SS} with a 0.1µF to 0.22µF capacitor to GND. Reference inputs can be used without bypassing. For optimum line/load-transient response and noise performance, bypass the reference inputs with 0.1µF to 4.7µF to GND. Careful PC board layout minimizes crosstalk among DAC outputs, reference inputs, and digital inputs. Separate analog lines with ground traces between them. Make sure that high-frequency digital lines are not routed in parallel to analog lines.

Unipolar Output

With unipolar output, the output voltage and the reference voltage are the same polarity. The MAX512/MAX513 can be used with a single supply if the reference voltages are positive. With a negative supply, the REFAB voltage can vary from V_{SS} to approximately (V_{DD} - 1.5V), allowing two-quadrant multiplication.

Table 3. Unipolar Code Table

DAC CONTENTS								ANALOG OUTPUT
B7	B6	B5	B4	B3	B2	B1	B0	
1	1	1	1	1	1	1	1	$+REF\_ \times \left(\frac{255}{256}\right)$
1	0	0	0	0	0	0	1	$+REF\_ \times \left(\frac{129}{256}\right)$
1	0	0	0	0	0	0	0	$+REF\_ \times \left(\frac{128}{256}\right) = +\frac{REF\_}{2}$
0	1	1	1	1	1	1	1	$+REF\_ \times \left(\frac{127}{256}\right)$
0	0	0	0	0	0	0	1	$+REF\_ \times \left(\frac{1}{256}\right)$
0	0	0	0	0	0	0	0	0V

Note :

$$1LSB = REF\_ \times 2^{-8} = REF\_ \times \left(\frac{1}{256}\right)$$

$$ANALOG\ OUTPUT = REF\_ \times \left(\frac{D}{256}\right)$$

Table 4. Bipolar Code Table

DAC CONTENTS								ANALOG OUTPUT
B7	B6	B5	B4	B3	B2	B1	B0	
1	1	1	1	1	1	1	1	$+REF\_ \times \left(\frac{127}{128}\right)$
1	0	0	0	0	0	0	1	$+REF\_ \times \left(\frac{1}{128}\right)$
1	0	0	0	0	0	0	0	0V
0	1	1	1	1	1	1	1	$-REF\_ \times \left(\frac{1}{128}\right)$
0	0	0	0	0	0	0	1	$-REF\_ \times \left(\frac{127}{128}\right)$
0	0	0	0	0	0	0	0	$-REF\_ \times \left(\frac{128}{128}\right) = -REF\_$

Note :

$$1LSB = REF\_ \times 2^{-(8-1)} = REF\_ \times \left(\frac{1}{128}\right)$$

$$ANALOG\ OUTPUT = REF\_ \times \left(\frac{D}{128} - 1\right)$$

Bipolar Output

Using Figure 4's circuit, the MAX512/MAX13 can be configured for bipolar outputs. Table 4 lists the bipolar codes and corresponding output voltages. There are two ways to achieve rail-to-rail outputs: 1) Operate the MAX512/MAX513 with a single supply and positive reference voltages or 2) Use dual supplies with a positive or negative voltage at REFAB and a positive voltage at REFC. In either case, the op amps need dual supplies. When using the dual-supply mode, possible errors associated with the divide-by-two attenuator and gain-of-two buffer are eliminated (see the *Output Buffer Amplifier* section). For maximum output swing of all outputs in dual-supply mode, connect REFAB to V_{SS} and REFC to V_{DD}. In single-supply mode, connect REFAB, REFC, and V_{DD} together.

With dual supplies, DACs A and B can perform four-quadrant multiplication. Please note that in dual-supply mode, the REFAB input ranges from V_{SS} to (V_{DD} - 1.5V). Because REFC accepts only positive inputs, DAC C performs two-quadrant multiplication.

Figure 4 shows Maxim's ICL7612A with rail-to-rail input common-mode range and rail-to-rail output voltage swing—ideal for a high output voltage swing from low supply voltages.

RF Applications

Both the MAX512 and MAX513 can bias GaAs FETs, where the gate of the FETs must be negatively biased to ensure that there is no drain current. In a typical application, power to the RF amplifiers should not be turned on until the bias voltages provided by DAC A and DAC B are fully established; likewise, the supply should be turned off before the bias voltage is switched off. Figure 5 shows how DAC B supplies the negative bias V_{GG1} for the driver stage and DAC A provides the negative bias V_{GG2} for the output stage [1].

The DAC A and DAC B outputs are also ideal for controlling VCOs in mobile radios or cellular phones. Other applications include varactor and PIN diode circuits.

The unbuffered DAC C provides a span within GND and V_{DD} and is individually set at REF C. DAC C typically adjusts offset and gain in the system.

1 [John Wachsmann. "A High-Efficiency GaAs MMIC Power Amplifier for 1.9GHz PCS Applications," Proceedings of the First Annual Wireless Symposium, pp. 375, Penton Publishing, Jan. 1993.]

Low-Cost, Triple, 8-Bit Voltage-Output DACs with Serial Interface

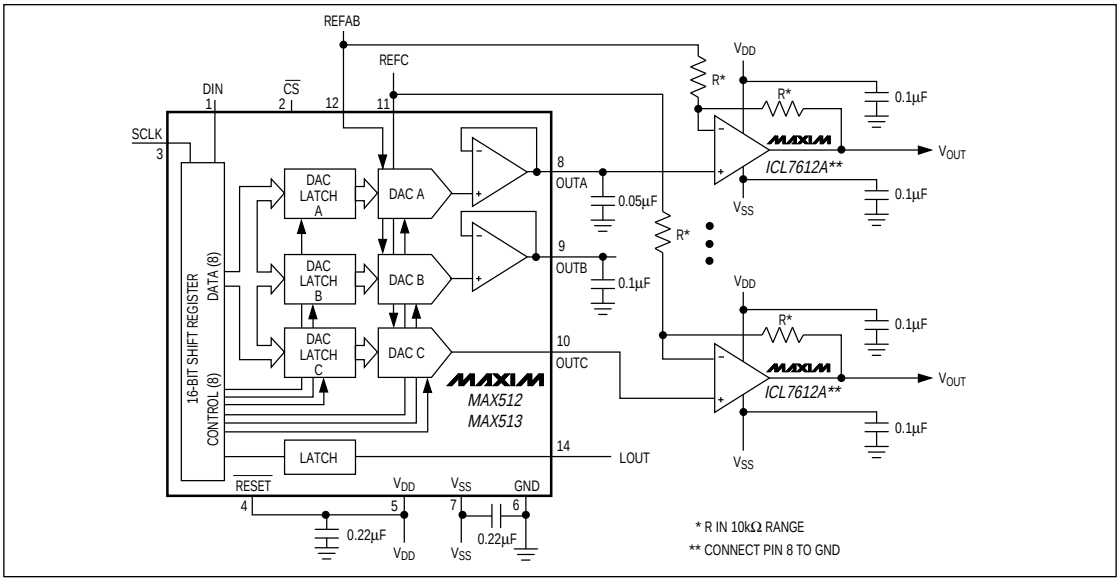


Figure 4. Bipolar Output Circuit

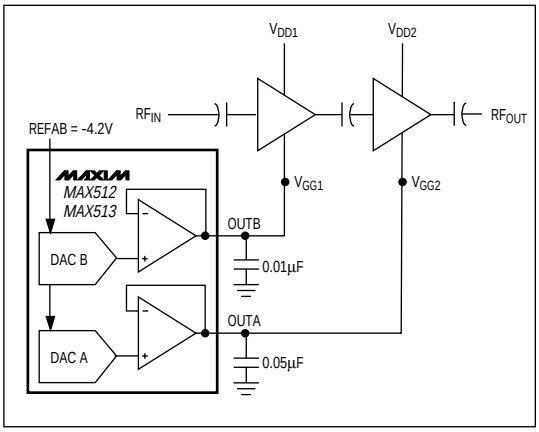


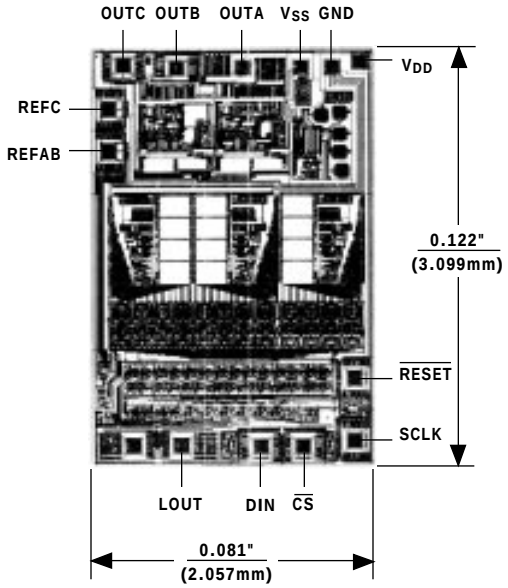
Figure 5. RF Bias Circuit

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX512EPD	-40°C to +85°C	14 Plastic DIP
MAX512ESD	-40°C to +85°C	14 SO
MAX512MJD	-55°C to +125°C	14 CERDIP
MAX513CPD	0°C to +70°C	14 Plastic DIP
MAX513CSD	0°C to +70°C	14 SO
MAX513C/D	0°C to +70°C	Dice*
MAX513EPD	-40°C to +85°C	14 Plastic DIP
MAX513ESD	-40°C to +85°C	14 SO
MAX513MJD	-55°C to +125°C	14 CERDIP

** Contact factory for dice specifications.*

_____Chip Topography

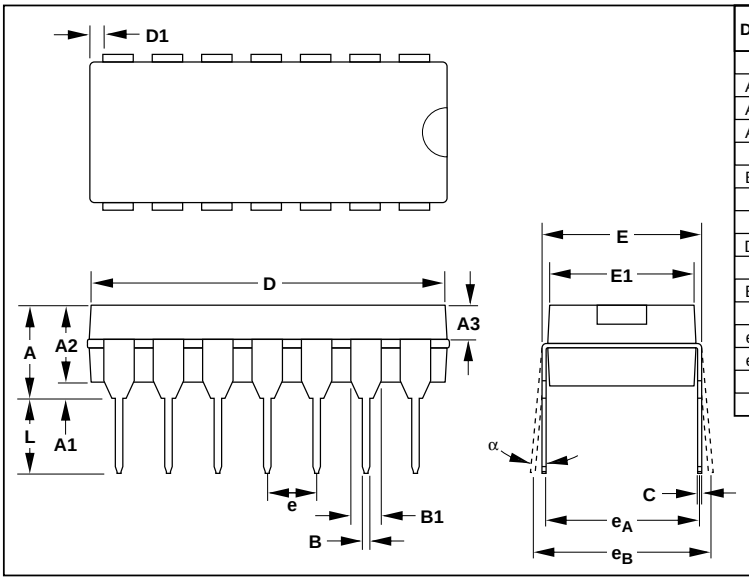


TRANSISTOR COUNT: 1910

SUBSTRATE CONNECTED TO V_{DD}

Low-Cost, Triple, 8-Bit Voltage-Output DACs with Serial Interface

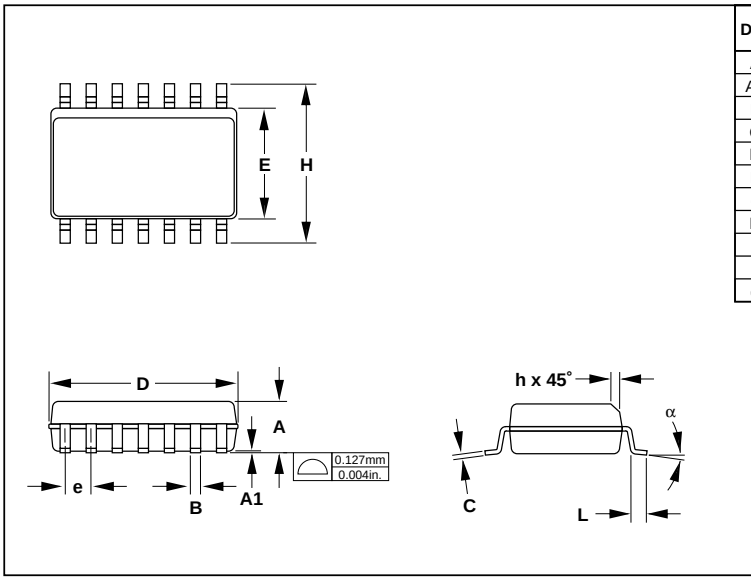
Package Information



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.150	3.18	3.81
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.050	0.065	1.27	1.65
C	0.008	0.012	0.20	0.30
D	0.735	0.765	18.67	19.43
D1	0.050	0.080	1.27	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e_A	0.300 BSC		7.62 BSC	
e_B	–	0.400	–	10.16
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°

21-330A

14-PIN PLASTIC DUAL-IN-LINE PACKAGE



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
D	0.337	0.344	8.55	8.75
E	0.150	0.157	3.80	4.00
e	0.050 BSC		1.27 BSC	
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

21-331A

14-PIN PLASTIC SMALL-OUTLINE PACKAGE

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