

# LM339, LM339E, LM239, LM2901, LM2901E, LM2901V, NCV2901, MC3302

## MAXIMUM RATINGS

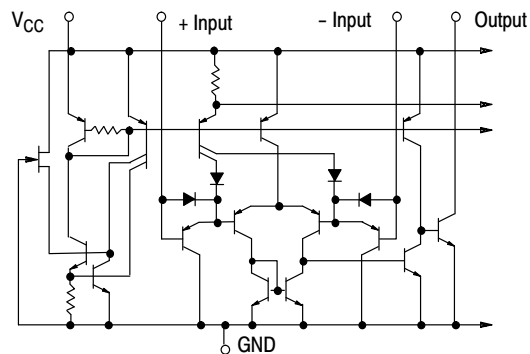
Rating	Symbol	Value	Unit
Power Supply Voltage LM239/LM339, E/LM2901, E, V MC3302	$V_{CC}$	+36 or $\pm 18$ +30 or $\pm 15$	Vdc
Input Differential Voltage Range LM239/LM339, E/LM2901, E, V MC3302	$V_{IDR}$	36 30	Vdc
Input Common Mode Voltage Range	$V_{ICMR}$	-0.3 to 36	Vdc
Output Short Circuit to Ground (Note 1)	$I_{SC}$	Continuous	
Power Dissipation @ $T_A = 25^\circ\text{C}$ Plastic Package Derate above $25^\circ\text{C}$	$P_D$ $1/R_{\theta JA}$	1.0 8.0	W mW/ $^\circ\text{C}$
Junction Temperature	$T_J$	150	$^\circ\text{C}$
Operating Ambient Temperature Range LM239 MC3302 LM2901, LM2901E LM2901V, NCV2901 LM339, LM339E	$T_A$	-25 to +85 -40 to +85 -40 to +105 -40 to +125 0 to +70	$^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-65 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The maximum output current may be as high as 20 mA, independent of the magnitude of  $V_{CC}$ . Output short circuits to  $V_{CC}$  can cause excessive heating and eventual destruction.

## ESD RATINGS

Rating	HBM	MM	Unit
ESD Protection at any Pin (Human Body Model – HBM, Machine Model – MM) NCV2901	2000	200	V
LM339E, LM2901E	1500	200	V
LM339DG/DR2G, LM2901DG/DR2G	250	100	V
All Other Devices	1500	200	V



NOTE: Diagram shown is for 1 comparator.

Figure 1. Circuit Schematic

# LM339, LM339E, LM239, LM2901, LM2901E, LM2901V, NCV2901, MC3302

## ELECTRICAL CHARACTERISTICS (V<sub>CC</sub> = +5.0 Vdc, T<sub>A</sub> = +25°C, unless otherwise noted)

Characteristic	Symbol	LM239/339/339E			LM2901/2901E/2901V /NCV2901			MC3302			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 3)	V <sub>IO</sub>	-	±2.0	±5.0	-	±2.0	±7.0	-	±3.0	±20	mVdc
Input Bias Current (Notes 3, 4) (Output in Analog Range)	I <sub>IB</sub>	-	25	250	-	25	250	-	25	500	nA
Input Offset Current (Note 3)	I <sub>IO</sub>	-	±5.0	±50	-	±5.0	±50	-	±3.0	±100	nA
Input Common Mode Voltage Range (Note 5)	V <sub>ICMR</sub>	0	-	V <sub>CC</sub> -1.5	0	-	V <sub>CC</sub> -1.5	0	-	V <sub>CC</sub> -1.5	V
Supply Current R <sub>L</sub> = ∞ (For All Comparators) R <sub>L</sub> = ∞, V <sub>CC</sub> = 30 Vdc	I <sub>CC</sub>	-	0.8 1.0	2.0 2.5	-	0.8 1.0	2.0 2.5	-	0.8 1.0	2.0 2.5	mA
Voltage Gain R <sub>L</sub> ≥ 15 kΩ, V <sub>CC</sub> = 15 Vdc	A <sub>VOL</sub>	50	200	-	25	100	-	25	100	-	V/mV
Large Signal Response Time V <sub>I</sub> = TTL Logic Swing, V <sub>ref</sub> = 1.4 Vdc, V <sub>RL</sub> = 5.0 Vdc, R <sub>L</sub> = 5.1 kΩ	-	-	300	-	-	300	-	-	300	-	ns
Response Time (Note 6) V <sub>RL</sub> = 5.0 Vdc, R <sub>L</sub> = 5.1 kΩ	-	-	1.3	-	-	1.3	-	-	1.3	-	μs
Output Sink Current V <sub>I</sub> (-) ≥ +1.0 Vdc, V <sub>I</sub> (+) = 0, V <sub>O</sub> ≤ 1.5 Vdc	I <sub>Sink</sub>	6.0	16	-	6.0	16	-	6.0	16	-	mA
Saturation Voltage V <sub>I</sub> (-) ≥ +1.0 Vdc, V <sub>I</sub> (+) = 0, I <sub>sink</sub> ≤ 4.0 mA	V <sub>sat</sub>	-	130	400	-	130	400	-	130	500	mV
Output Leakage Current V <sub>I</sub> (+) ≥ +1.0 Vdc, V <sub>I</sub> (-) = 0, V <sub>O</sub> = +5.0 Vdc	I <sub>OL</sub>	-	0.1	-	-	0.1	-	-	0.1	-	nA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- (LM239) T<sub>low</sub> = -25°C, T<sub>high</sub> = +85°C  
(LM339, LM339E) T<sub>low</sub> = 0°C, T<sub>high</sub> = +70°C  
(MC3302) T<sub>low</sub> = -40°C, T<sub>high</sub> = +85°C  
(LM2901), LM2901E T<sub>low</sub> = -40°C, T<sub>high</sub> = +105°C  
(LM2901V & NCV2901) T<sub>low</sub> = -40°C, T<sub>high</sub> = +125°C  
*NCV2901 is qualified for automotive use.*
- At the output switch point, V<sub>O</sub> = 1.4 Vdc, R<sub>S</sub> ≤ 100 Ω 5.0 Vdc ≤ V<sub>CC</sub> ≤ 30 Vdc, with the inputs over the full common mode range (0 Vdc to V<sub>CC</sub> - 1.5 Vdc).
- The bias current flows out of the inputs due to the PNP input stage. This current is virtually constant, independent of the output state.
- Positive excursions of input voltage may exceed the power supply level. As long as one input voltage remains within the common mode range, the comparator will provide a proper output state. Refer to the Maximum Ratings table for safe operating area.
- The response time specified is for a 100 mV input step with 5.0 mV overdrive. For larger signals, 300 ns is typical.

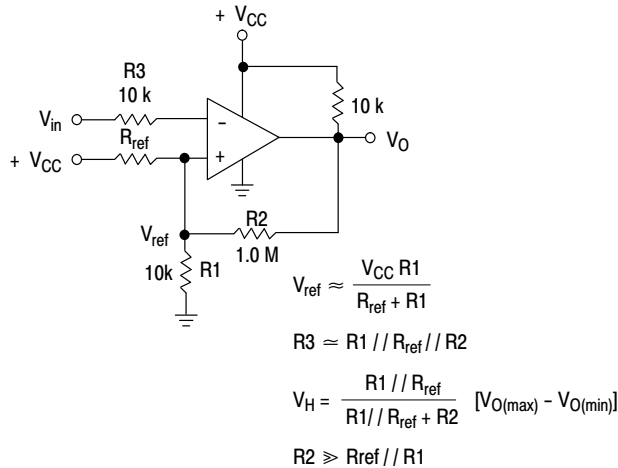
# LM339, LM339E, LM239, LM2901, LM2901E, LM2901V, NCV2901, MC3302

## PERFORMANCE CHARACTERISTICS (V<sub>CC</sub> = +5.0 Vdc, T<sub>A</sub> = T<sub>low</sub> to T<sub>high</sub> [Note 7])

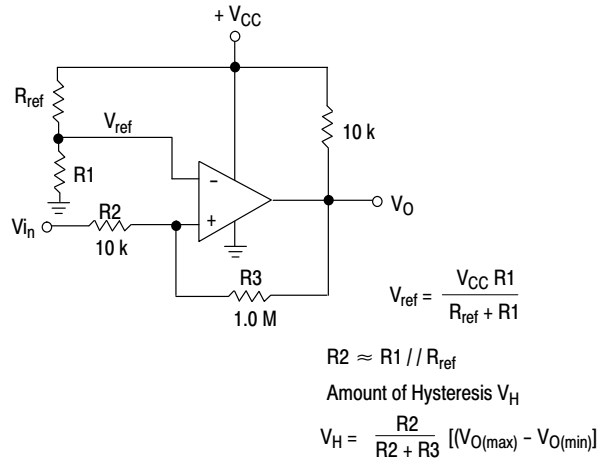
Characteristic	Symbol	LM239/339/339E			LM2901/2901E/2901V /NCV2901			MC3302			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 8)	V <sub>IO</sub>	-	-	±9.0	-	-	±15	-	-	±40	mVdc
Input Bias Current (Notes 8, 9) (Output in Analog Range)	I <sub>IB</sub>	-	-	400	-	-	500	-	-	1000	nA
Input Offset Current (Note 8)	I <sub>IO</sub>	-	-	±150	-	-	±200	-	-	±300	nA
Input Common Mode Voltage Range	V <sub>ICMR</sub>	0	-	V <sub>CC</sub> -2.0	0	-	V <sub>CC</sub> -2.0	0	-	V <sub>CC</sub> -2.0	V
Saturation Voltage  V <sub>I(-)</sub> ≥ +1.0 Vdc, V <sub>I(+)</sub> = 0, I <sub>sink</sub> ≤ 4.0 mA	V <sub>sat</sub>	-	-	700	-	-	700	-	-	700	mV
Output Leakage Current  V <sub>I(+)</sub> ≥ +1.0 Vdc, V <sub>I(-)</sub> = 0, V <sub>O</sub> = 30 Vdc	I <sub>OL</sub>	-	-	1.0	-	-	1.0	-	-	1.0	μA
Differential Input Voltage  All V <sub>I</sub> ≥ 0 Vdc	V <sub>ID</sub>	-	-	V <sub>CC</sub>	-	-	V <sub>CC</sub>	-	-	V <sub>CC</sub>	Vdc

7. (LM239) T<sub>low</sub> = -25°C, T<sub>high</sub> = +85°C  
 (LM339, LM339E) T<sub>low</sub> = 0°C, T<sub>high</sub> = +70°C  
 (MC3302) T<sub>low</sub> = -40°C, T<sub>high</sub> = +85°C  
 (LM2901, LM2901E) T<sub>low</sub> = -40°C, T<sub>high</sub> = +105°C  
 (LM2901V & NCV2901) T<sub>low</sub> = -40°C, T<sub>high</sub> = +125°C  
*NCV2901 is qualified for automotive use.*

8. At the output switch point, V<sub>O</sub> ≈ 1.4 Vdc, R<sub>S</sub> ≤ 100 Ω 5.0 Vdc ≤ V<sub>CC</sub> ≤ 30 Vdc, with the inputs over the full common mode range (0 Vdc to V<sub>CC</sub> - 1.5 Vdc).  
 9. The bias current flows out of the inputs due to the PNP input stage. This current is virtually constant, independent of the output state.



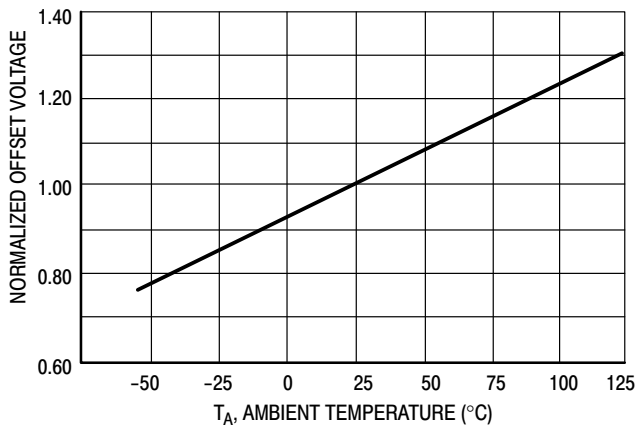
**Figure 2. Inverting Comparator with Hysteresis**



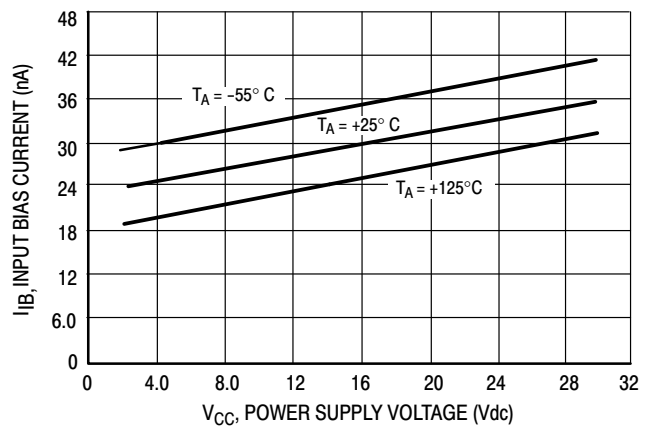
**Figure 3. Noninverting Comparator with Hysteresis**

**Typical Characteristics**

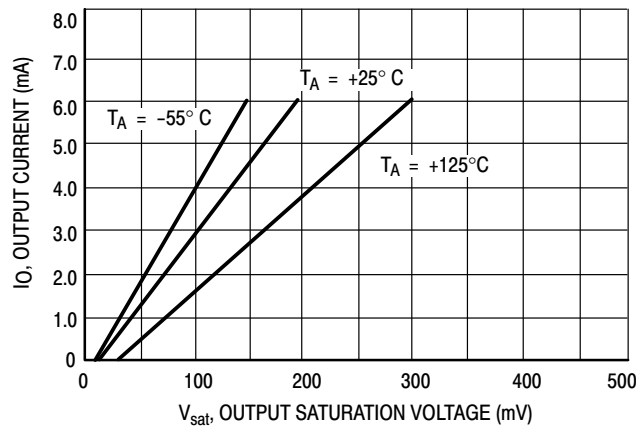
( $V_{CC} = 15 \text{ Vdc}$ ,  $T_A = +25^\circ\text{C}$  (each comparator) unless otherwise noted.)



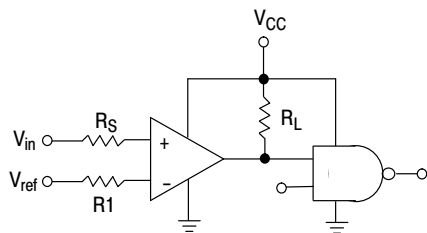
**Figure 4. Normalized Input Offset Voltage**



**Figure 5. Input Bias Current**



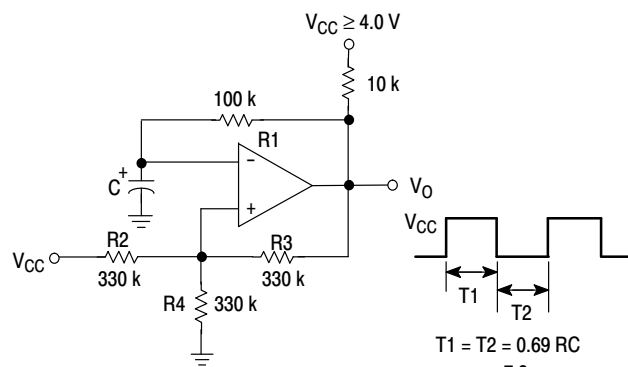
**Figure 6. Output Sink Current versus Output Saturation Voltage**



$R_S = \text{Source Resistance}$   
 $R_1 \approx R_S$

Logic	Device	$V_{CC}$ (V)	$R_L$ k $\Omega$
CMOS	1/4 MC14001	+15	100
TTL	1/4 MC7400	+5.0	10

**Figure 7. Driving Logic**



$$T_1 = T_2 = 0.69 RC$$

$$f \approx \frac{7.2}{C(\mu F)}$$

$$R_2 = R_3 = R_4$$

$$R_1 \approx R_2 // R_3 // R_4$$

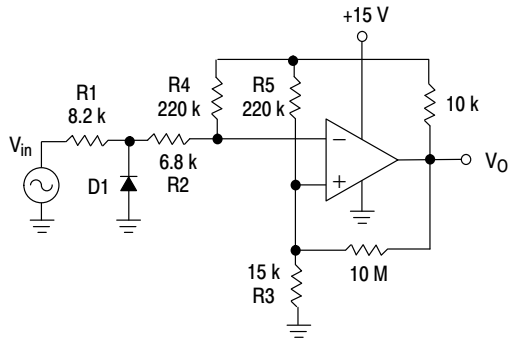
**Figure 8. Squarewave Oscillator**

APPLICATIONS INFORMATION

These quad comparators feature high gain, wide bandwidth characteristics. This gives the device oscillation tendencies if the outputs are capacitively coupled to the inputs via stray capacitance. This oscillation manifests itself during output transitions ( $V_{OL}$  to  $V_{OH}$ ). To alleviate this situation input resistors  $< 10\text{ k}\Omega$  should be used. The

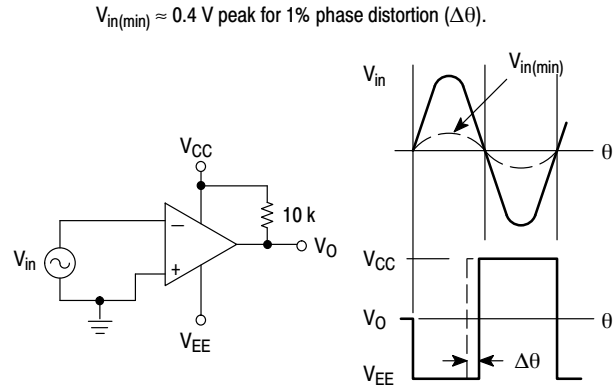
addition of positive feedback ( $< 10\text{ mV}$ ) is also recommended. It is good design practice to ground all unused input pins.

Differential input voltages may be larger than supply voltages without damaging the comparator's inputs. Voltages more negative than  $-300\text{ mV}$  should not be used.



D1 prevents input from going negative by more than  $0.6\text{ V}$ .  
 $R1 + R2 = R3$   
 $R3 \leq \frac{R5}{10}$  for small error in zero crossing

Figure 9. Zero Crossing Detector (Single Supply)



$V_{in(min)} \approx 0.4\text{ V}$  peak for 1% phase distortion ( $\Delta\theta$ ).

Figure 10. Zero Crossing Detector (Split Supplies)

# LM339, LM339E, LM239, LM2901, LM2901E, LM2901V, NCV2901, MC3302

## ORDERING INFORMATION

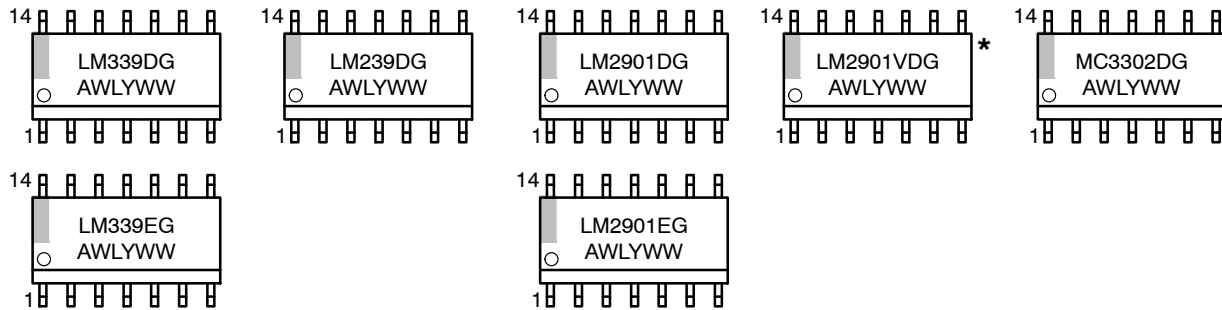
Device	Package	Shipping†
LM239DR2G	SOIC-14 (Pb-Free)	2500 / Tape & Reel
LM239DTBR2G	TSSOP-14 (Pb-Free)	2500 / Tape & Reel
LM339DR2G	SOIC-14 (Pb-Free)	2500 / Tape & Reel
LM339EDR2G	SOIC-14 (Pb-Free)	2500 / Tape & Reel
LM339DTBR2G	TSSOP-14 (Pb-Free)	2500 / Tape & Reel
LM2901DR2G	SOIC-14 (Pb-Free)	2500 / Tape & Reel
LM2901EDR2G	SOIC-14 (Pb-Free)	2500 / Tape & Reel
LM2901DTBR2G	TSSOP-14 (Pb-Free)	2500 / Tape & Reel
LM2901VDR2G	SOIC-14 (Pb-Free)	2500 / Tape & Reel
LM2901VDTBR2G	TSSOP-14 (Pb-Free)	2500 / Tape & Reel
NCV2901DR2G*	SOIC-14 (Pb-Free)	2500 / Tape & Reel
NCV2901DTBR2G*	TSSOP-14 (Pb-Free)	2500 / Tape & Reel
NCV2901CTR*	Bare Die	6000 / Tape & Reel
MC3302DR2G	SOIC-14 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

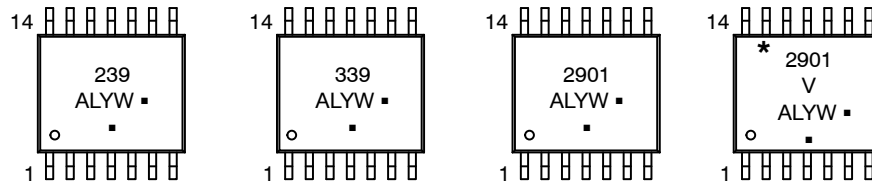
\*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

MARKING DIAGRAMS

SOIC-14  
D SUFFIX  
CASE 751A



TSSOP-14  
DTB SUFFIX  
CASE 948G



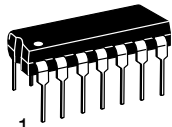
A = Assembly Location  
 WL, L = Wafer Lot  
 YY, Y = Year  
 WW, W = Work Week  
 G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

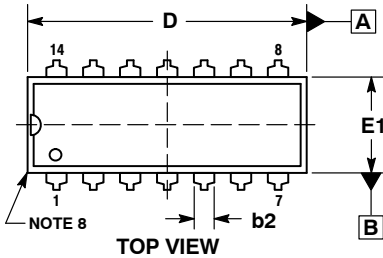
\*This marking diagram also applies to NCV2901.

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®

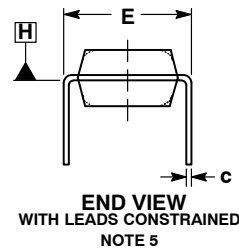


SCALE 1:1



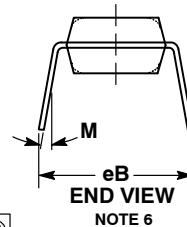
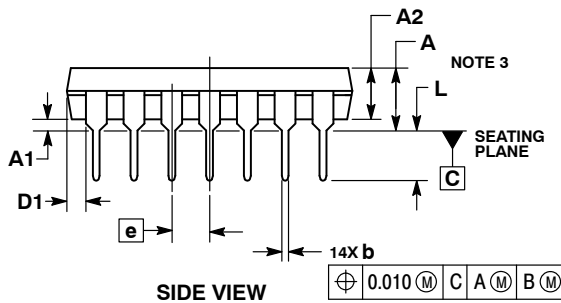
PDIP-14  
CASE 646-06  
ISSUE S

DATE 22 APR 2015



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	----	0.210	----	5.33
A1	0.015	----	0.38	----
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.735	0.775	18.67	19.69
D1	0.005	----	0.13	----
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	----	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	----	10°

GENERIC MARKING DIAGRAM\*



- XXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

STYLES ON PAGE 2

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**PDIP-14**  
**CASE 646-06**  
**ISSUE S**

DATE 22 APR 2015

**STYLE 1:**  
 PIN 1. COLLECTOR  
 2. BASE  
 3. EMITTER  
 4. NO  
**CONNECTION**  
 5. EMITTER  
 6. BASE  
 7. COLLECTOR  
 8. COLLECTOR  
 9. BASE  
 10. EMITTER  
 11. NO  
**CONNECTION**  
 12. EMITTER  
 13. BASE  
 14. COLLECTOR

**STYLE 2:**  
 CANCELLED

**STYLE 3:**  
 CANCELLED

**STYLE 4:**  
 PIN 1. DRAIN  
 2. SOURCE  
 3. GATE  
 4. NO  
**CONNECTION**  
 5. GATE  
 6. SOURCE  
 7. DRAIN  
 8. DRAIN  
 9. SOURCE  
 10. GATE  
 11. NO  
**CONNECTION**  
 12. GATE  
 13. SOURCE  
 14. DRAIN

**STYLE 5:**  
 PIN 1. GATE  
 2. DRAIN  
 3. SOURCE  
 4. NO CONNECTION  
 5. SOURCE  
 6. DRAIN  
 7. GATE  
 8. GATE  
 9. DRAIN  
 10. SOURCE  
 11. NO CONNECTION  
 12. SOURCE  
 13. DRAIN  
 14. GATE

**STYLE 6:**  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. ANODE/CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. NO CONNECTION  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

**STYLE 7:**  
 PIN 1. NO CONNECTION  
 2. ANODE  
 3. ANODE  
 4. NO CONNECTION  
 5. ANODE  
 6. NO CONNECTION  
 7. ANODE  
 8. ANODE  
 9. ANODE  
 10. NO CONNECTION  
 11. ANODE  
 12. ANODE  
 13. NO CONNECTION  
 14. COMMON  
 CATHODE

**STYLE 8:**  
 PIN 1. NO CONNECTION  
 2. CATHODE  
 3. CATHODE  
 4. NO CONNECTION  
 5. CATHODE  
 6. NO CONNECTION  
 7. CATHODE  
 8. CATHODE  
 9. CATHODE  
 10. NO CONNECTION  
 11. CATHODE  
 12. CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

**STYLE 9:**  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. ANODE/CATHODE  
 7. COMMON ANODE  
 8. COMMON ANODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. NO CONNECTION  
 12. ANODE/CATHODE  
 13. ANODE/CATHODE  
 14. COMMON CATHODE

**STYLE 10:**  
 PIN 1. COMMON  
 CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. COMMON ANODE  
 8. COMMON  
 CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

**STYLE 11:**  
 PIN 1. CATHODE  
 2. CATHODE  
 3. CATHODE  
 4. CATHODE  
 5. CATHODE  
 6. CATHODE  
 7. CATHODE  
 8. ANODE  
 9. ANODE  
 10. ANODE  
 11. ANODE  
 12. ANODE  
 13. ANODE  
 14. ANODE

**STYLE 12:**  
 PIN 1. COMMON CATHODE  
 2. COMMON ANODE  
 3. ANODE/CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. COMMON ANODE  
 7. COMMON CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. ANODE/CATHODE  
 14. ANODE/CATHODE

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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

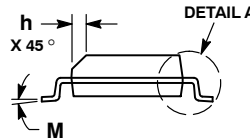
ON Semiconductor®



SCALE 1:1

SOIC-14 NB  
CASE 751A-03  
ISSUE L

DATE 03 FEB 2016



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°

SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM\*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

STYLES ON PAGE 2

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**SOIC-14**  
**CASE 751A-03**  
**ISSUE L**

DATE 03 FEB 2016

STYLE 1:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. ANODE/CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. NO CONNECTION  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 2:  
 CANCELLED

STYLE 3:  
 PIN 1. NO CONNECTION  
 2. ANODE  
 3. ANODE  
 4. NO CONNECTION  
 5. ANODE  
 6. NO CONNECTION  
 7. ANODE  
 8. ANODE  
 9. ANODE  
 10. NO CONNECTION  
 11. ANODE  
 12. ANODE  
 13. NO CONNECTION  
 14. COMMON CATHODE

STYLE 4:  
 PIN 1. NO CONNECTION  
 2. CATHODE  
 3. CATHODE  
 4. NO CONNECTION  
 5. CATHODE  
 6. NO CONNECTION  
 7. CATHODE  
 8. CATHODE  
 9. CATHODE  
 10. NO CONNECTION  
 11. CATHODE  
 12. CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 5:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. COMMON ANODE  
 8. COMMON CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 6:  
 PIN 1. CATHODE  
 2. CATHODE  
 3. CATHODE  
 4. CATHODE  
 5. CATHODE  
 6. CATHODE  
 7. CATHODE  
 8. ANODE  
 9. ANODE  
 10. ANODE  
 11. ANODE  
 12. ANODE  
 13. ANODE  
 14. ANODE

STYLE 7:  
 PIN 1. ANODE/CATHODE  
 2. COMMON ANODE  
 3. COMMON CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. ANODE/CATHODE  
 7. ANODE/CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. COMMON CATHODE  
 12. COMMON ANODE  
 13. ANODE/CATHODE  
 14. ANODE/CATHODE

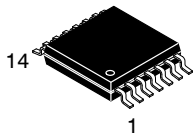
STYLE 8:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. ANODE/CATHODE  
 7. COMMON ANODE  
 8. COMMON ANODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. NO CONNECTION  
 12. ANODE/CATHODE  
 13. ANODE/CATHODE  
 14. COMMON CATHODE

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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



**TSSOP-14 WB**  
CASE 948G  
ISSUE C

DATE 17 FEB 2016

SCALE 2:1

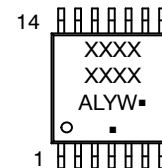


**NOTES:**

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

**GENERIC MARKING DIAGRAM\***

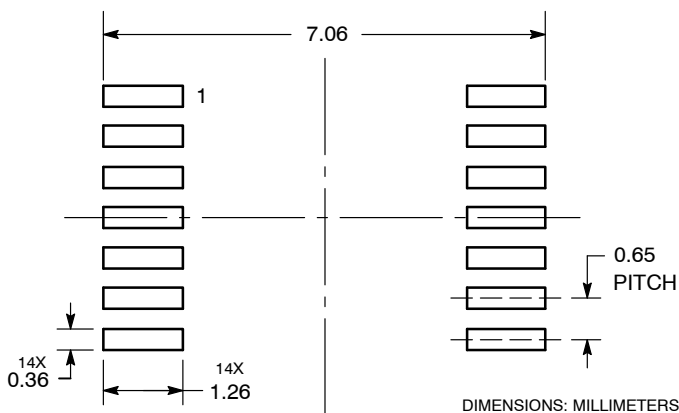


- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

**SOLDERING FOOTPRINT**



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