Serially Interfaced, +2.7V to +5.5V, 5- and 8-Digit LED Display Drivers

ABSOLUTE MAXIMUM RATINGS

Voltage (with Respect to GND)
V+.....-0.3V to 6V
All Other Pins.....-0.3V to (V+ + 0.3V)
DIG1–DIG8 Sink Current..... 440mA
SEG1–SEG9 Source Current..... 55mA
Continuous Power Dissipation (T_A = +70°C)
16-Pin QSOP (derate 8.34mW/°C above +70°C).....667mW

Operating Temperature Ranges (T_{MIN} to T_{MAX})
MAX695_CEE.....0°C to +70°C
MAX695_EEE.....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range.....-65°C to +150°C
Lead Temperature (soldering, 10s).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Typical operating circuit, V+ = +3.0V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Voltage	V+			2.7		5.5	V
Shutdown Supply Current	I_{SHDN}	Shutdown mode, all digital inputs at V+ or GND	Overtemperature		75		µA
			T_A = +25°C		62	160	
Operating Supply Current	I+	All segments on, all digits scanned, intensity set to full, internal oscillator, no display load connected			10	15	mA
Master Clock Frequency (OSC Internal Oscillator)	f_{OSC}	OSC = RC oscillator		1		8	MHz
		OSC = RC oscillator, R_{SET} = 56kΩ, C_{SET} = 27pF			4		
Master Clock Frequency (OSC External Clock)	f_{OSC}	OSC overdriven externally		1		8	MHz
Display Scan Rate (OSC External Clock)	f_{SCAN}	Eight digits scanned, OSC = overdriven externally		155		1250	Hz
Display Scan Rate (OSC Internal Oscillator)	f_{SCAN}	Eight digits scanned, OSC = RC oscillator		155		1250	Hz
Display Scan Rate (OSC Internal Oscillator)	f_{SCAN}	Eight digits scanned, OSC = RC oscillator, R_{SET} = 56kΩ, C_{SET} = 27pF			625		Hz
OSC Internal/External Detection Threshold	V_{OSC}				1.7		V
Dead Clock Protection Frequency	f_{OSC}				75.5		kHz
OSC High Time (OSC External Clock)	t_{CH}			50			ns
OSC Low Time (OSC External Clock)	t_{CL}			50			ns

ELECTRICAL CHARACTERISTICS

(Typical operating circuit, V+ = +3.0V to +5.5V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Slow Segment Blink Period (Internal Oscillator)	$f_{SLOWBLINK}$	Eight digits scanned, OSC = RC oscillator, R_{SET} = 56kΩ, C_{SET} = 27pF		1		s
Fast Segment Blink Period (Internal Oscillator)	$f_{FASTBLINK}$	Eight digits scanned, OSC = RC oscillator, R_{SET} = 56kΩ, C_{SET} = 27pF		0.5		s
Fast or Slow Segment Blink Duty Cycle (Note 2)			49.9	50	50.1	%
Digit Drive Sink Current	I_{DIGIT}	T_A = +25°C, V_{LED} = 2.4V	240	320	400	mA
Segment Drive Source Current	I_{SEG}	T_A = +25°C, V_{LED} = 2.4V	-30	-40	-50	mA
Digit Drive Sink Current (Note 2)	I_{DIGIT}	T_A = +25°C, V+ = 2.7V to 3V, V_{LED} = 2.2V	80			mA
Segment Drive Source Current (Note 2)	I_{SEG}	T_A = +25°C, V+ = 2.7V to 3V, V_{LED} = 2.2V	-10			mA
Slew Rate Rise Time	$\Delta I_{SEG}/\Delta t$	T_A = +25°C		35		mA/µs
LOGIC INPUTS						
Input Current DIN, CLK, $\overline{CS}$	I_{IH}, I_{IL}	V_{IN} = 0 or V+	-2		2	µA
Logic High Input Voltage DIN, CLK, $\overline{CS}$	V_{IH}		2.4			V
Logic Low Input Voltage DIN, CLK, $\overline{CS}$	V_{IL}				0.4	V
Hysteresis Voltage DIN, CLK, $\overline{CS}$	ΔV_I			0.5		V
TIMING CHARACTERISTICS (Figure 1)						
CLK Clock Period	t_{CP}		38.4			ns
CLK Pulse Width High	t_{CH}		19			ns
CLK Pulse Width Low	t_{CL}		19			ns
$\overline{CS}$ Fall to CLK Rise Setup Time	t_{CSS}		9.5			ns
CLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		3			ns
DIN Setup Time	t_{DS}		9.5			ns
DIN Hold Time	t_{DH}		0			ns
$\overline{CS}$ Pulse High	t_{CSW}		19			ns
TIMING CHARACTERISTICS (V+ = +2.7V) (Note 2)						
CLK Clock Period	t_{CP}		50			ns
CLK Pulse Width High	t_{CH}		24			ns
CLK Pulse Width Low	t_{CL}		24			ns
$\overline{CS}$ Fall to CLK Rise Setup Time	t_{CSS}		12			ns
CLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		4			ns
DIN Setup Time	t_{DS}		12			ns
DIN Hold Time	t_{DH}		4			ns
$\overline{CS}$ Pulse High	t_{CSW}		24			ns

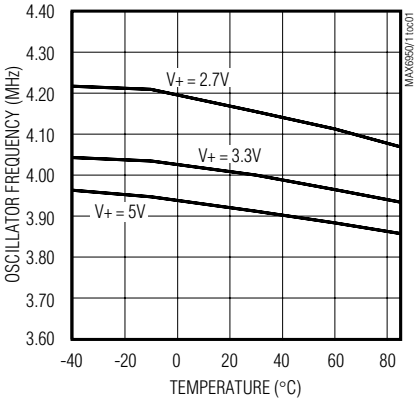
Note 1: All parameters tested at T_A = +25°C. Specifications over temperature are guaranteed by design.
Note 2: Guaranteed by design.

Serially Interfaced, +2.7V to +5.5V, 5- and 8-Digit LED Display Drivers

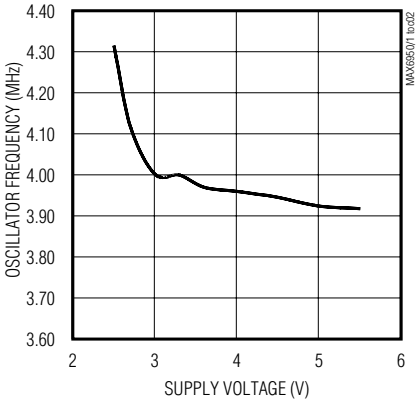
Typical Operating Characteristics

(Typical operating circuit, scan limit set to eight digits, V+ = +3.3V, V_{LED} = 2.4V, T_A = +25°C, unless otherwise noted.)

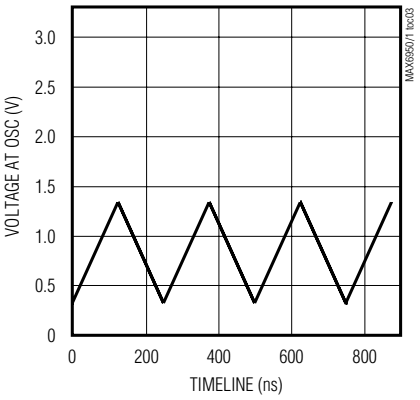
INTERNAL OSCILLATOR FREQUENCY vs. TEMPERATURE



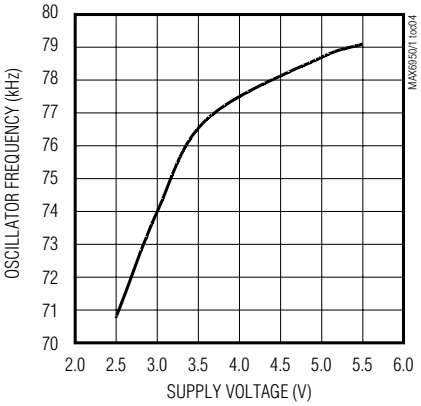
INTERNAL OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE



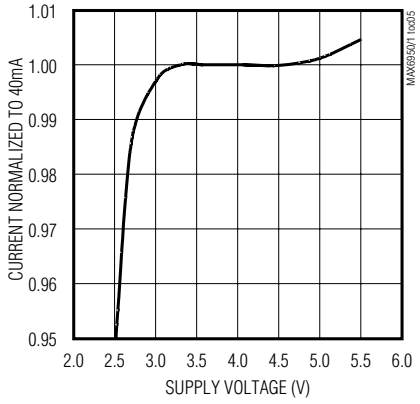
INTERNAL OSCILLATOR WAVEFORM AT OSC (PIN 9)



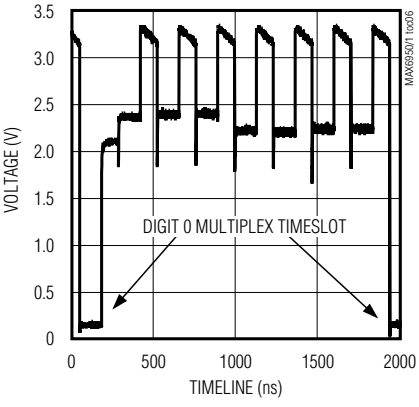
DEAD CLOCK OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE



SEGMENT SOURCE CURRENT vs. SUPPLY VOLTAGE



WAVEFORM AT SEG0/DIG0 (PIN 6) V+ = 3.3V, 8 DIGITS SCANNED, 8/16 INTENSITY



Pin Description

PIN	NAME	FUNCTION
1	DIN	Serial Data Input. Data is loaded into the internal 16–bit Shift register on CLK's rising edge.
2	CLK	Serial-Clock Input. On CLK's rising edge, data is shifted into the Internal Shift register. On CLK's falling edge, data is clocked out of DOUT. CLK input is active only while $\overline{CS}$ is low.
3–6, 10–14	DIGX, SEGX	Digit X outputs sink current from the display common cathode when acting as digit drivers. Segment X drivers source current to the display. Segment/digit drivers are high impedance when turned off.
7	I_{SET}	Current Setting. Connect to GND through a resistor (R_{SET}) to set the peak current. This resistor, together with capacitor C_{SET}, also sets the multiplex clock frequency.
8	GND	Ground
9	OSC	Multiplexer Clock Input. A capacitor (C_{SET}) is connected to GND when the internal RC oscillator multiplex clock is used. Resistor R_{SET} (also used to set the peak current) and capacitor C_{SET} together set the multiplex clock frequency. When the external clock is used, OSC should be driven by a 1MHz to 8MHz clock.
15	$\overline{CS}$	Chip-Select Input. Serial data is loaded into the Shift register while $\overline{CS}$ is low. The last 16 bits of serial data are latched on $\overline{CS}$'s rising edge.
16	V+	Positive Supply Voltage. Bypass to GND with a 0.1µF capacitor.
PAD	Exposed pad	Exposed pad on package underside. Connect to GND.

Detailed Description

Differences Between MAX6950 and MAX6951

The MAX6950 is a five-digit common-cathode display driver. It drives five digits, with each digit comprising eight LEDs with cathodes connected to a common cathode. The display limit is therefore 40 LEDs or digit segments.

The MAX6951 is an eight-digit common-cathode display driver. It drives eight digits, with each digit comprising eight LEDs. The only difference between the MAX6950 and MAX6951 is that the MAX6950 is missing three digit drivers. The MAX6950 can be configured to scan eight digits, but if the last three digits are wired up, they do not light.

The MAX6950/MAX6951 use a unique multiplexing scheme to minimize the connections between the driver and LED display. The scheme requires that the segment connections are different to each of the five (MAX6950) or eight (MAX6951) digits (Table 1). This is shown in the *Typical Application Circuit*, which uses single-digit type displays. The MAX6950/MAX6951 are not intended to drive multidigit display types, which have the segments internally wired together, unless the segments are wired with the common cathodes to follow Table 1. The MAX6950/MAX6951 can drive multidigit LED displays that have the segments individually pinned for each digit because then the digits can be connected together correctly externally, just as if individual digits were used.

Serial-Addressing Modes

The microprocessor interface on the MAX6950/MAX6951 is a SPI-compatible 3-wire serial interface using three input pins (Figure 1). This interface is used to write configuration and display data to the MAX6950/MAX6951. The serial interface data word length is 16 bits, which are labeled D15–D0 (Table 2). D15–D8 contain the command address, and D7–D0 contain the data. The first bit received is D15, the most-significant bit (MSB). The three input pins are:

- CLK is the serial clock input, and may idle low or high at the start and end of a write sequence.
- $\overline{CS}$ is the MAX6950/MAX6951s' chip-select input, and must be low to clock data into the MAX6950/MAX6951.
- DIN is the serial data input, and must be stable when it is sampled on the rising edge of the clock.

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Table 1. Standard Driver Connection to Single-Digit Displays

	DIG/SEG0 PIN 6	DIG/SEG1 PIN 5	DIG/SEG2 PIN 4	DIG/SEG3 PIN 3	DIG/SEG4 PIN 14	DIG/SEG5 PIN 13	DIG/SEG6 PIN 12	DIG/SEG7 PIN 11	SEG 8 PIN 10
LED Digit 0	**CC0**	SEG dp	SEG g	SEG f	SEG e	SEG d	SEG c	SEG b	SEG a
LED Digit 1	SEG dp	**CC1**	SEG g	SEG f	SEG e	SEG d	SEG c	SEG b	SEG a
LED Digit 2	SEG dp	SEG g	**CC2**	SEG f	SEG e	SEG d	SEG c	SEG b	SEG a
LED Digit 3	SEG dp	SEG g	SEG f	**CC3**	SEG e	SEG d	SEG c	SEG b	SEG a
LED Digit 4	SEG dp	SEG g	SEG f	SEG e	**CC4**	SEG d	SEG c	SEG b	SEG a
LED Digit 5	SEG dp	SEG g	SEG f	SEG e	SEG d	**CC5**	SEG c	SEG b	SEG a
LED Digit 6	SEG dp	SEG g	SEG f	SEG e	SEG d	SEG c	**CC6**	SEG b	SEG a
LED Digit 7	SEG dp	SEG g	SEG f	SEG e	SEG d	SEG c	SEG b	**CC7**	SEG a

Table 2. Serial-Data Format (16 Bits)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ADDRESS								MSB	DATA						LSB

The serial interface comprises a 16-bit shift register into which DIN data is clocked on the rising edge of CLK when $\overline{CS}$ is low. When $\overline{CS}$ is high, transitions on CLK do not clock data into the shift register. When $\overline{CS}$ goes high, the 16 bits in the shift register are parallel loaded into a 16-bit latch. The 16 bits in the latch are then decoded to determine and execute the command.

The MAX6950/MAX6951 are written to using the following sequence (Figure 2):

1) Take CLK low.
2) Take $\overline{CS}$ low. This enables the internal 16-bit shift register.
3) Clock 16 bits of data in order, D15 first to D0 last, into DIN, observing the setup and hold times.
4) Take $\overline{CS}$ high.

CLK and DIN may well be used to transmit data to other peripherals. The MAX6950/MAX6951 ignore all activity on CLK and DIN except when $\overline{CS}$ is low. Data cannot be read from the MAX6950/MAX6951.

If fewer or greater than 16 bits are clocked into the MAX6950/MAX6951 between taking $\overline{CS}$ low and taking $\overline{CS}$ high again, the MAX6950/MAX6951 store the last 16 bits received, including the previous transmission(s). The general case is when n bits (where n > 16) are transmitted to the MAX6950/MAX6951. The last bits comprising bits {n-15} to {n} are retained and are parallel loaded into the 16-bit latch as bits D15 to D0, respectively (Figure 3).

Digit and Control Registers

Table 3 lists the addressable Digit and Configuration registers. The digit registers are implemented by two planes of 8-byte dual-port SRAM, P0 and P1.

Initial Power-Up

On initial power-up, all control registers are reset, the display is blanked, and the MAX6950/MAX6951 enter shutdown mode. Program the display driver prior to display use. Otherwise, it is initially set to scan five digits, it does not decode data in the data registers, and the Intensity register is set to its minimum value. Table 4 lists the register status after power-up.

Configuration Register

The configuration register is used to enter and exit shutdown, select the blink rate, globally enable and disable the blink function, globally clear the digit data, and reset the blink timing. Bit position D1 should always be written with a zero when the configuration register is updated. See Table 5 for configuration register format.

The S bit selects shutdown or normal operation.

The B bit selects the blink rate.

The E bit globally enables or disables the blink function.

The T bit resets the blink timing.

The R bit globally clears the digit data for both planes P0 and P1 for all digits.

When the MAX6950/MAX6951 are in shutdown mode (Table 6), the scan oscillator is halted; all segment and digit drivers are high impedance. Data in the digit and

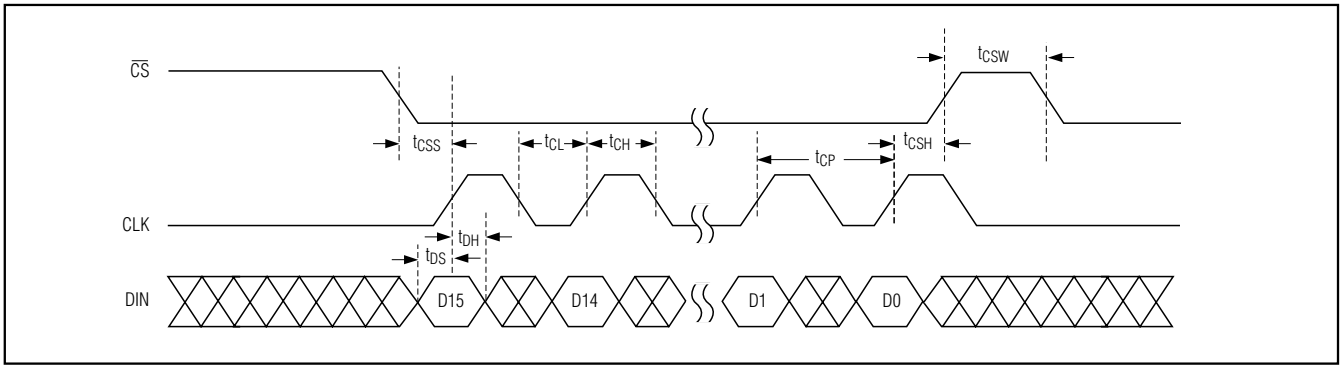

Figure 1. Timing Diagram

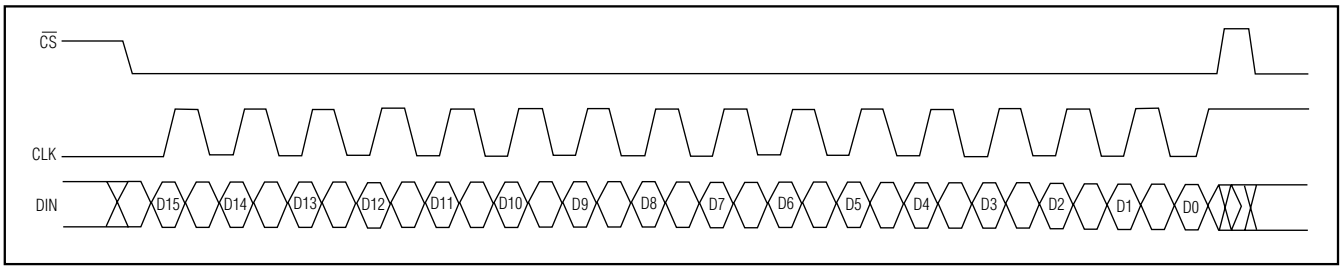

Figure 2. Transmission of 16 Bits to the MAX6950/MAX6951

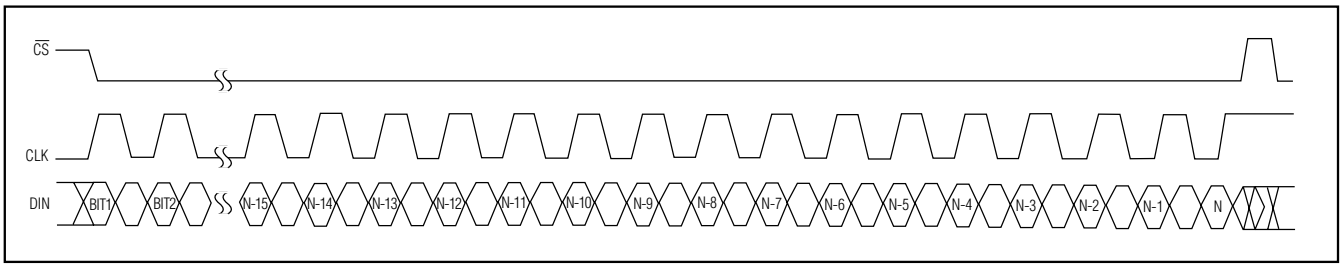

Figure 3 . Transmission of More than 16 Bits to the MAX6950/MAX6951

control registers remains unaltered. Shutdown can be used to save power. For minimum supply current in shutdown mode, logic inputs should be at ground or V+ (CMOS-logic levels). The display driver can be programmed while in shutdown mode, and shutdown mode can be overridden by the display test function.

Table 7 lists the blink rate selection format.

If blink is globally enabled by setting the E bit of the configuration register (Table 8), then the digit data in both planes P0 and P1 are used to control the display (Table 9).

When the global blink timing synchronization bit is set, the multiplex and blink timing counter is cleared on the rising edge of $\overline{CS}$. By setting the T bit in multiple MAX6950/MAX6951s at the same time (or in quick succession), the blink timing can be synchronized across all the devices.

When the global digit data clear (R data bit D5) is set, the digit data for both planes P0 and P1 for ALL digits is cleared on the rising edge of $\overline{CS}$. Digits with decode enabled display the zero. Digits without decode enabled show all segments unlit.

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Table 3. Register Address Map

REGISTER	COMMAND ADDRESS								HEX CODE
	D15	D14	D13	D12	D11	D10	D9	D8	
No-Op	0	0	0	0	0	0	0	0	0x00
Decode Mode	0	0	0	0	0	0	0	1	0x01
Intensity	0	0	0	0	0	0	1	0	0x02
Scan Limit	0	0	0	0	0	0	1	1	0x03
Configuration	0	0	0	0	0	1	0	0	0x04
Factory reserved. Do not write to this.	0	0	0	0	0	1	1	0	0x06
Display Test	0	0	0	0	0	1	1	1	0x07
Digit 0 plane P0 only (plane 1 unchanged)	0	0	1	0	0	0	0	0	0x20
Digit 1 plane P0 only (plane 1 unchanged)	0	0	1	0	0	0	0	1	0x21
Digit 2 plane P0 only (plane 1 unchanged)	0	0	1	0	0	0	1	0	0x22
Digit 3 plane P0 only (plane 1 unchanged)	0	0	1	0	0	0	1	1	0x23
Digit 4 plane P0 only (plane 1 unchanged)	0	0	1	0	0	1	0	0	0x24
Digit 5 plane P0 only (plane 1 unchanged)	0	0	1	0	0	1	0	1	0x25
Digit 6 plane P0 only (plane 1 unchanged)	0	0	1	0	0	1	1	0	0x26
Digit 7 plane P0 only (plane 1 unchanged)	0	0	1	0	0	1	1	1	0x27
Digit 0 plane P1 only (plane 0 unchanged)	0	1	0	0	0	0	0	0	0x40
Digit 1 plane P1 only (plane 0 unchanged)	0	1	0	0	0	0	0	1	0x41
Digit 2 plane P1 only (plane 0 unchanged)	0	1	0	0	0	0	1	0	0x42
Digit 3 plane P1 only (plane 0 unchanged)	0	1	0	0	0	0	1	1	0x43
Digit 4 plane P1 only (plane 0 unchanged)	0	1	0	0	0	1	0	0	0x44
Digit 5 plane P1 only (plane 0 unchanged)	0	1	0	0	0	1	0	1	0x45
Digit 6 plane P1 only (plane 0 unchanged)	0	1	0	0	0	1	1	0	0x46
Digit 7 plane P1 only (plane 0 unchanged)	0	1	0	0	0	1	1	1	0x47
Digit 0 plane P0 and plane P1 (with same data)	0	1	1	0	0	0	0	0	0x60
Digit 1 plane P0 and plane P1 (with same data)	0	1	1	0	0	0	0	1	0x61
Digit 2 plane P0 and plane P1 (with same data)	0	1	1	0	0	0	1	0	0x62
Digit 3 plane P0 and plane P1 (with same data)	0	1	1	0	0	0	1	1	0x63
Digit 4 plane P0 and plane P1 (with same data)	0	1	1	0	0	1	0	0	0x64
Digit 5 plane P0 and plane P1 (with same data)	0	1	1	0	0	1	0	1	0x65
Digit 6 plane P0 and plane P1 (with same data)	0	1	1	0	0	1	1	0	0x66
Digit 7 plane P0 and plane P1 (with same data)	0	1	1	0	0	1	1	1	0x67

No-Op Register

The no-op register is used when the MAX6950/MAX6951 are connected as the last device on a chain of cascaded SPI devices. To write the other cascaded device(s), ensure that while the intended device receives its specific command, the MAX6950/MAX6951 receive a no-op command.

Display-Test Register

The display-test register switches the drivers between one of two modes: normal and display test. Display-test mode turns all LEDs on by overriding, but not altering, all control and digit registers (including the Shutdown register) In display-test mode, eight digits are scanned and the duty cycle is 7/16 (half power). Table 11 lists the display-test register format.

Table 4. Initial Power-Up Register Status

REGISTER	POWER-UP CONDITION	ADDRESS CODE (HEX)	REGISTER DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
Decode	No decode for digits 7–0	0x01	0	0	0	0	0	0	0	0
Intensity	1/16 (min on)	0x02	X	X	X	X	0	0	0	0
Scan Limit	Display 5 digits: 0 1 2 3 4	0x03	X	X	X	X	X	1	0	0
Configuration	Shutdown enabled/blink speed is slow/blink disabled	0x04	X	X	X	0	0	0	0	0
Display Test	Normal operation	0x07	X	X	X	X	X	X	X	0
Digit 0	Blank digit, both planes	0x60	0	0	0	0	0	0	0	0
Digit 1	Blank digit, both planes	0x61	0	0	0	0	0	0	0	0
Digit 2	Blank digit, both planes	0x62	0	0	0	0	0	0	0	0
Digit 3	Blank digit, both planes	0x63	0	0	0	0	0	0	0	0
Digit 4	Blank digit, both planes	0x64	0	0	0	0	0	0	0	0
Digit 5	Blank digit, both planes	0x65	0	0	0	0	0	0	0	0
Digit 6	Blank digit, both planes	0x66	0	0	0	0	0	0	0	0
Digit 7	Blank digit, both planes	0x67	0	0	0	0	0	0	0	0

Scan-Limit Register

The scan-limit register sets how many digits are displayed, from one to eight digits. It is possible to set the MAX6950 (the five-digit part) to scan six, seven, or eight digits. The MAX6951 set to eight digits displays five digits less brightly than if it had been set to scan five digits, but the brightness would match that of a MAX6951 used in the same system if the Intensity registers are set to the same value. For example, consider an 11-digit requirement. This can be served by using a MAX6950 to drive five digits plus a MAX6951 to drive six digits. Both parts are configured to drive six digits to ensure the brightness is the same.

The digits are displayed in a multiplexed manner with a typical display scan rate of 1kHz with five digits displayed or 625Hz with eight digits displayed with f_{OSC} = 4MHz. Since the number of scanned digits affects the display brightness, the Scan-Limit register should not be used to blank portions of the display (such as for leading-zero suppression). Table 12 lists the scan-limit register format.

Intensity Register

Digital control of display brightness is provided by an internal pulse-width modulator, which is controlled by the lower nibble of the intensity register (Figure 4). The modulator scales the average segment current in 16 steps from a minimum of 15/16 down to 1/16 of the peak current. The minimum interdigit blanking time is set to 1/16 of a cycle. See Table 13 for Intensity register format.

Decode Mode Register

The decode mode register sets hexadecimal code (0–9, A–F) or no-decode operation for each digit. Each bit in the register corresponds to one digit. A logic high selects hexadecimal code font decoding for that digit, while logic low bypasses the decoder. Digits may be set for decode or no-decode in any combination. Examples of the decode mode control register format are shown in Table 14.

When the hexadecimal code-decode mode is used, the decoder looks only at the lower nibble of the data in the digit register (D3–D0), disregarding bits D6–D4. D7, which sets the decimal point (SEG DP), is independent of the decoder, and is positive logic (D7 = 1 turns the decimal point on). Table 15 lists the hexadecimal code font. When no-decode is selected, data bits D7–D0 correspond to the segment lines of the MAX6950/MAX6951. Table 15 shows the one-to-one pairing of each data bit to the appropriate segment line.

Display Digit Registers

The MAX6950/MAX6951 use a digit register to store the data that the user wishes to display on the LED digits. These digit registers are implemented by two planes of 8-byte, dual-port SRAM, called P0 and P1. The digit registers are dual port to enable them to be written to through the SPI interface, asynchronous to being read to multiplex the display.

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Table 5. Configuration Register Format

MODE	ADDRESS CODE (HEX)	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Configuration register	0x04	X	X	R	T	E	B	0	S

Table 6. Shutdown Control (S Data Bit D0) Format

MODE	ADDRESS CODE (HEX)	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Shutdown	0x04	X	X	R	T	E	B	0	0
Normal operation	0x04	X	X	R	T	E	B	0	1

Table 7. Blink Rate Selection (B Data Bit D2) Format

MODE	ADDRESS CODE (HEX)	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Slow-blinking segments blink on for 1s, off for 1s with f_{OSC} = 4MHz	0x04	X	X	R	T	E	0	0	S
Fast-blinking segments blink on for 0.5s, off for 0.5s with f_{OSC} = 4MHz	0x04	X	X	R	T	E	1	0	S

Table 8. Global Blink Enable/Disable (E Data Bit D3) Format

MODE	ADDRESS CODE (HEX)	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Blink function is disabled	0x04	X	X	R	T	0	B	0	S
Blink function is enabled	0x04	X	X	R	T	1	B	0	S

Table 9. Global Blink Timing Synchronization (T Data Bit D4) Format

MODE	ADDRESS CODE (HEX)	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Blink timing counters are unaffected	0x04	X	X	R	0	E	B	0	S
Blink timing counters are cleared on the rising edge of $\overline{CS}$	0x04	X	X	R	1	E	B	0	S

Each LED digit is represented by 2 bytes of memory, 1 byte in plane P0 and the other in plane P1. Each LED digit's segment is represented by 2 bits of memory, 1 bit from the appropriate byte in each plane. The digit registers are mapped so that a digit's data can be updated in plane P0, or plane P1, or both planes at the same time (Table 3).

Table 10. Global Clear Digit Data (R Data Bit D5) Format

MODE	ADDRESS CODE (HEX)	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Digit data for both planes P0 and P1 are unaffected	0x04	X	X	0	T	E	B	0	S
Digit data for both planes P0 and P1 are cleared on the rising edge of $\overline{CS}$	0x04	X	X	1	T	E	B	0	S

Table 11. Display-Test Register Format

MODE	ADDRESS CODE (HEX)	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Normal operation	0x07	X	X	X	X	X	X	X	0
Display test	0x07	X	X	X	X	X	X	X	1

Table 12. Scan-Limit Register Format

SCAN LIMIT	ADDRESS CODE (HEX)	REGISTER DATA								HEX CODE
		D7	D6	D5	D4	D3	D2	D1	D0	
Display digit 0 only	0x03	X	X	X	X	X	0	0	0	0xX0
Display digits 0 and 1	0x03	X	X	X	X	X	0	0	1	0xX1
Display digits 0 and 1 2	0x03	X	X	X	X	X	0	1	0	0xX2
Display digits 0 and 1 2 3	0x03	X	X	X	X	X	0	1	1	0xX3
Display digits 0 and 1 2 3 4	0x03	X	X	X	X	X	1	0	0	0xX4
Display digits 0 and 1 2 3 4 5	0x03	X	X	X	X	X	1	0	1	0xX5
Display digits 0 and 1 2 3 4 5 6	0x03	X	X	X	X	X	1	1	0	0xX6
Display digits 0 and 1 2 3 4 5 6 7	0x03	X	X	X	X	X	1	1	1	0xX7

If the blink function is disabled through the Blink Enable Bit E (Table 8) in the configuration register, then the digit register data in plane P0 is used to multiplex the display. The digit register data in P1 is not used (Table 17).

If the blink function is enabled, then the digit register data in both plane P0 and plane P1 are alternately used to multiplex the display. Blinking is achieved by multiplexing the LED display using data plane P0 and plane P1 on alternate phases of the blink clock (Table 18).

Display Blink Mode

The display blinking facility, when enabled, makes the driver flip automatically between displaying the digit register data in planes P0 and plane P1. If the digit register data for any individual segment is different in the two planes, then that segment appears to blink or flash on and off. Once blinking has been configured, it continues automatically without further intervention.

Blink Speed

The blink speed is determined by frequency of the multiplex clock, OSC, and by the setting of the Blink Rate Selection Bit B (Table 7) in the configuration register. The Blink Rate Selection Bit B sets either fast or slow blink speed for the whole display.

Multiplex Clock and OSC Oscillator

The OSC input pin is used to set both the display scan rate and the blink timing for the display driver. OSC must either be fitted with an external capacitor C_{SET} to GND to set the frequency of the MAX6950/MAX6951s' internal RC oscillator, or be overdriven with an external TTL/CMOS clock.

Serially Interfaced, +2.7V to +5.5V, 5- and 8-Digit LED Display Drivers

Table 13. Intensity Register Format

DUTY CYCLE	TYPICAL SEGMENT CURRENT (mA)	ADDRESS CODE (HEX)	D7	D6	D5	D4	D3	D2	D1	D0	HEX CODE
1/16 (min on)	2.5	0x02	X	X	X	X	0	0	0	0	0xX0
2/16	5	0x02	X	X	X	X	0	0	0	1	0xX1
3/16	7.5	0x02	X	X	X	X	0	0	1	0	0xX2
4/16	10	0x02	X	X	X	X	0	0	1	1	0xX3
5/16	12.5	0x02	X	X	X	X	0	1	0	0	0xX4
6/16	15	0x02	X	X	X	X	0	1	0	1	0xX5
7/16	17.5	0x02	X	X	X	X	0	1	1	0	0xX6
8/16	20	0x02	X	X	X	X	0	1	1	1	0xX7
9/16	22.5	0x02	X	X	X	X	1	0	0	0	0xX8
10/16	25	0x02	X	X	X	X	1	0	0	1	0xX9
11/16	27.5	0x02	X	X	X	X	1	0	1	0	0xXA
12/16	30	0x02	X	X	X	X	1	0	1	1	0xXB
13/16	32.5	0x02	X	X	X	X	1	1	0	0	0xXC
14/16	35	0x02	X	X	X	X	1	1	0	1	0xXD
15/16	37.5	0x02	X	X	X	X	1	1	1	0	0xXE
15/16 (max on)	37.5	0x02	X	X	X	X	1	1	1	1	0xXF

The allowed range of the frequency at the OSC pin, f_{OSC}, is 1MHz to 8MHz, which allows the blink frequency to be adjusted over a wide range. The internal oscillator may be accurate enough for many applications using a single device. If an exact or synchronized blink rate is required, then OSC should be driven by an external clock.

The display scan rate (defined in the *Electrical Characteristics* table) is calculated by dividing f_{OSC} by 4000 for the MAX6950 (scanning a full five digits), or by 6400 for the MAX6951 (scanning a full eight digits). The display scan rate is the refresh rate for all the digits of the display. With f_{OSC} at 4MHz, each display digit is enabled for 200µs.

There is a fail-safe circuit in the MAX6950/MAX6951 to ensure the display multiplexing works if the OSC is configured incorrectly. This ensures that the driver cannot remain stuck on a single digit, forcing a peak current continuously through segments. The fail-safe circuit detects that f_{OSC} is too slow, and generates extra clock transitions to guarantee a minimum effective clock of typically 75.5kHz. The scan rate for eight digits is about 11Hz in fail-safe mode, and appears to flicker to most observers. A flickering display is a good indication that there is a problem with the multiplex clock. The clock failure detection works regardless of the clock source being the internal RC oscillator or external clock drive.

The RC oscillator uses an external resistor R_{SET} (which also sets the peak segment current) and an external capacitor C_{SET} to set the oscillator frequency. The recommended values of R_{SET} and C_{SET} set the oscillator at 4MHz, which makes the slow and fast blink frequency 0.5Hz and 1Hz, respectively.

Synchronization of Blinking Across Multiple MAX6950/MAX6951 Drivers

The OSC inputs of multiple MAX6950/MAX6951 drivers can be connected together to an external clock to make the devices blink at the same frequency. Segment blinking may be synchronized across multiple MAX6950/MAX6951s so that all drivers blink not only at the same frequency, but also in phase. When the control register is written with the T bit set (Table 9), the OSC divider chain is cleared and the display multiplexing sequence reset. To synchronize several drivers, it is necessary to write this register in all drivers at the same time. In practice, adequate synchronization can be achieved by writing to multiple drivers in quick succession.

When the global blink timing synchronization bit is set, the multiplexing and blink counter is cleared on the rising edge of $\overline{CS}$. By setting the T bit in multiple MAX6950/MAX6951s at the same time (or in quick succession), the blink timing can be synchronized across all the devices. Note that the display multiplexing

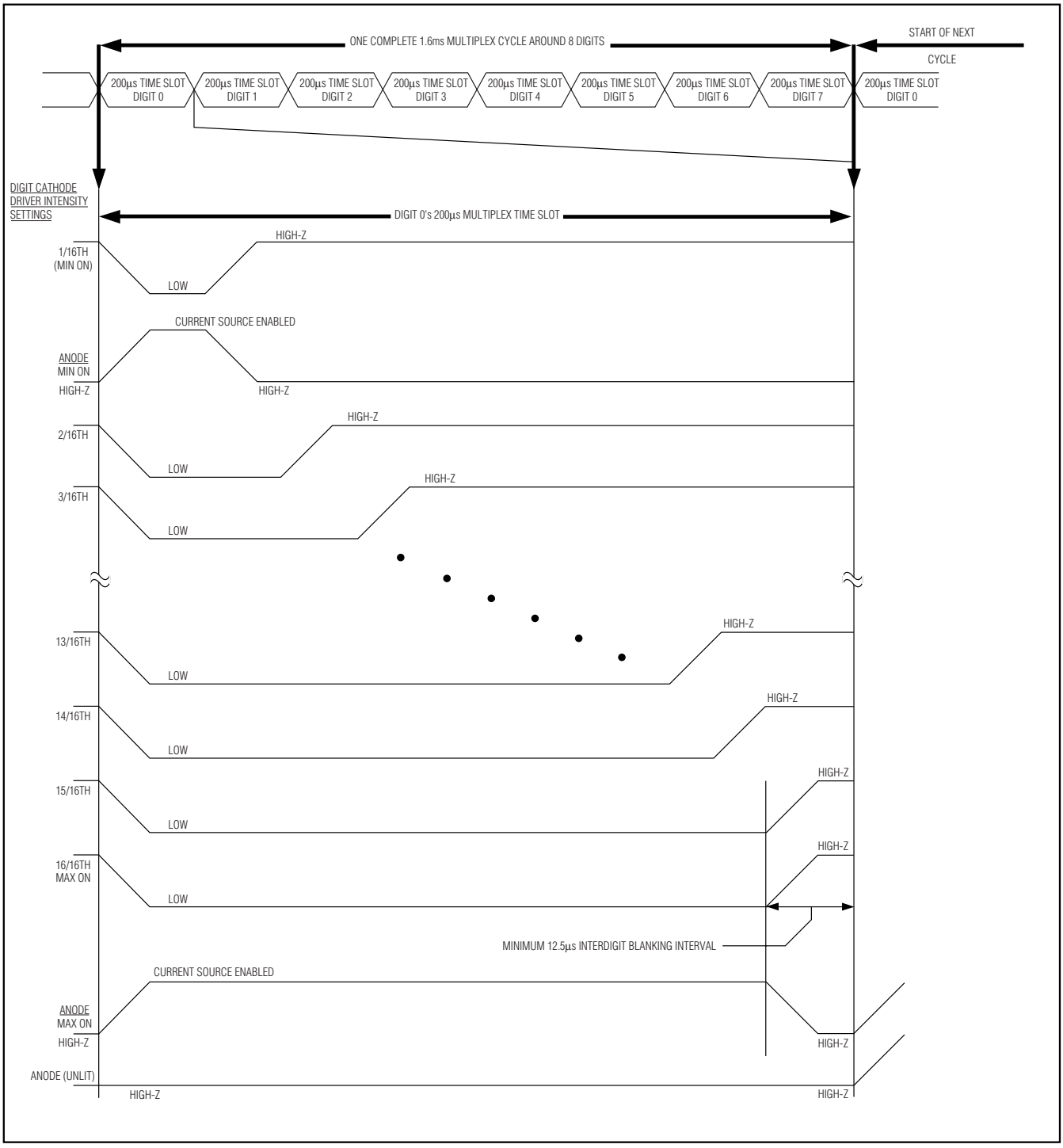


Figure 4. Multiplex and Intensity Timing Diagram

Serially Interfaced, +2.7V to +5.5V, 5- and 8-Digit LED Display Drivers

Table 14. Decode-Mode Register Examples

DECODE CODE	ADDRESS CODE (HEX)	REGISTER DATA								HEX CODE
		D7	D6	D5	D4	D3	D2	D1	D0	
No decode for digits 7–0	0x01	0	0	0	0	0	0	0	0	0x00
Hexadecimal decode for digit 0, no decode for digits 7–1	0x01	0	0	0	0	0	0	0	1	0x01
Hexadecimal decode for digits 2–0, no decode for digits 7–3	0x01	0	0	0	0	0	1	1	1	0x07
Hexadecimal decode for digits 7–0	0x01	1	1	1	1	1	1	1	1	0xFF

Table 15. Hexadecimal Font

7-SEGMENT CHARACTER	REGISTER DATA						ON SEGMENTS = 1							
	D7*	D6–D4	D3	D2	D1	D0	dp*	a	b	c	d	e	f	g
0		X	0	0	0	0		1	1	1	1	1	1	0
1		X	0	0	0	1		0	1	1	0	0	0	0
2		X	0	0	1	0		1	1	0	1	1	0	1
3		X	0	0	1	1		1	1	1	1	0	0	1
4		X	0	1	0	0		0	1	1	0	0	1	1
5		X	0	1	0	1		1	0	1	1	0	1	1
6		X	0	1	1	0		1	0	1	1	1	1	1
7		X	0	1	1	1		1	1	1	0	0	0	0
8		X	1	0	0	0		1	1	1	1	1	1	1
9		X	1	0	0	1		1	1	1	1	0	1	1
A		X	1	0	1	0		1	1	1	0	1	1	1
B		X	1	0	1	1		0	0	1	1	1	1	1
C		X	1	1	0	0		1	0	0	1	1	1	0
D		X	1	1	0	1		0	1	1	1	1	1	1
E		X	1	1	1	0		1	0	0	1	1	1	1
F		X	1	1	1	1		1	0	0	0	1	1	1

The decimal point segment is lit when bit D7 = 1.

sequence is also reset, which might give rise to a one-time display flicker when the register is written.

Selecting External Components R_{SET} and C_{SET} to Set Oscillator Frequency and Segment Current

The RC oscillator uses an external resistor R_{SET} and an external capacitor C_{SET} to set the oscillator frequency, f_{OSC}. The allowed range of f_{OSC} is 1MHz to 8MHz. R_{SET} also sets the peak segment current. The recommended values of R_{SET} and C_{SET} set the oscillator to 4MHz, which makes the blink frequencies 0.5Hz and 1Hz. The recommended value of R_{SET} also sets the peak current to 40mA, which makes the segment current adjustable from 2.5mA to 37.5mA in 2.5mA steps.

$$I_{SEG} = K_I / R_{SET}\ mA$$

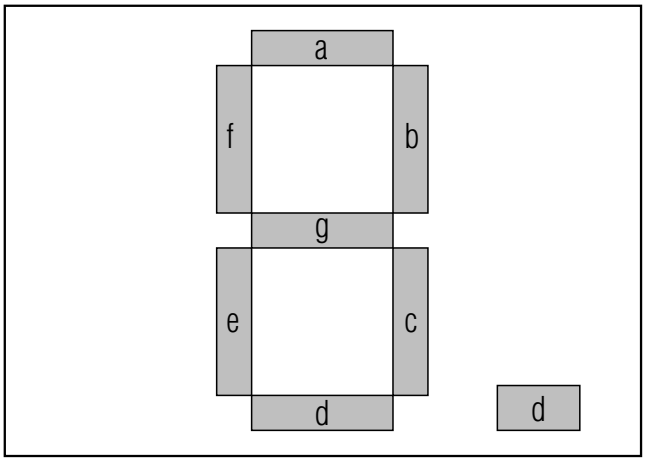
$$f_{OSC} = K_F / (R_{SET} \times C_{SET} + C_{STRAY})\ MHz$$

Where:

$K_I = 2240$

Table 16. No-Decode Mode Data Bits and Corresponding Segment Lines

	REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
Segment line	dp	a	b	c	d	e	f	g



K_F = 6720

R_{SET} = external resistor in kΩ

C_{SET} = external capacitor in pF

C_{STRAY} = stray capacitance from OSC pin to GND in pF, typically 3pF

The recommended value of R_{SET} is 56kΩ and the recommended value of C_{SET} is 27pF.

The recommended value of R_{SET} is the minimum allowed value, since it sets the display driver to the maximum allowed segment current. R_{SET} can be set to a higher value to set the segment current to a lower peak value where desired. The user must also ensure that the peak current specifications of the LEDs connected to the driver are not exceeded.

The effective value of C_{SET} includes not only the actual external capacitor used, but also the stray capacitance from the OSC pin to GND. This capacitance is usually in the 1pF to 5pF range, depending on the layout used.

LED Maximum Reverse Voltage

The display connection scheme used by the MAX6950/MAX6951 puts LED segments in reverse bias during a portion of the multiplexing time. The maximum applied reverse bias voltage is the value of the supply voltage, V+. It is therefore important to ensure that the LEDs chosen are rated to withstand a reverse bias equal to the maximum supply voltage applied to the MAX6950/MAX6951.

Applications Information

Choosing Supply Voltage to Minimize Power Dissipation

The MAX6950/MAX6951 drive a peak current of 40mA into LEDs with a 2.4V forward-voltage drop when operated from a supply voltage of at least 3.0V. The minimum voltage drop across the internal LED drivers is therefore (3.0V - 2.4V) = 0.6V. If a higher supply voltage is used, the driver absorbs a higher voltage, and the driver's power dissipation increases accordingly. However, if the LEDs used have a higher forward voltage drop than 2.4V, the supply voltage must be raised accordingly to ensure that the driver always has at least 0.6V headroom.

The voltage drop across the drivers with a nominal +5V supply (5.0V - 2.4V) = 2.6V is nearly 3 times the drop across the drivers with a nominal 3.3V supply (3.3V - 2.4V) = 0.9V. In many systems, consumption is an important design criterion, and the MAX6950/MAX6951 should be operated from the system's 3.3V nominal supply. In other designs, the lowest supply voltage may be 5V. The issue now is to ensure the dissipation limit for the MAX6950/MAX6951 is not exceeded. This can be achieved by inserting a series resistor in the supply to the MAX6950/MAX6951, ensuring that the supply decoupling capacitors are still on the MAX6950/MAX6951 side of the resistor. For example, consider the requirement that the minimum supply voltage to a MAX6951 must be 3.0V, and the input supply range is 5V ±5%. Maximum supply current is 15mA + (40mA × 8) = 335mA. Minimum input supply voltage is 4.75V. Maximum series resistor value is (4.75V - 3.0V)/0.335A = 5.2Ω. We choose 4.7Ω ±10%. Worst-case resistor dissipation is at maximum toleranced resistance, i.e., $(0.335A)^2 \times (4.7\Omega \times 1.1) = 0.584W$. We choose a 1W resistor rating. The maximum MAX6951 supply voltage is at maximum input supply voltage and minimum toleranced resistance, i.e., 5.25V - (0.335A × 4.7Ω × 0.9) = 3.83V.

Low-Voltage Operation

The MAX6950/MAX6951 work over the +2.7V to +5.5V supply range. The minimum useful supply voltage is determined by the forward voltage drop of the LEDs at the peak current I_{SEG}, plus the 0.6V headroom required by the driver output stages. The MAX6950/MAX6951 correctly regulate I_{SEG} with a supply above this minimum voltage. If the supply drops below this minimum voltage, the driver output stages may brown out, and

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Table 17. Digit Register Mapping with Blink Globally Disabled

SEGMENT'S BIT SETTING IN PLANE P1	SEGMENT'S BIT SETTING IN PLANE P0	SEGMENT BEHAVIOR
X	0	Segment off during both halves of each blink period
X	1	Segment off during both halves of each blink period

Table 18. Digit Register Mapping with Blink Globally Enabled

SEGMENT'S BIT SETTING IN PLANE P1	SEGMENT'S BIT SETTING IN PLANE P0	SEGMENT BEHAVIOR
0	0	Segment off
0	1	Segment on only during the 1st half of each blink period
1	0	Segment on only during the 2nd half of each blink period
1	1	Segment on

be unable to regulate the current correctly. As the supply voltage drops further, the LED segment drive current becomes effectively limited by the output drivers' on-resistance, and the LED drive current drops. The characteristics of each individual LED in a modern 7-segment digit usually match well, so the result is that the display intensity dims uniformly as supply voltage drops out of regulation and beyond. The MAX6950/MAX6951 operate down to 2V supply voltage (although most displays are very dim at this voltage), providing that the MAX6950/MAX6951 are powered up initially to at least 2.7V to trigger the device's internal reset, and also that the SPI interface is constrained to 5Mbps.

Computing Power Dissipation

The upper limit for power dissipation (PD) for the MAX6950/MAX6951 is determined from the following equation:

$$P_D = (V+ \times I+) + (V+ - V_{LED}) (DUTY \times I_{SEG} \times N)$$

Where:

V+ = supply voltage

DUTY = duty cycle set by intensity register

N = number of segment driven (worst case is 8)

V_{LED} = LED forward voltage

I_{SEG} = segment current set by R_{SET}

PD = power dissipation, in mW if currents are in mA

Dissipation example:

I_{SEG} = 40mA, N = 8, Duty = 15/16, V_{LED} = 2.4V at 40mA, V+ = 3.6V

P_D = 3.6V (15mA) + (3.6V - 2.4V)(15 / 16 × 40mA x 8) = 0.414W

Thus, for the 16-pin QSOP package (T_{JA} = 1/0.00834 = +120°C/W), the maximum allowed ambient temperature T_A is given by:

$T_{J\,(MAX)} = T_A + (P_D \times T_{JA}) = +150°C = T_A + (0.44 \times +120°C/W)$

So T_A = +100°C. Thus, the device can be operated safely at a maximum package temperature of +85°C.

Power Supplies

The MAX6950/MAX6951 operate from a single +2.7V to +5.5V power supply. Bypass the power supply to ground with a 0.1µF capacitor as close to the pin as possible. Add a 22µF capacitor if the MAX6950/MAX6951 are not close to the board's input bulk decoupling capacitor.

Connect the underside exposed pad to GND.

Board Layout

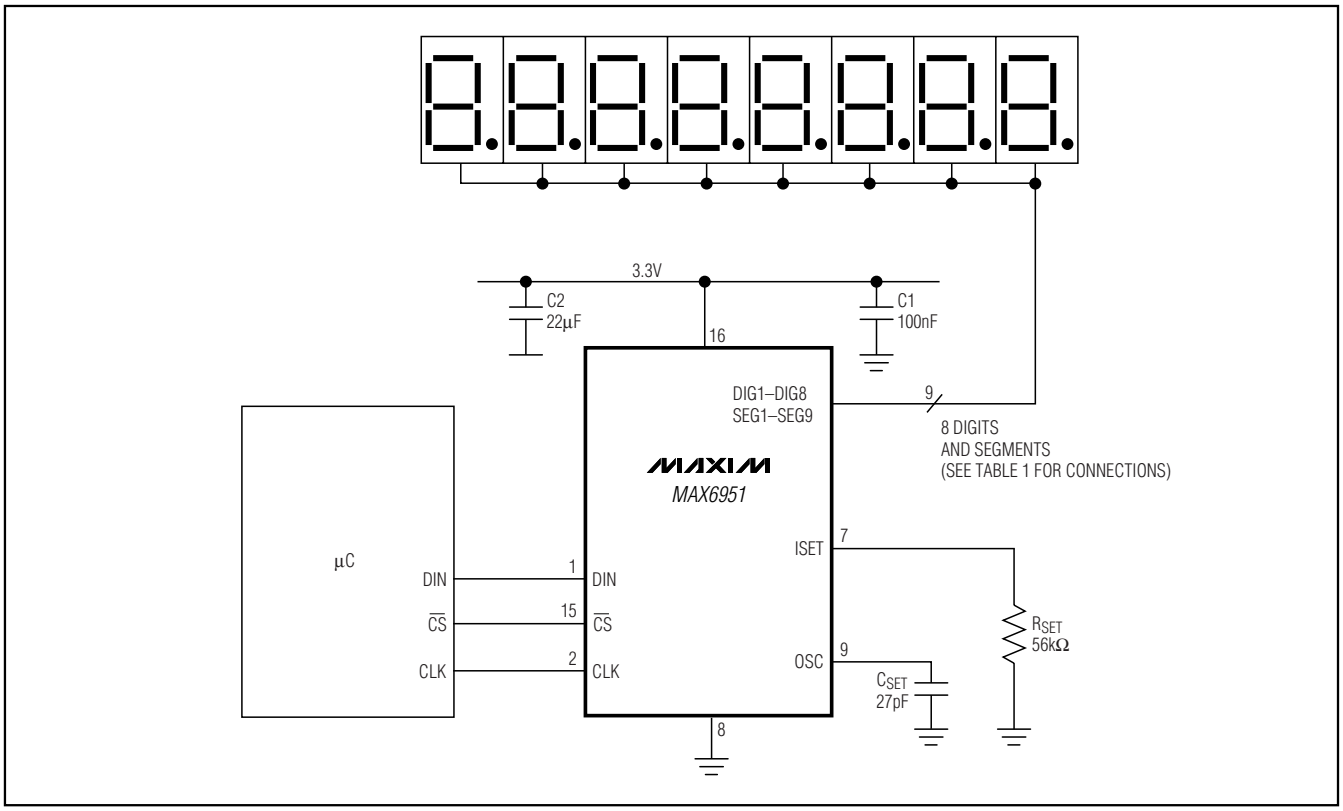
When designing a board, use the following guidelines:

1. The R_{SET} connection to pin 7 is a high-impedance node, and sensitive to layout. Place R_{SET} right next to pins 7 and 8 and route R_{SET} directly to these pins with very short tracks.

2. Ensure that the track from the ground end of R_{SET} routes directly to pin 8, and that this track is not used as part of any other ground connection.

Figure 5 shows a good layout. The decoupling capacitors C1 (ceramic) and C2 (bulk, if required) are located above the IC. The ground track to R_{SET} is a separate track from both the IC's power ground connection and the ground plane.

Typical Application Circuit



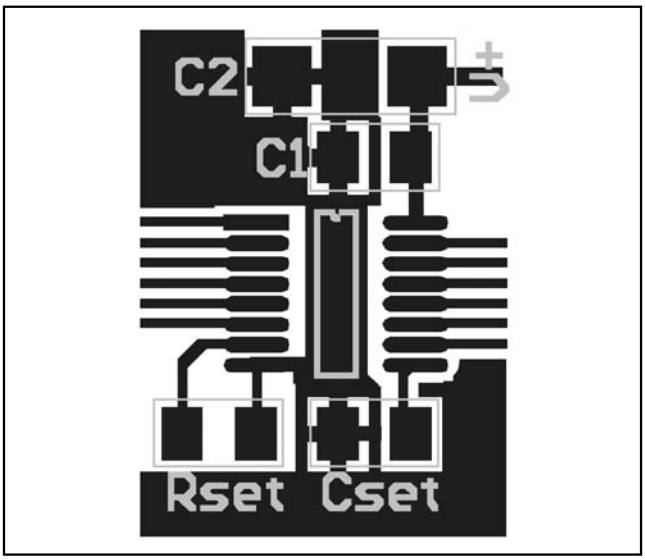


Figure 5. Sample Board Layout

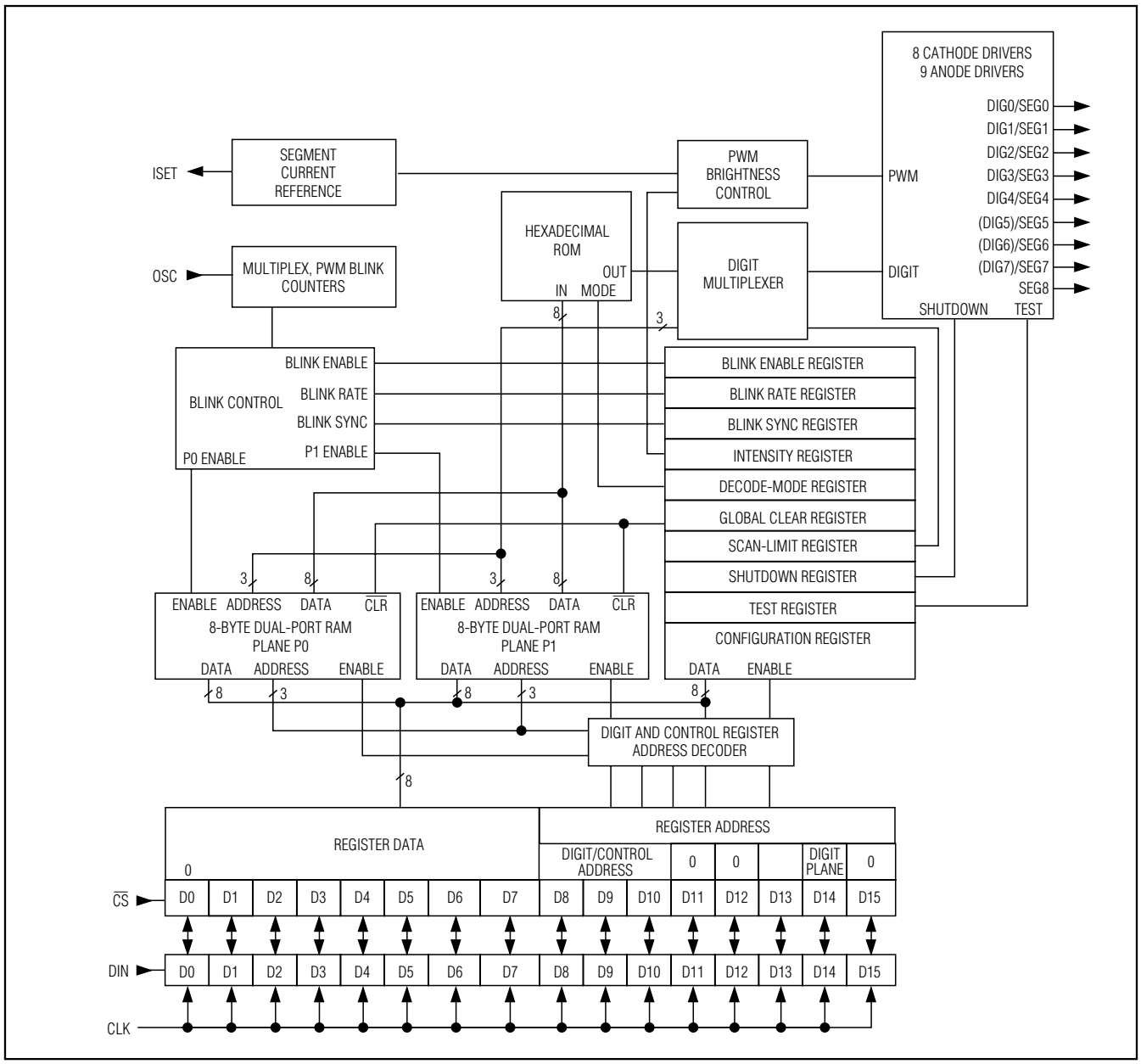
Chip Information

TRANSISTOR COUNT: 17,350

PROCESS: CMOS

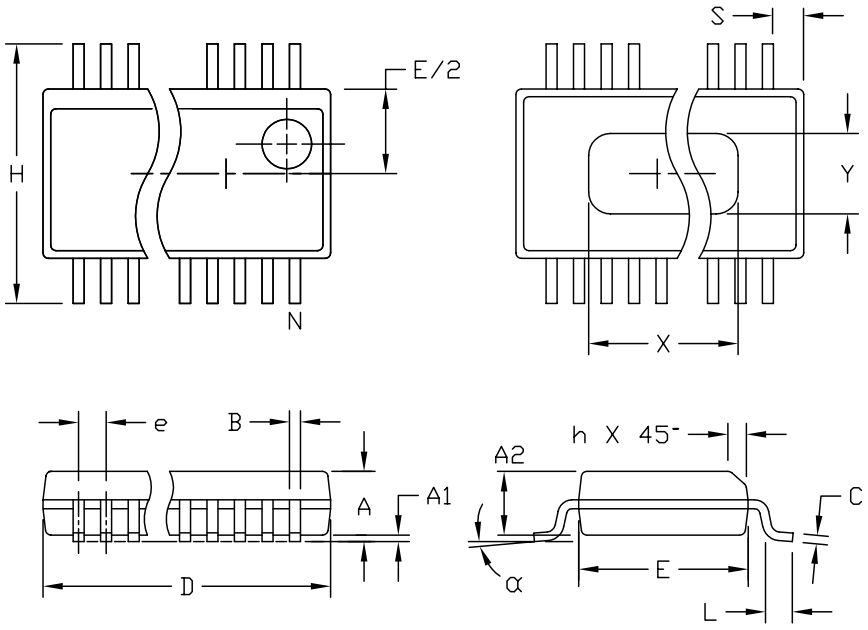
Serially Interfaced, +2.7V to +5.5V, 5- and 8-Digit LED Display Drivers

Functional Diagram



Package Information

QSOP.EPS



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
X	SEE VARIATIONS			
Y	.071	.087	1.803	2.209
α	0°	8°	0°	8°

VARIATIONS:

	INCHES		MILLIMETERS			
	MIN.	MAX.	MIN.	MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
X	.107	.123	2.72	3.12		
D	.337	.344	8.56	8.74	20	AB
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AC
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AD
S	.0250	.0300	0.635	0.762		
X	.271	.287	6.88	7.29		

NOTES:
1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3. HEAT SLUG DIMENSIONS X AND Y APPLY ONLY TO 16 AND 28 LEAD POWER-QSOP PACKAGES.
4. CONTROLLING DIMENSIONS: INCHES.
5. MEETS JEDEC MO137.

MAXIM
PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, QSOP, .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0055	C	1/1

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Maxim Integrated:

MAX6951CEE+ MAX6951EEE+ MAX6950CEE+ MAX6950CEE+T MAX6950EEE+ MAX6950EEE+T MAX6951CEE+T MAX6951EEE+T