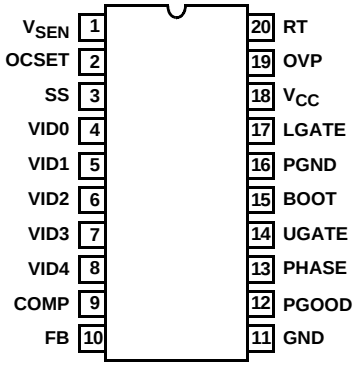
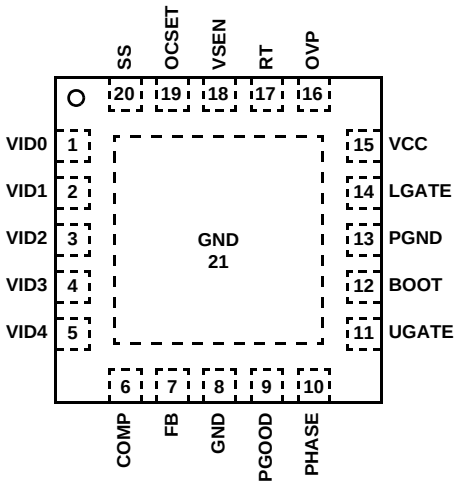
Pinouts

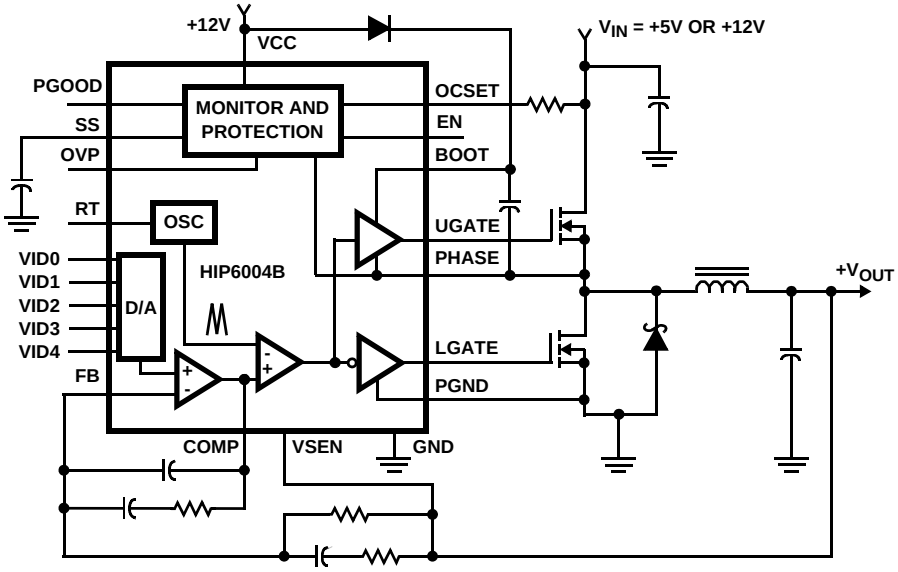
HIP6004B (SOIC, TSSOP)
TOP VIEW



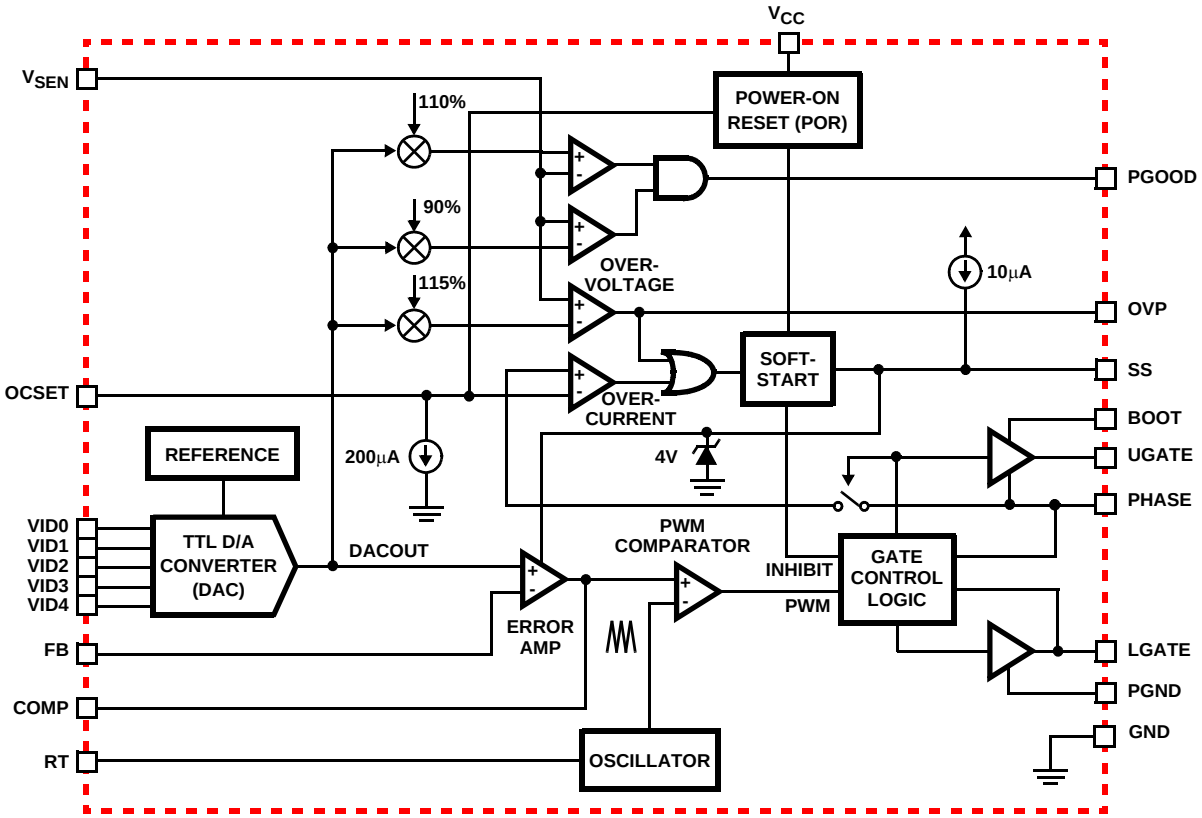
HIP6004B (QFN)
TOP VIEW



Typical Application



Block Diagram



Absolute Maximum Ratings

Supply Voltage, V_{CC} . . . . . +15V
Boot Voltage, V_{BOOT} - V_{PHASE} . . . . . +15V
Input, Output or I/O Voltage . . . . . GND -0.3V to V_{CC} +0.3V
ESD Classification . . . . . Class 2

Operating Conditions

Supply Voltage, V_{CC} . . . . . +12V ±10%
Ambient Temperature Range . . . . . 0^oC to 70^oC

Thermal Information

Thermal Resistance	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
SOIC Package (Note 1)	65	NA
TSSOP Package (Note 1)	85	NA
QFN Package (Notes 2, 3)	33	5

Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
3. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} SUPPLY CURRENT						
Nominal Supply	I_{CC}	UGATE and LGATE Open	-	5	-	mA
POWER-ON RESET						
Rising V_{CC} Threshold		V_{OCSET} = 4.5V	-	-	10.4	V
Falling V_{CC} Threshold		V_{OCSET} = 4.5V	8.2	-	-	V
Rising V_{OCSET} Threshold			-	1.26	-	V
OSCILLATOR						
Free Running Frequency		RT = OPEN	185	200	215	kHz
Total Variation		6kΩ < RT to GND < 200kΩ	-15	-	+15	%
Ramp Amplitude	ΔV_{OSC}	RT = Open	-	1.9	-	V_{P-P}
REFERENCE AND DAC						
DAC (VID0-VID4) Input Low Voltage			-	-	0.8	V
DAC (VID0-VID4) Input High Voltage			2.0	-	-	V
DACOUT Voltage Accuracy			-1.0	-	+1.0	%
ERROR AMPLIFIER						
DC Gain			-	88	-	dB
Gain-Bandwidth Product	GBW		-	15	-	MHz
Slew Rate	SR	COMP = 10pF	-	6	-	V/μs
GATE DRIVERS						
Upper Gate Source	I_{UGATE}	V_{BOOT} - V_{PHASE} = 12V, V_{UGATE} = 6V	350	500	-	mA
Upper Gate Sink	R_{UGATE}	I_{LGATE} = 0.3A	-	5.5	10	Ω
Lower Gate Source	I_{LGATE}	V_{CC} = 12V, V_{LGATE} = 6V	300	450	-	mA
Lower Gate Sink	R_{LGATE}	I_{LGATE} = 0.3A	-	3.5	6.5	Ω
PROTECTION						
Over-Voltage Trip (V_{SEN}/DACOUT)			-	115	120	%
OCSET Current Source	I_{OCSET}	V_{OCSET} = 4.5V_{DC}	170	200	230	μA
OVP Sourcing Current	I_{OVP}	V_{SEN} = 5.5V, V_{OVP} = 0V	60	-	-	mA
Soft Start Current	I_{SS}		-	10	-	μA

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER GOOD						
Upper Threshold (V_{SEN}/DACOUT)		V_{SEN} Rising	106	-	111	%
Lower Threshold (V_{SEN}/DACOUT)		V_{SEN} Falling	89	-	94	%
Hysteresis (V_{SEN}/DACOUT)		Upper and Lower Threshold	-	2	-	%
PGOOD Voltage Low	V_{PGOOD}	I_{PGOOD} = -5mA	-	0.5	-	V

Typical Performance Curves

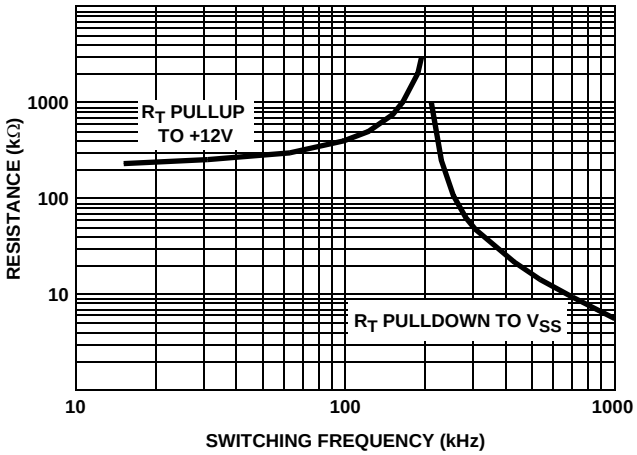


FIGURE 1. R_T RESISTANCE vs FREQUENCY

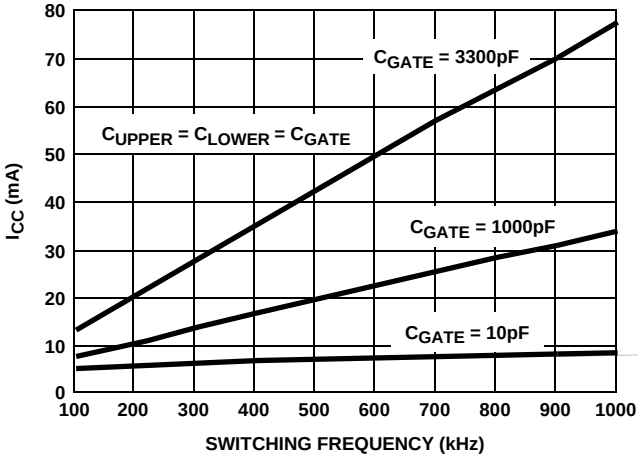
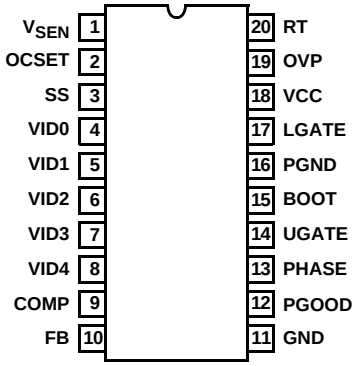


FIGURE 2. BIAS SUPPLY CURRENT vs FREQUENCY

Functional Pin Descriptions



V_{SEN} (Pin 1)

This pin is connected to the converters output voltage. The PGOOD and OVP comparator circuits use this signal to report output voltage status and for overvoltage protection.

OCSET (Pin 2)

Connect a resistor (R_{OCSET}) from this pin to the drain of the upper MOSFET. R_{OCSET}, an internal 200µA current source (I_{OCS}), and the upper MOSFET on-resistance ($r_{DS(ON)}$) set the converter over-current (OC) trip point according to the following equation:

$$I_{PEAK} = \frac{I_{OCSET} \times R_{OCSET}}{r_{DS(ON)}}$$

An over-current trip cycles the soft-start function.

SS (Pin 3)

Connect a capacitor from this pin to ground. This capacitor, along with an internal 10µA current source, sets the soft-start interval of the converter.

VID0-4 (Pins 4-8)

VID0-4 are the input pins to the 5-bit DAC. The states of these five pins program the internal voltage reference (DACOUT). The level of DACOUT sets the converter output voltage. It also sets the PGOOD and OVP thresholds. Table 1 specifies DACOUT for the all combinations of DAC inputs.

COMP (Pin 9) and FB (Pin 10)

COMP and FB are the available external pins of the error amplifier. The FB pin is the inverting input of the error amplifier and the COMP pin is the error amplifier output. These pins are used to compensate the voltage-control feedback loop of the converter.

GND (Pin 11)

Signal ground for the IC. All voltage levels are measured with respect to this pin.

PGOOD (Pin 12)

PGOOD is an open collector output used to indicate the status of the converter output voltage. This pin is pulled low when the converter output is not within ±10% of the DACOUT reference voltage. Exception to this behavior is the '11111' VID pin combination which disables the converter; in this case PGOOD asserts a high level.

PHASE (Pin 13)

Connect the PHASE pin to the upper MOSFET source. This pin is used to monitor the voltage drop across the MOSFET for over-current protection. This pin also provides the return path for the upper gate drive.

UGATE (Pin 14)

Connect UGATE to the upper MOSFET gate. This pin provides the gate drive for the upper MOSFET.

BOOT (Pin 15)

This pin provides bias voltage to the upper MOSFET driver. A bootstrap circuit may be used to create a BOOT voltage suitable to drive a standard N-Channel MOSFET.

PGND (Pin 16)

This is the power ground connection. Tie the lower MOSFET source to this pin.

LGATE (Pin 17)

Connect LGATE to the lower MOSFET gate. This pin provides the gate drive for the lower MOSFET.

V_{CC} (Pin 18)

Provide a 12V bias supply for the chip to this pin.

OVP (Pin 19)

The OVP pin can be used to drive an external SCR in the event of an overvoltage condition. Output rising 15% more than the DAC-set voltage triggers a high output on this pin and disables PWM gate drive circuitry.

RT (Pin 20)

This pin provides oscillator switching frequency adjustment. By placing a resistor (R_T) from this pin to GND, the nominal 200kHz switching frequency is increased according to the following equation:

$$Fs \approx 200kHz + \frac{5 \times 10^6}{R_T(k\Omega)} \quad (R_T \text{ to GND})$$

Conversely, connecting a pull-up resistor (R_T) from this pin to V_{CC} reduces the switching frequency according to the following equation:

$$Fs \approx 200kHz - \frac{4 \times 10^7}{R_T(k\Omega)} \quad (R_T \text{ to 12V})$$

Functional Description

Initialization

The HIP6004B automatically initializes upon receipt of power. Special sequencing of the input supplies is not necessary. The Power-On Reset (POR) function continually monitors the input supply voltages. The POR monitors the bias voltage at the V_{CC} pin and the input voltage (V_{IN}) on the OCSET pin. The level on OCSET is equal to V_{IN} less a fixed voltage drop (see over-current protection). The POR function initiates soft start operation after both input supply voltages exceed their POR thresholds. For operation with a single +12V power source, V_{IN} and V_{CC} are equivalent and the +12V power source must exceed the rising V_{CC} threshold before POR initiates operation.

Soft Start

The POR function initiates the soft start sequence. An internal 10µA current source charges an external capacitor (C_{SS}) on the SS pin to 4V. Soft start clamps the error amplifier output (COMP pin) and reference input (+ terminal of error amp) to the SS pin voltage. Figure 3 shows the soft start interval with C_{SS} = 0.1µF. Initially the clamp on the error amplifier (COMP pin) controls the converter's output voltage. At t_1 in Figure 3, the SS voltage reaches the valley of the oscillator's triangle wave. The oscillator's triangular waveform is compared to the ramping error amplifier voltage. This generates PHASE pulses of increasing width that charge the output capacitor(s). This interval of increasing pulse width continues to t_2. With sufficient output voltage, the clamp on the reference input controls the output voltage. This is the interval between t_2 and t_3 in Figure 3. At t_3 the SS voltage exceeds the DACOUT voltage and the output voltage is in regulation. This method provides a rapid and controlled output voltage rise. The PGOOD signal toggles 'high' when the output voltage (V_{SEN} pin) is within ±5% of DACOUT. The 2% hysteresis built into the power good comparators prevents PGOOD oscillation due to nominal output voltage ripple.

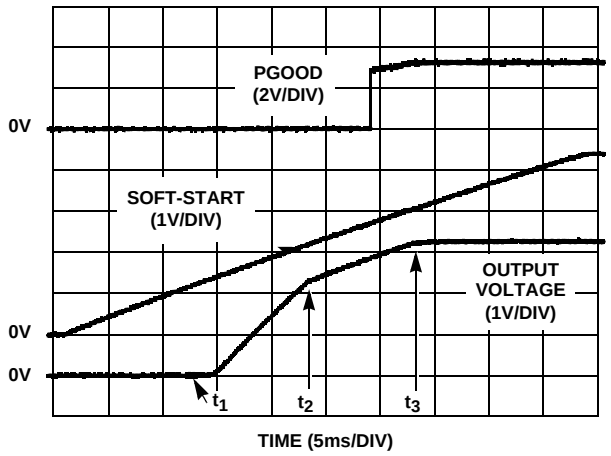


FIGURE 3. SOFT START INTERVAL

Over-Current Protection

The over-current function protects the converter from a shorted output by using the upper MOSFET's on-resistance, $r_{DS(ON)}$ to monitor the current. This method enhances the converter's efficiency and reduces cost by eliminating a current sensing resistor.

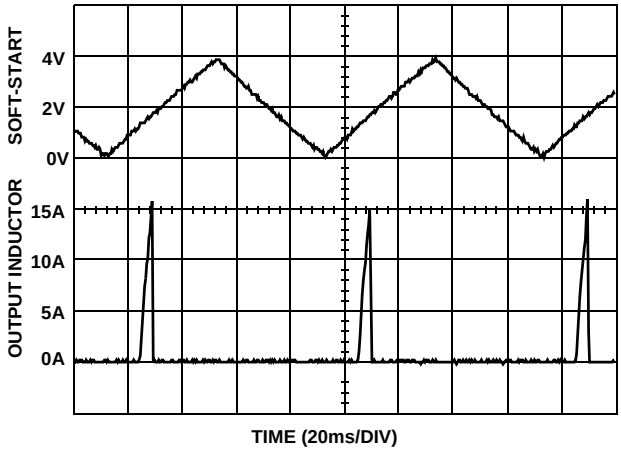


FIGURE 4. OVER-CURRENT OPERATION

The over-current function cycles the soft-start function in a hiccup mode to provide fault protection. A resistor (R_{OCSET}) programs the over-current trip level. An internal 200µA current sink develops a voltage across R_{OCSET} that is referenced to V_{IN}. When the voltage across the upper MOSFET (also referenced to V_{IN}) exceeds the voltage across R_{OCSET}, the over-current function initiates a soft-start sequence. The soft-start function discharges C_{SS} with a 10µA current sink and inhibits PWM operation. The soft-start function recharges C_{SS}, and PWM operation resumes with the error amplifier clamped to the SS voltage. Should an overload occur while recharging C_{SS}, the soft start function inhibits PWM operation while fully charging C_{SS} to 4V to complete its cycle. Figure 4 shows this operation with an overload condition. Note that the inductor current increases to over 15A during the C_{SS} charging interval and causes an over-current trip. The converter dissipates very little power with this method. The measured input power for the conditions of Figure 4 is 2.5W.

The over-current function will trip at a peak inductor current (I_{PEAK}) determined by:

$$I_{PEAK} = \frac{I_{OCSET} \times R_{OCSET}}{r_{DS(ON)}}$$

where I_{OCSET} is the internal OCSET current source (200µA typical). The OC trip point varies mainly due to the MOSFET's $r_{DS(ON)}$ variations. To avoid over-current tripping in the normal operating load range, find the R_{OCSET} resistor from the equation above with:

1. The maximum $r_{DS(ON)}$ at the highest junction temperature.
2. The minimum I_{OCSET} from the specification table.
3. Determine I_{PEAK} for $I_{PEAK} > I_{OUT(MAX)} + (\Delta I)/2$, where ΔI is the output inductor ripple current.

For an equation for the ripple current see the section under component guidelines titled 'Output Inductor Selection'.

A small ceramic capacitor should be placed in parallel with R_{OCSET} to smooth the voltage across R_{OCSET} in the presence of switching noise on the input voltage.

Output Voltage Program

The output voltage of a HIP6004B converter is programmed to discrete levels between $1.8V_{DC}$ and $3.5V_{DC}$. The voltage identification (VID) pins program an internal voltage reference (DACOUT) with a TTL-compatible 5-bit digital-to-analog converter (DAC). The level of DACOUT also sets the PGOOD and OVP thresholds. Table 1 specifies the DACOUT voltage for the 32 different combinations of connections on the VID pins. The output voltage should not be adjusted while the converter is delivering power. Remove input power before changing the output voltage. Adjusting the output voltage during operation could toggle the PGOOD signal and exercise the overvoltage protection.

'11111' VID pin combination resulting in a 0V output setting activates the Power-On Reset function and disables the gate drives circuitry. For this specific VID combination, though, PGOOD asserts a high level. This unusual behavior has been implemented in order to allow for operation in dual-microprocessor systems where AND-ing of the PGOOD signals from two individual power converters is implemented.

Application Guidelines

Layout Considerations

As in any high frequency switching converter, layout is very important. Switching current from one power device to another can generate voltage transients across the impedances of the interconnecting bond wires and circuit traces. These interconnecting impedances should be minimized by using wide, short printed circuit traces. The critical components should be located as close together as possible, using ground plane construction or single point grounding.

TABLE 1. OUTPUT VOLTAGE PROGRAM

PIN NAME					NOMINAL OUTPUT VOLTAGE DACOUT	PIN NAME					NOMINAL OUTPUT VOLTAGE DACOUT
VID4	VID3	VID2	VID1	VID0		VID4	VID3	VID2	VID1	VID0	
0	1	1	1	1	1.30	1	1	1	1	1	0
0	1	1	1	0	1.35	1	1	1	1	0	2.1
0	1	1	0	1	1.40	1	1	1	0	1	2.2
0	1	1	0	0	1.45	1	1	1	0	0	2.3
0	1	0	1	1	1.50	1	1	0	1	1	2.4
0	1	0	1	0	1.55	1	1	0	1	0	2.5
0	1	0	0	1	1.60	1	1	0	0	1	2.6
0	1	0	0	0	1.65	1	1	0	0	0	2.7
0	0	1	1	1	1.70	1	0	1	1	1	2.8
0	0	1	1	0	1.75	1	0	1	1	0	2.9
0	0	1	0	1	1.80	1	0	1	0	1	3.0
0	0	1	0	0	1.85	1	0	1	0	0	3.1
0	0	0	1	1	1.90	1	0	0	1	1	3.2
0	0	0	1	0	1.95	1	0	0	1	0	3.3
0	0	0	0	1	2.00	1	0	0	0	1	3.4
0	0	0	0	0	2.05	1	0	0	0	0	3.5

NOTE: 0 = connected to GND or V_{SS}, 1 = connected to V_{DD} through pull-up resistors.

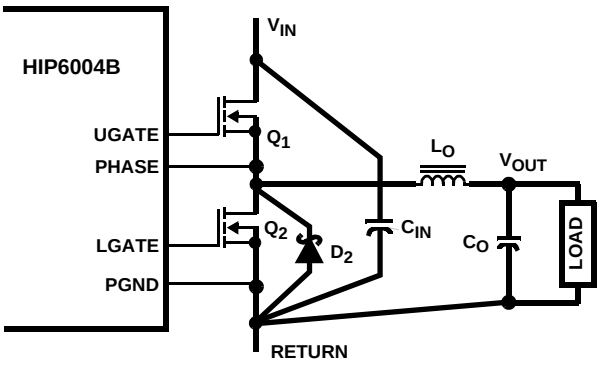


FIGURE 5. PRINTED CIRCUIT BOARD POWER AND GROUND PLANES OR ISLANDS

Figure 5 shows the critical power components of the converter. To minimize the voltage overshoot the interconnecting wires indicated by heavy lines should be part of ground or power plane in a printed circuit board. The components shown in Figure 5 should be located as close together as possible. Please note that the capacitors C_{IN} and C_O each represent numerous physical capacitors. Locate the HIP6004B within 3 inches of the MOSFETs, Q_1 and Q_2. The circuit traces for the MOSFETs' gate and source connections from the HIP6004B must be sized to handle up to 1A peak current.

Figure 6 shows the circuit traces that require additional layout consideration. Use single point and ground plane construction for the circuits shown. Minimize any leakage current paths on the SS PIN and locate the capacitor, C_{SS} close to the SS pin because the internal current source is only 10µA. Provide local V_{CC} decoupling between V_{CC} and GND pins. Locate the capacitor, C_{BOOT} as close as practical to the BOOT and PHASE pins.

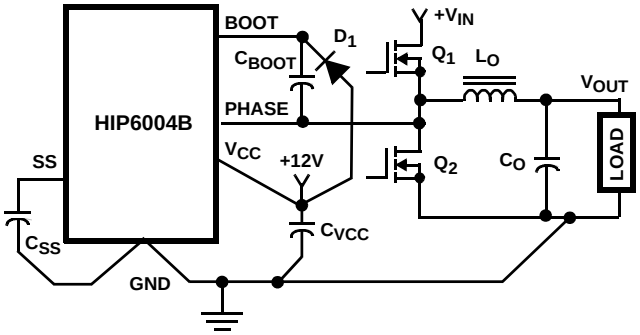


FIGURE 6. PRINTED CIRCUIT BOARD SMALL SIGNAL LAYOUT GUIDELINES

Feedback Compensation

Figure 7 highlights the voltage-mode control loop for a synchronous-rectified buck converter. The output voltage (V_{OUT}) is regulated to the Reference voltage level. The error amplifier (Error Amp) output ($V_{E/A}$) is compared with the oscillator (OSC) triangular wave to provide a pulse-width modulated (PWM) wave with an amplitude of V_{IN} at the PHASE node.

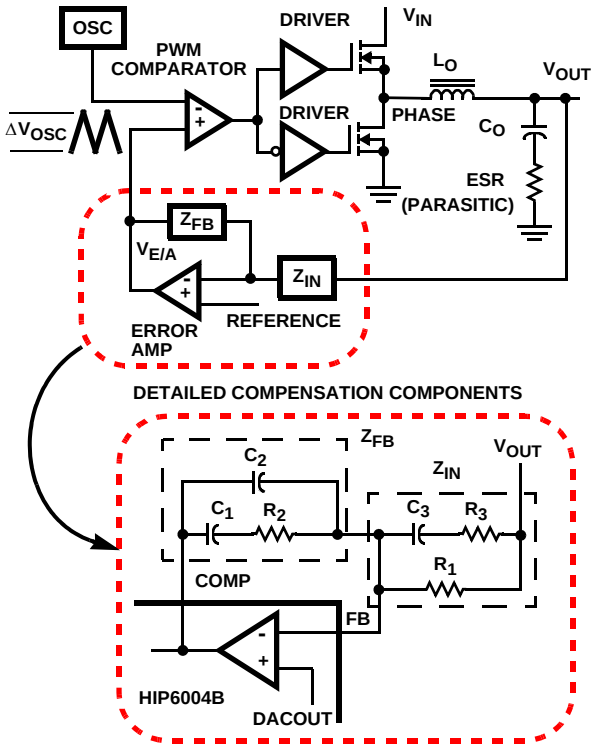


FIGURE 7. VOLTAGE-MODE BUCK CONVERTER COMPENSATION DESIGN

The PWM wave is smoothed by the output filter (L_O and C_O). The modulator transfer function is the small-signal transfer function of $V_{OUT}/V_{E/A}$. This function is dominated by a DC Gain and the output filter (L_O and C_O), with a double pole break frequency at F_{LC} and a zero at F_{ESR}. The DC Gain of the modulator is simply the input voltage (V_{IN}) divided by the peak-to-peak oscillator voltage ΔV_{OSC}.

Modulator Break Frequency Equations

$$F_{LC} = \frac{1}{2\pi \times \sqrt{L_O \times C_O}} \qquad F_{ESR} = \frac{1}{2\pi \times ESR \times C_O}$$

The compensation network consists of the error amplifier (internal to the HIP6004B) and the impedance networks Z_{IN} and Z_{FB}. The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency (f_{0dB}) and adequate phase margin. Phase margin is the difference between the closed loop phase at f_{0dB} and 180 degrees. The equations below relate the compensation network's poles, zeros and gain to the components (R_1, R_2, R_3, C_1, C_2, and C_3) in Figure 7. Use these guidelines for locating the poles and zeros of the compensation network:

1. Pick Gain (R_2/R_1) for desired converter bandwidth.
2. Place 1ST Zero Below Filter's Double Pole (~75% F_{LC}).
3. Place 2ND Zero at Filter's Double Pole.
4. Place 1ST Pole at the ESR Zero.
5. Place 2ND Pole at Half the Switching Frequency.
6. Check Gain against Error Amplifier's Open-Loop Gain.
7. Estimate Phase Margin - Repeat if Necessary.

Compensation Break Frequency Equations

$$F_{Z1} = \frac{1}{2\pi \times R_2 \times C_1} \qquad F_{P1} = \frac{1}{2\pi \times R_2 \times \left(\frac{C_1 \times C_2}{C_1 + C_2}\right)}$$

$$F_{Z2} = \frac{1}{2\pi \times (R_1 + R_3) \times C_3} \qquad F_{P2} = \frac{1}{2\pi \times R_3 \times C_3}$$

Figure 8 shows an asymptotic plot of the DC-DC converter's gain vs frequency. The actual Modulator Gain has a high gain peak due to the high Q factor of the output filter and is not shown in Figure 8. Using the above guidelines should give a Compensation Gain similar to the curve plotted. The open loop error amplifier gain bounds the compensation gain. Check the compensation gain at F_{P2} with the capabilities of the error amplifier. The Closed Loop Gain is constructed on the log-log graph of Figure 8 by adding the Modulator Gain (in dB) to the Compensation Gain (in dB). This is equivalent to multiplying the modulator transfer function to the compensation transfer function and plotting the gain.

The compensation gain uses external impedance networks Z_{FB} and Z_{IN} to provide a stable, high bandwidth (BW) overall loop. A stable control loop has a gain crossing with -20dB/decade slope and a phase margin greater than 45 degrees. Include worst case component variations when determining phase margin.

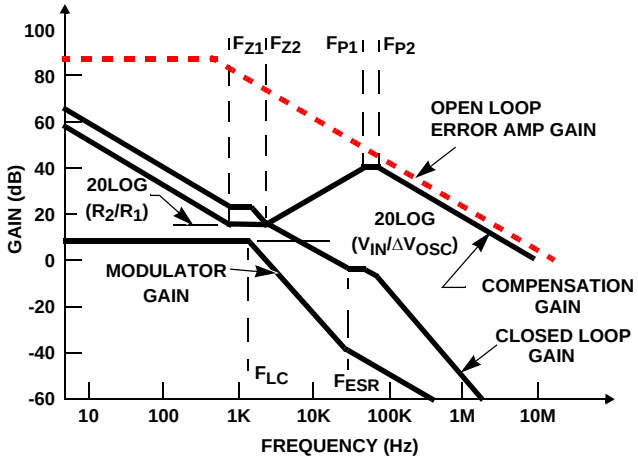


FIGURE 8. ASYMPTOTIC BODE PLOT OF CONVERTER GAIN

Component Selection Guidelines

Output Capacitor Selection

An output capacitor is required to filter the output and supply the load transient current. The filtering requirements are a function of the switching frequency and the ripple current. The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitors and careful layout.

Modern microprocessors produce transient load rates above 1A/ns. High frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (Effective Series Resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements. For example, Intel recommends that the high frequency decoupling for the Pentium Pro be composed of at least forty (40) 1µF ceramic capacitors in the 1206 surface-mount package.

Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR will determine the output ripple voltage and the initial voltage drop after a high slew-rate transient. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes. However, the Equivalent Series Inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading. Unfortunately, ESL is not a specified parameter. Work with your capacitor supplier and measure the capacitor's impedance with frequency to select a suitable component. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

Output Inductor Selection

The output inductor is selected to meet the output voltage ripple requirements and minimize the converter's response time to the load transient. The inductor value determines the converter's ripple current and the ripple voltage is a function of the ripple current. The ripple voltage and current are approximated by the following equations:

$$DI = \frac{V_{IN} - V_{OUT}}{Fs \times L} \times \frac{V_{OUT}}{V_{IN}} \qquad DV_{OUT} = DI \times ESR$$

Increasing the value of inductance reduces the ripple current and voltage. However, the large inductance values reduce the converter's response time to a load transient.

One of the parameters limiting the converter's response to a load transient is the time required to change the inductor current. Given a sufficiently fast control loop design, the HIP6004B will provide either 0% or 100% duty cycle in response to a load transient. The response time is the time required to slew the inductor current from an initial current value to the transient current level. During this interval the difference between the inductor current and the transient current level must be supplied by the output capacitor. Minimizing the response time can minimize the output capacitance required.

The response time to a transient is different for the application of load and the removal of load. The following equations give the approximate response time interval for application and removal of a transient load:

$$t_{RISE} = \frac{L \times I_{TRAN}}{V_{IN} - V_{OUT}} \qquad t_{FALL} = \frac{L \times I_{TRAN}}{V_{OUT}}$$

where: I_{TRAN} is the transient load current step, t_{RISE} is the response time to the application of load, and t_{FALL} is the response time to the removal of load. With a +5V input source, the worst case response time can be either at the application or removal of load and dependent upon the DACOUT setting. Be sure to check both of these equations at the minimum and maximum output levels for the worst case response time. With a +12V input, and output voltage level equal to DACOUT, t_{FALL} is the longest response time.

Input Capacitor Selection

Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the current needed each time Q_1 turns on. Place the small ceramic capacitors physically close to the MOSFETs and between the drain of Q_1 and the source of Q_2.

The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. The RMS current rating requirement for the input capacitor of a buck regulator is approximately 1/2 the DC load current.

For a through hole design, several electrolytic capacitors (Panasonic HFQ series or Nichicon PL series or Sanyo MV-GX or equivalent) may be needed. For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge-current at power-up. The TPS series available from AVX, and the 593D series from Sprague are both surge current tested.

MOSFET Selection/Considerations

The HIP6004B requires 2 N-Channel power MOSFETs. These should be selected based upon $r_{DS(ON)}$, gate supply requirements, and thermal management requirements.

In high-current applications, the MOSFET power dissipation, package selection and heatsink are the dominant design factors. The power dissipation includes two loss components; conduction loss and switching loss. The conduction losses are the largest component of power dissipation for both the upper and the lower MOSFETs. These losses are distributed between the two MOSFETs according to duty factor (see the equations

below). Only the upper MOSFET has switching losses, since the Schottky rectifier clamps the switching node before the synchronous rectifier turns on. These equations assume linear voltage-current transitions and do not adequately model power loss due the reverse-recovery of the lower MOSFET's body diode. The gate-charge losses are dissipated by the HIP6004B and don't heat the MOSFETs. However, large gate-charge increases the switching interval, t_{SW} which increases the upper MOSFET switching losses. Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications. A separate heatsink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.

$$P_{UPPER} = Io^2 \times r_{DS(ON)} \times D + \frac{1}{2} Io \times V_{IN} \times t_{SW} \times F_S$$

$$P_{LOWER} = Io^2 \times r_{DS(ON)} \times (1 - D)$$

Where: D is the duty cycle = V_{OUT} / V_{IN},
t_{SW} is the switch ON time, and
F_S is the switching frequency.

Standard-gate MOSFETs are normally recommended for use with the HIP6004B. However, logic-level gate MOSFETs can be used under special circumstances. The input voltage, upper gate drive level, and the MOSFET's absolute gate-to-source voltage rating determine whether logic-level MOSFETs are appropriate.

Figure 9 shows the upper gate drive (BOOT pin) supplied by a bootstrap circuit from V_{CC}. The boot capacitor, C_{BOOT} develops a floating supply voltage referenced to the PHASE pin. This supply is refreshed each cycle to a voltage of V_{CC} less the boot diode drop (V_D) when the lower MOSFET, Q_2 turns on. Logic-level MOSFETs can only be used if the MOSFET's absolute gate-to-source voltage rating exceeds the maximum voltage applied to V_{CC}.

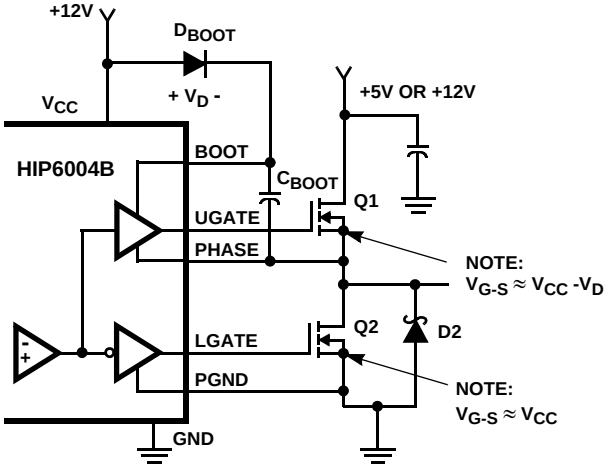


FIGURE 9. UPPER GATE DRIVE - BOOTSTRAP OPTION

Figure 10 shows the upper gate drive supplied by a direct connection to V_{CC}. This option should only be used in converter systems where the main input voltage is $+5V_{DC}$ or less. The peak upper gate-to-source voltage is approximately V_{CC} less the input supply. For +5V main power and $+12V_{DC}$ for the bias, the gate-to-source voltage of Q_1 is 7V. A logic-level MOSFET is a good choice for Q_1 and a logic-level MOSFET can be used for Q_2 if its absolute gate-to-source voltage rating exceeds the maximum voltage applied to V_{CC}.

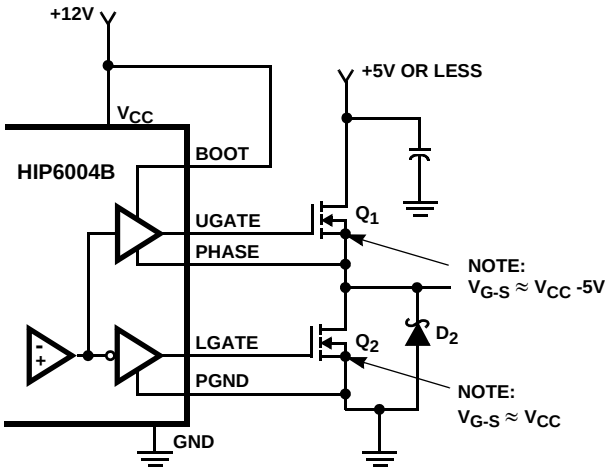


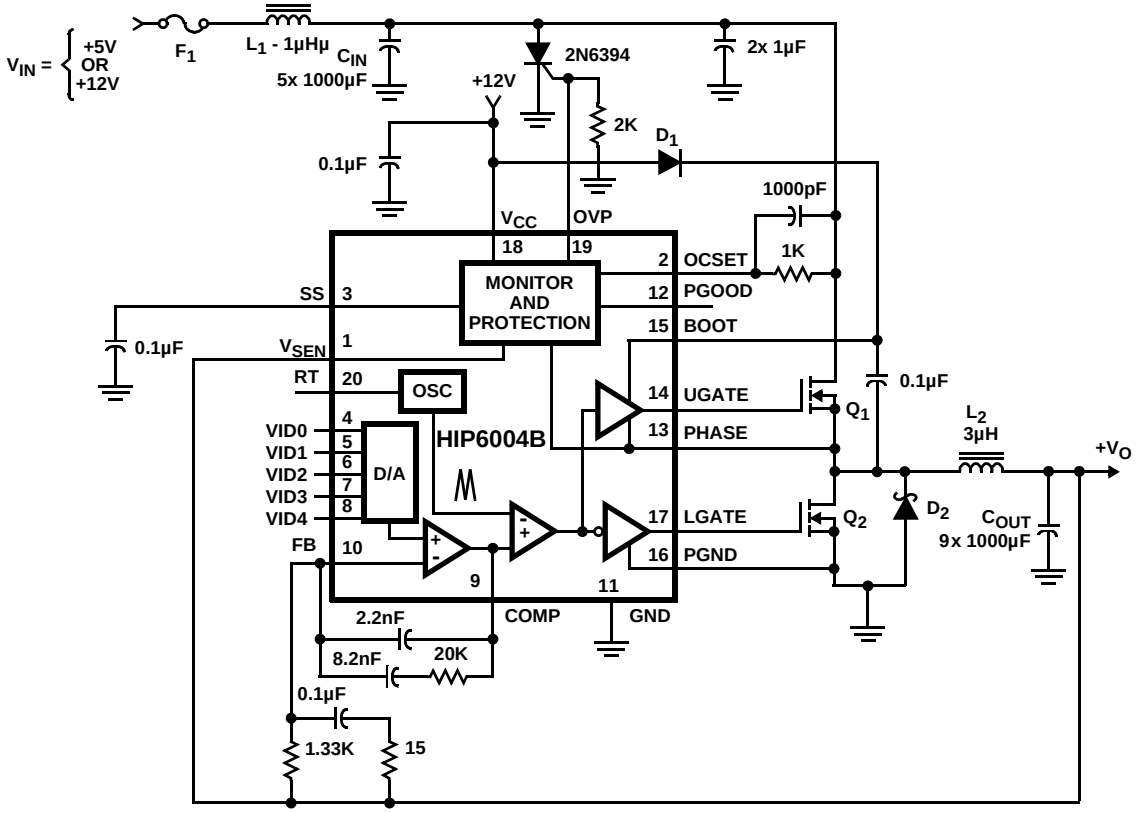
FIGURE 10. UPPER GATE DRIVE - DIRECT V_{CC} DRIVE OPTION

Schottky Selection

Rectifier D_2 is a clamp that catches the negative inductor swing during the dead time between turning off the lower MOSFET and turning on the upper MOSFET. The diode must be a Schottky type to prevent the lossy parasitic MOSFET body diode from conducting. It is acceptable to omit the diode and let the body diode of the lower MOSFET clamp the negative inductor swing, but efficiency will drop one or two percent as a result. The diode's rated reverse breakdown voltage must be greater than the maximum input voltage.

HIP6004B DC-DC Converter Application Circuit

Figure 11 shows an application circuit of a DC-DC Converter for an Intel Pentium Pro microprocessor. Detailed information on the circuit, including a complete Bill-of-Materials and circuit board description, can be found in Application Note AN9672. Although the Application Note details the HIP6004, the same evaluation platform can be used to evaluate the HIP6004B.



Component Selection Notes:

C_{OUT} - Each 1000µF 6.3W VDC, Sanyo MV-GX or Equivalent.

C_{IN} - Each 330µF 25W VDC, Sanyo MV-GX or Equivalent.

L_2 - Core: Micrometals T50-52B; Each Winding: 10 Turns of 16AWG.

L_1 - Core: Micrometals T50-52; Winding: 5 Turns of 18AWG.

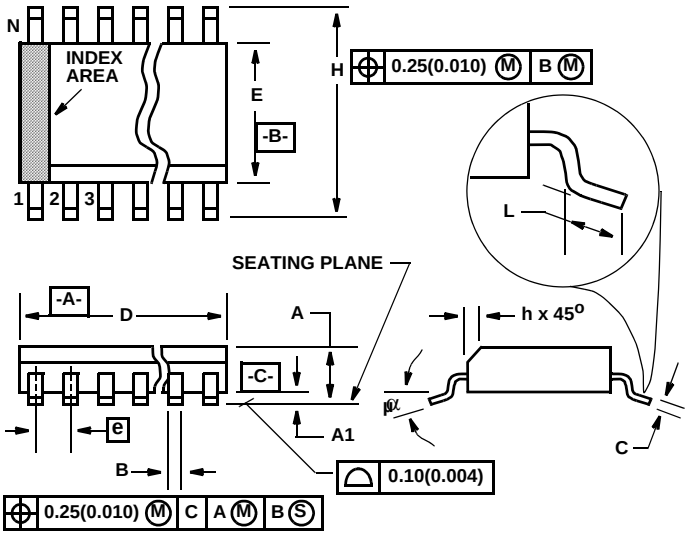
D_1 - 1N4148 or Equivalent.

D_2 - 3A, 40V Schottky, Motorola MBR340 or Equivalent.

Q_1, Q_2 - Intersil MOSFET; RFP70N03.

FIGURE 11. PENTIUM PRO DC-DC CONVERTER

Small Outline Plastic Packages (SOIC)



M20.3 (JEDEC MS-013-AC ISSUE C)
20 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.014	0.019	0.35	0.49	9
C	0.0091	0.0125	0.23	0.32	-
D	0.4961	0.5118	12.60	13.00	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	20		20		7
α	0^o	8^o	0^o	8^o	-

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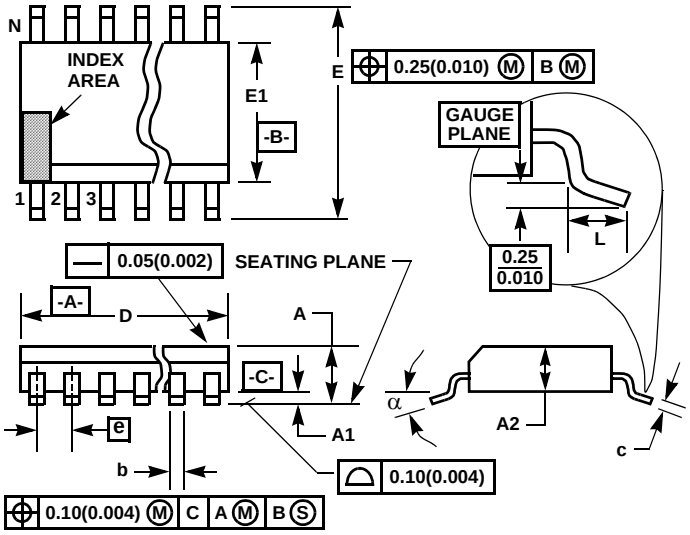
NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Thin Shrink Small Outline Plastic Packages (TSSOP)



NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AC, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

M20.173

20 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.047	-	1.20	-
A1	0.002	0.006	0.05	0.15	-
A2	0.031	0.051	0.80	1.05	-
b	0.0075	0.0118	0.19	0.30	9
c	0.0035	0.0079	0.09	0.20	-
D	0.252	0.260	6.40	6.60	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.0177	0.0295	0.45	0.75	6
N	20		20		7
α	0^o	8^o	0^o	8^o	-

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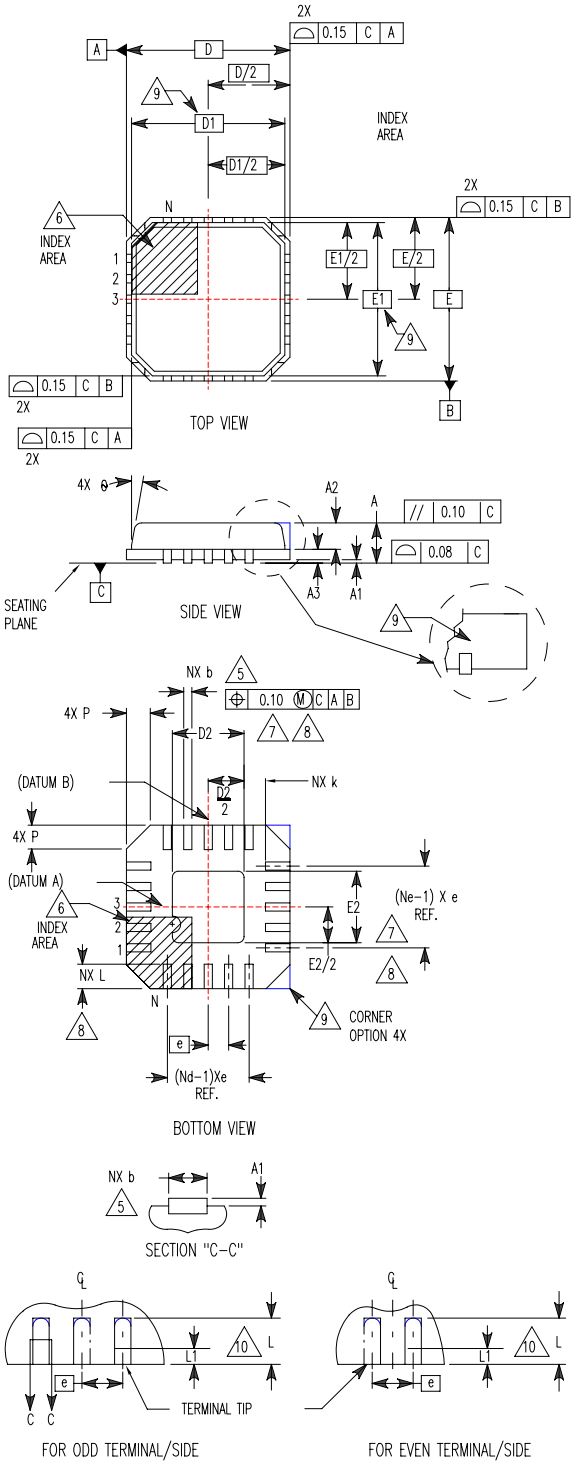
Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L20.5x5

20 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VHHC ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.23	0.28	0.38	5, 8
D		5.00 BSC		-
D1		4.75 BSC		9
D2	2.95	3.10	3.25	7, 8
E		5.00 BSC		-
E1		4.75 BSC		9
E2	2.95	3.10	3.25	7, 8
e		0.65 BSC		-
k	0.25	-	-	-
L	0.35	0.60	0.75	8
L1	-	-	0.15	10
N		20		2
Nd		5		3
Ne		5		3
P	-	-	0.60	9
θ	-	-	12	9

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NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.

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