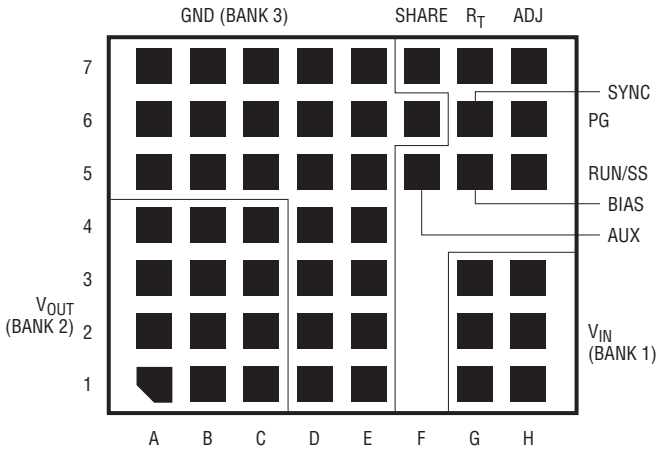
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, RUN/SS Voltage.....40V
ADJ, R_T, SHARE, Voltage.....5V
V_{OUT}, AUX.....10V
SYNC, PG.....30V
BIAS.....16V
V_{IN} + BIAS.....56V
Internal Operating Temperature.....–40°C to 125°C
Solder Temperature.....250°C
Storage Temperature.....–55°C to 125°C

PIN CONFIGURATION

(See Table 3, Pin Assignment)



LGA PACKAGE
50-LEAD (11.25mm × 9mm × 2.82mm)

T_{JMAX} = 125°C, θ_{JA} = 23.4°C/W, $\theta_{JC(BOTTOM)}$ = 9.20°C/W,
$\theta_{JC(TOP)}$ = 25.10°C/W, θ_{JBOARD} = 16°C/W
θ VALUES DETERMINED PER JESD51-9
WEIGHT = 0.93g

ORDER INFORMATION

LEAD FREE FINISH	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE (Note 2)
LTM8022EV#PBF	LTM8022V	50-Pin (11.25mm × 9mm × 2.82mm) LGA	–40°C to 85°C
LTM8022IV#PBF	LTM8022V	50-Pin (11.25mm × 9mm × 2.82mm) LGA	–40°C to 85°C
LTM8022MPV#PBF	LTM8022MPV	50-Pin (11.25mm × 9mm × 2.82mm) LGA	–55°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
This product is only offered in trays. For more information go to: http://linear.com/packaging/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 10V, $V_{RUN/SS}$ = 10V, V_{BIAS} = 3V, R_T = 60.4kΩ, C_{IN} = 2.2µF, C_{OUT} = 4.7µF, unless otherwise specified. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input DC Voltage		●	3.6		36	V
V_{OUT}	Output DC Voltage	0V < I_{OUT} < 1A, R_{ADJ} Open 0V < I_{OUT} < 1A, R_{ADJ} = 43.2k			0.8 10		V V
$R_{ADJ(MIN)}$	Minimum Allowable R_{ADJ}	(Note 3)		42.2			kΩ
$I_{OUT(MAX)}$	Continuous Output DC Current	4V < V_{IN} < 36V, C_{OUT} = 51µF (Note 4)		0		1	A
IQ_{VIN}	V_{IN} Quiescent Current	$V_{RUN/SS}$ = 0.2V, R_T = 174k V_{BIAS} = 3V, Not Switching, R_T = 174k (E, I) V_{BIAS} = 3V, Not Switching, R_T = 174k (MP) V_{BIAS} = 0V, Not Switching, R_T = 174k	 ● ● 		0.1 25 25 85	0.5 60 350 120	µA µA µA µA
IQ_{BIAS}	BIAS Quiescent Current	$V_{RUN/SS}$ = 0.2V, R_T = 174k V_{BIAS} = 3V, Not Switching, R_T = 174k (E, I) V_{BIAS} = 3V, Not Switching, R_T = 174k (MP) V_{BIAS} = 0V, Not Switching, R_T = 174k	 ● ● 		0.03 50 50 1	0.5 120 200 5	µA µA µA µA
$\Delta V_{OUT}/V_{OUT}$	Line Regulation	3.6V < V_{IN} < 36V, I_{OUT} = 1A, V_{OUT} = 3.3V			0.1		%
$\Delta V_{OUT}/V_{OUT}$	Load Regulation	V_{IN} = 24V, 0V < I_{OUT} < 1A, V_{OUT} = 3.3V, C_{OUT} = 51µF			0.4		%
$V_{OUT(AC\_RMS)}$	Output Ripple (RMS)	V_{IN} = 24V, I_{OUT} = 1A, V_{OUT} = 3.3V, C_{OUT} = 51µF			10		mV
f_{SW}	Switching Frequency	R_T = 113kΩ, C_{OUT} = 51µF			325		kHz
$I_{SC(OUT)}$	Output Short-Circuit Current	V_{IN} = 36V, V_{OUT} = 0V (Note 5)			3		A
V_{ADJ}	Voltage at ADJ Pin	C_{OUT} = 51µF	●	765	790	805	mV
$V_{BIAS(MIN)}$	Minimum BIAS Voltage for Proper Operation				1.9	2.4	V
I_{ADJ}	Current Out of ADJ Pin	ADJ = 1V, C_{OUT} = 51µF			2		µA
$I_{RUN/SS}$	RUN/SS Pin Current	$V_{RUN/SS}$ = 2.5V			5	10	µA
$V_{IH(RUN/SS)}$	RUN/SS Input High Voltage	C_{OUT} = 51µF		2.5			V
$V_{IL(RUN/SS)}$	RUN/SS Input Low Voltage	C_{OUT} = 51µF				0.2	V
$V_{PG(TH)}$	PG Threshold	V_{FB} Rising			730		mV
I_{PGO}	PG Leakage	V_{PG} = 30V			0.1	1	µA
$I_{PG(SINK)}$	PG Sink Current	V_{PG} = 0.4V		200	800		µA
$V_{SYNC(IL)}$	SYNC Low Threshold	f_{SYNC} = 550kHz, C_{OUT} = 51µF		0.5			V
$V_{SYNC(IH)}$	SYNC High Threshold	f_{SYNC} = 550kHz, C_{OUT} = 51µF				0.7	V
$I_{SYNC(BIAS)}$	SYNC Pin Bias Current	V_{SYNC} = 0V			0.1		µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTM8022E is guaranteed to meet performance specifications from 0°C to 85°C ambient. Specifications over the full –40°C to 85°C ambient operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM8022I is guaranteed to meet specifications over the full –40°C to 85°C ambient operating temperature range. The LTM8022MP is guaranteed to meet specifications over the full –55°C to 125°C temperature range. Note that the maximum internal temperature is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

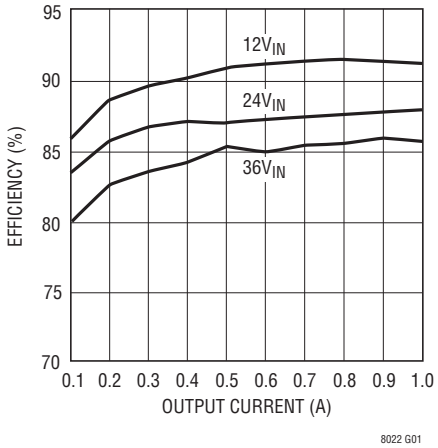
Note 3: Guaranteed by design.

Note 4: C_{OUT} = 51µF is composed of a 4.7µF ceramic capacitor and a 47µF electrolytic.

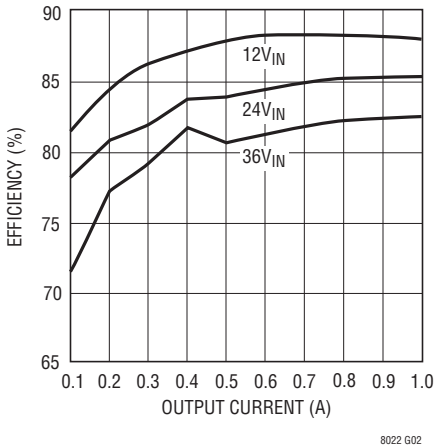
Note 5: Short circuit current at V_{IN} = 36V is guaranteed by characterization and correlation. 100% tested at V_{IN} = 10V.

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C, unless otherwise noted)

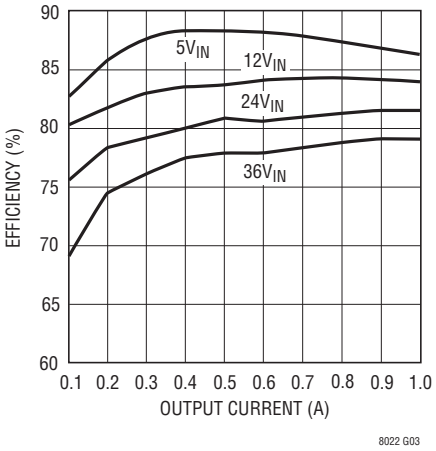
Efficiency vs Load ($8V_{OUT}$)



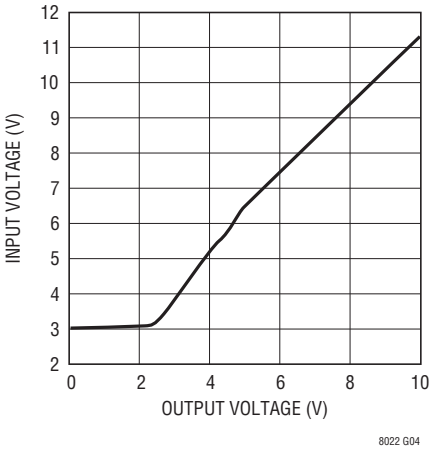
Efficiency vs Load ($5V_{OUT}$)



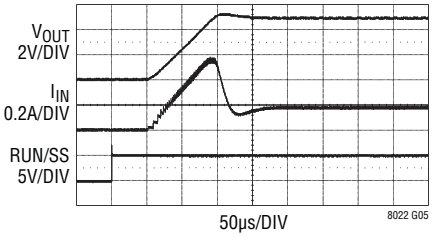
Efficiency vs Load ($3.3V_{OUT}$)



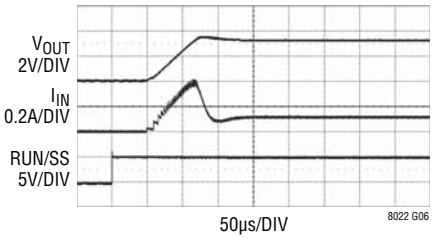
Minimum Required Input Voltage vs Output Voltage, I_{OUT} = 1A



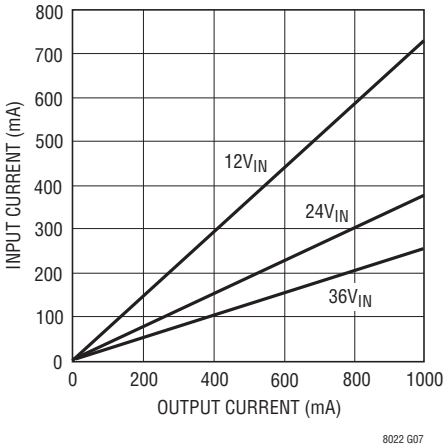
Output Start-up Waveform V_{IN} = 36V, $5V_{OUT}$, I_{OUT} = 1A



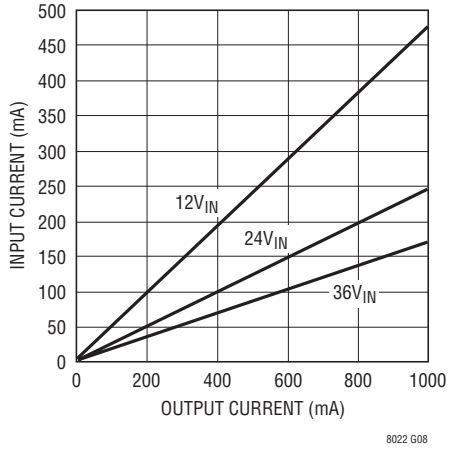
Output Start-up Waveform V_{IN} = 36V, $3.3V_{OUT}$, I_{OUT} = 1A



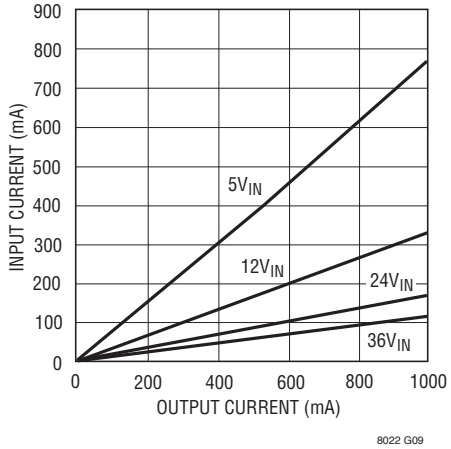
Input Current vs Output Current ($8V_{OUT}$)



Input Current vs Output Current ($5V_{OUT}$)

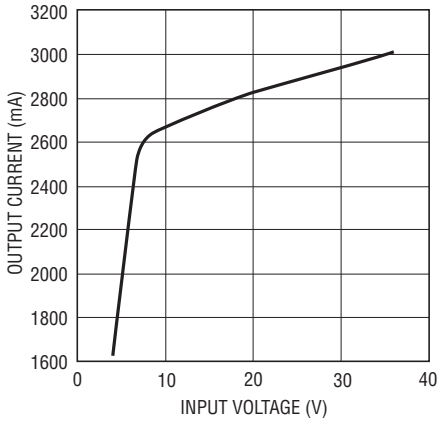


Input Current vs Output Current ($3.3V_{OUT}$)

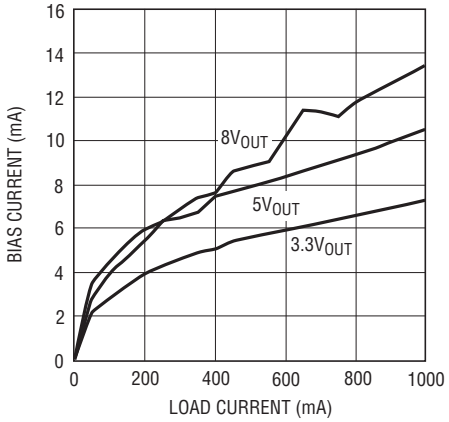


TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C, unless otherwise noted)

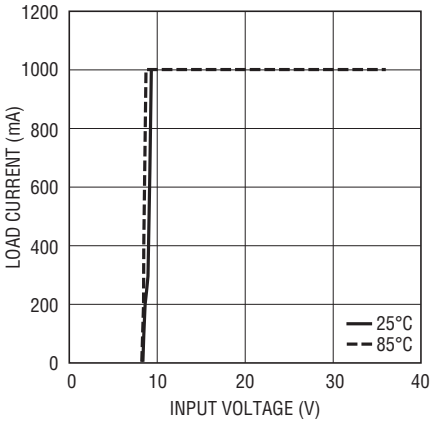
Output Current vs Input Voltage (Output Short)



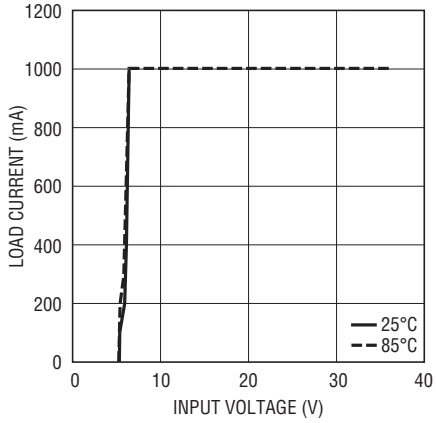
BIAS Quiescent Current vs Load Current



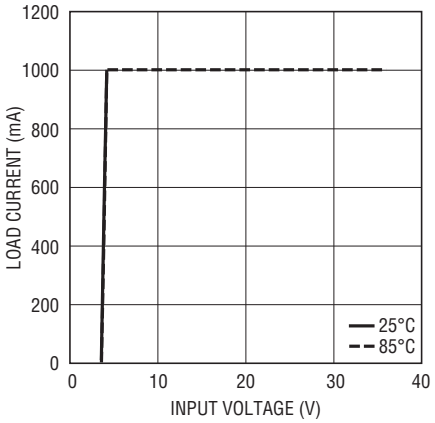
Minimum Required Input Voltage vs Output Load ($8V_{OUT}$)



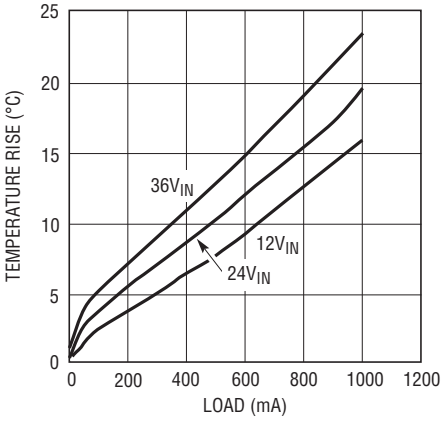
Minimum Required Input Voltage vs Output Load ($5V_{OUT}$)



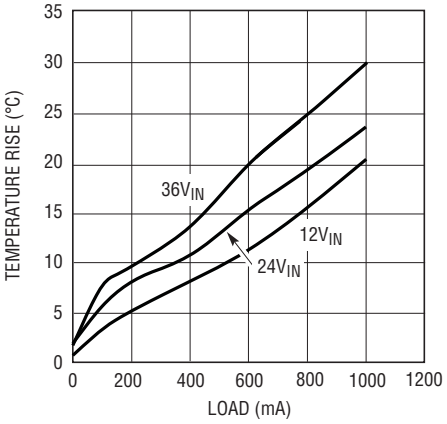
Minimum Required Input Voltage vs Output Load ($3.3V_{OUT}$)



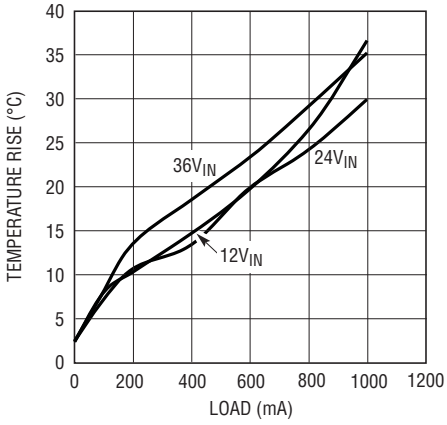
Temperature Rise vs Load ($3.3V_{OUT}$)



Temperature Rise vs Load ($5V_{OUT}$)



Temperature Rise vs Load ($8V_{OUT}$)



PIN FUNCTIONS

V_{IN} (Bank 1): The V_{IN} pin supplies current to the LTM8022's internal regulator and to the internal power switch. This pin must be locally bypassed with an external, low ESR capacitor of at least 2.2µF.

V_{OUT} (Bank 2): Power Output Pins. Apply the output filter capacitor and the output load between these pins and GND pins.

AUX (Pin F5): Low current voltage source for BIAS. In many designs, the BIAS pin is simply connected to V_{OUT}. The AUX pin is internally connected to V_{OUT} and is placed adjacent to the BIAS pin to ease printed circuit board routing. Although this pin is internally connected to V_{OUT}, do NOT connect this pin to the load. If this pin is not tied to BIAS, leave it floating. The Application Information section gives specific information about the BIAS and AUX connections

BIAS (Pin G5): The BIAS pin connects to the internal power bus. Connect to a power source greater than 2.4V. If the output is greater than 2.4V, connect this pin there. If the output voltage is less, connect this to a voltage source between 2.4V and 16V. Also, make sure that BIAS + V_{IN} is less than 56V.

RUN/SS (Pin H5): Tie RUN/SS pin to ground to shut down the LTM8022. Tie to 2.5V or more for normal operation. If the shutdown feature is not used, tie this pin to the V_{IN} pin. RUN/SS also provides a soft-start function; see the Applications Information section.

GND (Bank 3): Tie these GND pins to a local ground plane below the LTM8022 and the circuit components. Return the feedback divider (R_{ADJ}) to this pin.

R_T (Pin G7): The R_T pin is used to program the switching frequency of the LTM8022 by connecting a resistor from this pin to ground. The Applications Information section of the data sheet includes a table to determine the resistance value based on the desired switching frequency. Minimize capacitance at this pin.

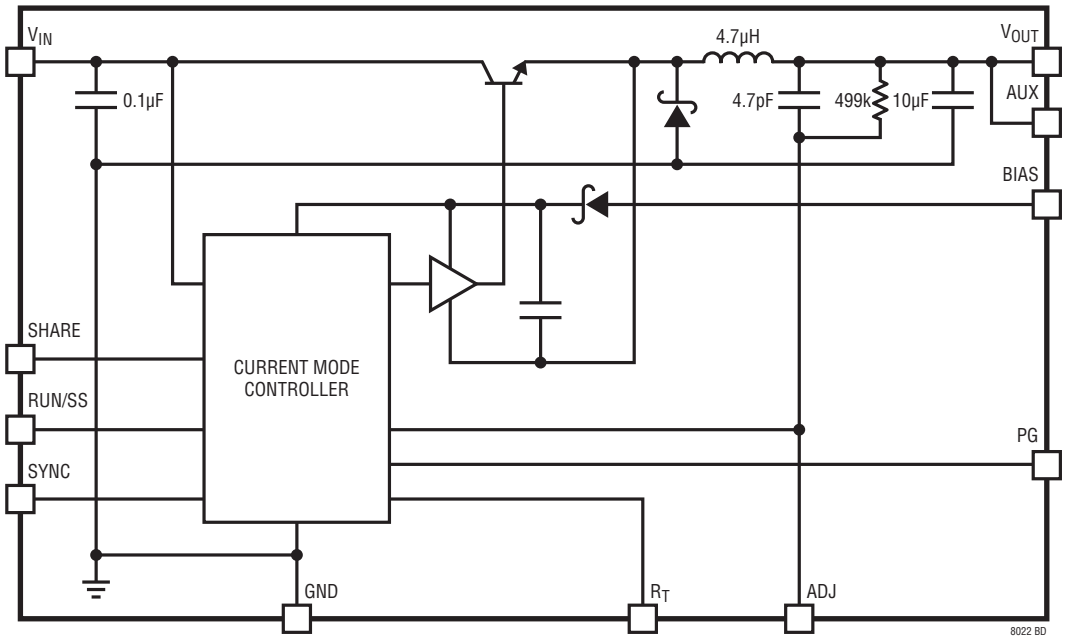
SHARE (Pin F7): Tie this to the SHARE pin of another LTM8022 when paralleling the outputs. Otherwise, leave this pin floating.

SYNC (Pin G6): External Clock Synchronization Input. Ground this pin for low ripple Burst Mode® operation at low output loads, or connect to a stable voltage source above 0.7V to disable Burst Mode operation. **Do not leave this pin floating.** Tie to a clock source for synchronization. Clock edges should have rise and fall times faster than 1µs. See Synchronization in the Applications Information section.

PG (Pin H6): Open Collector Output of an Internal Comparator. PG remains low until the ADJ pin is within 10% of the final regulation voltage. PG output is valid when V_{IN} is above 3.6V and RUN/SS is high. If this function is not used, leave this pin floating.

ADJ (Pin H7): The LTM8022 regulates its ADJ pin to 0.79V. Connect the adjust resistor from this pin to ground. The value of R_{ADJ} is given by the equation, $R_{ADJ} = 394.21/(V_{OUT} - 0.79)$, where R_{ADJ} is in kΩ.

BLOCK DIAGRAM



OPERATION

The LTM8022 is a standalone non-isolated step-down switching DC/DC power supply. It can deliver up to 1A of DC output current with only bulk external input and output capacitors. This module provides a precisely regulated output voltage programmable via one external resistor from $0.8V_{DC}$ to $10V_{DC}$. The input voltage range is 3.6V to 36V. Given that the LTM8022 is a step-down converter, make sure that the input voltage is high enough to support the desired output voltage and load current. A simplified Block Diagram is shown above.

The LTM8022 contains a current mode controller, power switching element, power inductor, power Schottky diode and a modest amount of input and output capacitance.

The LTM8022 is a fixed frequency PWM regulator. The switching frequency is set by simply connecting the appropriate value resistor from the R_T pin to GND.

An internal regulator provides power to the control circuitry. The bias regulator normally draws power from the V_{IN} pin, but if the BIAS pin is connected to an external voltage higher than 2.4V, bias power will be drawn from the external source (typically the regulated output voltage). This improves efficiency. The RUN/SS pin is used to place the LTM8022 in shutdown, disconnecting the output and reducing the input current to less than 1µA.

To further optimize efficiency, the LTM8022 automatically switches to Burst Mode operation in light load situations. Between bursts, all circuitry associated with controlling the output switch is shut down reducing the input supply current to 50µA in a typical application. The oscillator reduces the LTM8022's operating frequency when the voltage at the ADJ pin is low. This frequency foldback helps to control the output current during start-up and overload.

The LTM8022 contains a power good comparator which trips when the ADJ pin is at 92% of its regulated value. The PG output is an open-collector transistor that is off when the output is in regulation, allowing an external resistor to pull the PG pin high. Power good is valid when the LTM8022 is enabled and V_{IN} is above 3.6V.

APPLICATIONS INFORMATION

Table 1. Recommended Component Values and Configuration

V_{IN}*	V_{OUT}	C_{IN}	C_{OUT}	R_{ADJ}	B_{IAS}	$f_{OPTIMAL}$(kHz)	$R_{T(OPTIMAL)}$	f_{MAX} (kHz)	$R_{T(MIN)}$
3.6V to 36V	0.82V	2.2µF	247µF 1206	13M	≥2.4V, <16V	250	150k	250	150k
3.6V to 36V	1V	2.2µF	200µF 1206	1.87M	≥2.4V, <16V	300	124k	300	124k
3.6V to 36V	1.2V	2.2µF	100µF 1206	953k	≥2.4V, <16V	325	113k	325	113k
3.6V to 36V	1.5V	2.2µF	100µF 1206	549k	≥2.4V, <16V	375	93.1k	375	93.1k
3.6V to 36V	1.8V	2.2µF	68µF 1206	383k	≥2.4V, <16V	450	79k	450	79k
3.8V to 36V	2V	2.2µF	47µF 1206	324k	≥2.4V, <16V	475	73.2k	475	73.2k
3.8V to 36V	2.2V	2.2µF	47µF 0805	274k	≥2.4V, <16V	525	64.9k	525	64.9k
3.8V to 36V	2.5V	2.2µF	47µF 0805	226k	≥2.4V, <16V	575	59.0k	575	59.0k
4.75V to 36V	3.3V	2.2µF	22µF 0805	154k	AUX	750	42.2k	750	42.2k
6.8V to 36V	5V	2.2µF	4.7µF 1206	93.1k	AUX	1000	29.4k	1050	28.0k
11.5V to 36V	8V	2.2µF	4.7µF 0805	53.6k	AUX	1200	23.7k	1600	15.8k
3.6V to 15V	0.82V	2.2µF	200µF 1206	13M	V_{IN}	500	69.8k	615	54.9k
3.6V to 15V	1V	2.2µF	147µF 1206	1.87M	V_{IN}	615	54.9k	650	49.9k
3.6V to 15V	1.2V	2.2µF	100µF 1206	953k	V_{IN}	650	49.9k	750	42.2k
3.6V to 15V	1.5V	2.2µF	100µF 1206	549k	V_{IN}	700	44.2k	890	34.8k
3.6V to 15V	1.8V	2.2µF	68µF 1206	383k	V_{IN}	800	39.2k	1050	28.0k
3.6V to 15V	2V	2.2µF	47µF 1206	324k	V_{IN}	800	39.2k	1100	26.7k
3.6V to 15V	2.2V	2.2µF	47µF 0805	274k	V_{IN}	850	36.5k	1200	23.7k
3.6V to 15V	2.5V	2.2µF	47µF 0805	226k	V_{IN}	950	31.6k	1350	20.5k
4.75V to 15V	3.3V	2.2µF	22µF 0805	154k	AUX	950	31.6k	1725	14.3k
6.8V to 15V	5V	2.2µF	4.7µF 1206	93.1k	AUX	1150	25.5k	2400	7.87k
11.5V to 15V	8V	2.2µF	4.7µF 0805	53.6k	AUX	1200	23.7k	1900	12.1k
9V to 24V	0.82V	2.2µF	247µF 1206	13M	≥2.4V, <16V	375	93.1k	375	93.1k
9V to 24V	1V	2.2µF	200µF 1206	1.87M	≥2.4V, <16V	400	88.7k	400	88.7k
9V to 24V	1.2V	2.2µF	100µF 1206	953k	≥2.4V, <16V	450	79.0k	500	69.8k
9V to 24V	1.5V	2.2µF	100µF 1206	549k	≥2.4V, <16V	575	59.0k	575	59.0k
9V to 24V	1.8V	2.2µF	68µF 1206	383k	≥2.4V, <16V	650	49.9k	650	49.9k
9V to 24V	2V	2.2µF	47µF 0805	324k	≥2.4V, <16V	700	44.2k	700	44.2k
9V to 24V	2.2V	2.2µF	22µF 0805	274k	≥2.4V, <16V	775	41.2k	775	41.2k
9V to 24V	2.5V	2.2µF	22µF 0805	226k	≥2.4V, <16V	850	36.5k	850	36.5k
9V to 24V	3.3V	2.2µF	22µF 0805	154k	AUX	950	31.6k	1100	26.7k
9V to 24V	5V	2.2µF	4.7µF 1206	93.1k	AUX	1150	25.5k	1550	16.5k
11.5V to 24V	8V	2.2µF	4.7µF 0805	53.6k	AUX	1200	23.7k	2000	11.3k
18V to 24V	10V	2.2µF	2.2µF 0805	42.2k	AUX	1250	22.6k	1450	18.2k
18V to 36V	0.82V	2.2µF	247µF 1206	13M	≥2.4V, <16V	250	150k	250	150k
18V to 36V	1V	2.2µF	200µF 1206	1.87M	≥2.4V, <16V	300	124k	300	124k
18V to 36V	1.2V	2.2µF	100µF 1206	953k	≥2.4V, <16V	325	113k	325	113k
18V to 36V	1.5V	2.2µF	100µF 1206	549k	≥2.4V, <16V	375	93.1k	375	93.1k
18V to 36V	1.8V	2.2µF	68µF 1206	383k	≥2.4V, <16V	450	79k	450	79k
18V to 36V	2V	2.2µF	47µF 0805	324k	≥2.4V, <16V	475	73.2k	475	73.2k
18V to 36V	2.2V	2.2µF	22µF 0805	274k	≥2.4V, <16V	525	64.9k	525	64.9k
18V to 36V	2.5V	2.2µF	22µF 0805	226k	≥2.4V, <16V	575	59.0k	575	59.0k
18V to 36V	3.3V	2.2µF	22µF 0805	154k	AUX	750	42.2k	750	42.2k
18V to 36V	5V	2.2µF	4.7µF 1206	93.1k	AUX	1000	29.4k	1050	28.0k
18V to 36V	8V	2.2µF	4.7µF 0805	53.6k	AUX	1200	23.7k	1600	15.8k
18V to 36V	10V	2.2µF	2.2µF 0805	42.2k	AUX	1250	22.6k	1450	18.2k
4.75V to 32V	–3.3V	2.2µF	22µF 0805	154k	AUX	700	44.2k	775	41.2k
7V to 31V	–5V	2.2µF	10µF 0805	93.1k	AUX	1000	29.4k	1075	27.4k
13V to 28V	–8V	2.2µF	10µF 0805	53.6k	AUX	1100	26.7k	1350	20.5k

*Running voltage range. Please refer to Applications Information for start-up details.

APPLICATIONS INFORMATION

For most applications, the design process is straight forward, summarized as follows:

1. In Table 1, find the row that has the desired input voltage range and output voltage.
2. Apply the recommended C_{IN}, C_{OUT}, R_{ADJ} and R_T values.
3. Connect BIAS as indicated.

While these component combinations have been tested for proper operation, it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental conditions.

If the desired output voltage is not listed in Table 1, set the output by applying an R_{ADJ} resistor whose value is given by the equation $R_{ADJ} = 394.21/(V_{OUT} – 0.79)$, where R_{ADJ} is in kΩ and V_{OUT} is in volts. Verify the LTM8022's operation over the system's intended line, load and environmental conditions.

Capacitor Selection Considerations

The C_{IN} and C_{OUT} capacitor values in Table 1 are the minimum recommended values for the associated operating conditions. Applying capacitor values below those indicated in Table 1 is not recommended, and may result in undesirable operation. Using larger values is generally acceptable, and can yield improved dynamic response, if it is necessary. Again, it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental conditions.

Ceramic capacitors are small, robust and have very low ESR. However, not all ceramic capacitors are suitable. X5R and X7R types are stable over temperature and applied voltage and give dependable service. Other types, including Y5V and Z5U, have very large temperature and voltage coefficients of capacitance. In an application circuit they may have only a small fraction of their nominal capacitance, resulting in much higher output voltage ripple than expected.

Ceramic capacitors are also piezoelectric. In Burst Mode operation, the LTM8022's switching frequency depends on the load current, and can excite a ceramic capacitor at audio frequencies, generating audible noise. Since the LTM8022 operates at a lower current limit during Burst Mode operation, the noise is typically very quiet to a casual ear.

If this audible noise is unacceptable, use a high performance electrolytic capacitor at the output. The input capacitor can be a parallel combination of a 2.2µF ceramic capacitor and a low cost electrolytic capacitor.

A final precaution regarding ceramic capacitors concerns the maximum input voltage rating of the LTM8022. A ceramic input capacitor combined with trace or cable inductance forms a high Q (under damped) tank circuit. If the LTM8022 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided; see the Hot-Plugging Safely section.

Frequency Selection

The LTM8022 uses a constant-frequency PWM architecture that can be programmed to switch from 200kHz to 2.4MHz by using a resistor tied from the R_T pin to ground. Table 2 provides a list of R_T resistor values and their resultant frequencies.

Table 2. Switching Frequency vs R_T Value

SWITCHING FREQUENCY (MHz)	R_T VALUE (kΩ)
0.2	187
0.3	121
0.4	88.7
0.5	68.1
0.6	56.2
0.7	46.4
0.8	40.2
0.9	34
1.0	29.4
1.2	23.7
1.4	19.1
1.6	16.2
1.8	13.3
2.0	11.5
2.2	9.76
2.4	8.66

Operating Frequency Tradeoffs

It is recommended that the user apply the optimal R_T value given in Table 1 for the input and output operating condition. System level or other considerations, however, may necessitate another operating frequency. While the LTM8022 is flexible enough to accommodate a wide range

APPLICATIONS INFORMATION

of operating frequencies, a haphazardly chosen one may result in undesirable operation under certain operating or fault conditions. A frequency that is too high can reduce efficiency, generate excessive heat or even damage the LTM8022 if the output is overloaded or short-circuited. A frequency that is too low can result in a final design that has too much output ripple or too large of an output cap.

The maximum frequency and corresponding R_T value at which the LTM8022 should be allowed to switch is given in Table 1 in the $R_{T(MIN)}$ and f_{MAX} columns, while the recommended frequency and R_T value over the given input range is given in the $R_{T(OPTIMAL)}$ and $f_{OPTIMAL}$ columns.

There are additional conditions that must be satisfied if the synchronization function is used. Please refer to the Synchronization section for details.

Burst Mode Operation

To enhance efficiency at light loads, the LTM8022 automatically switches to Burst Mode operation which keeps the output capacitor charged to the proper voltage while minimizing the input quiescent current. During Burst Mode operation, the LTM8022 delivers single cycle bursts of current to the output capacitor followed by sleep periods where the output power is delivered to the load by the output capacitor. In addition, V_{IN} and BIAS quiescent currents are reduced to typically 20µA and 50µA, respectively, during the sleep time. As the load current decreases towards a no load condition, the percentage of time that the LTM8022 operates in sleep mode increases and the average input current is greatly reduced, resulting in higher efficiency.

Burst Mode operation is enabled by tying SYNC to GND. To disable Burst Mode operation, tie SYNC to a stable voltage source above 0.7V. **Do not leave this pin floating.**

BIAS Pin Considerations

The BIAS pin is used to provide drive power for the internal power switching stage and operate internal circuitry. For proper operation, it must be powered by at least 2.4V. If the output voltage is programmed to be 2.4V or higher, simply tie BIAS to AUX, which is internally tied to V_{OUT}. If V_{OUT} is less than 2.4V, BIAS can be tied to V_{IN} or some other voltage source. In all cases, ensure that the maximum voltage at the BIAS pin is less than 16V and the sum of V_{IN}+ BIAS is less than 56V. If BIAS power is applied from a remote or noisy voltage source, it may be necessary to apply a decoupling capacitor locally to the LTM8022.

Minimum Input Voltage

The LTM8022 is a step-down converter, so a minimum amount of headroom is required to keep the output in regulation. For most applications at full load, the input needs to be at least 1.5V above the desired output. In addition, the input voltage required to turn on depends upon how the RUN/SS pin is tied. As shown in Figure 1, it takes more input voltage to turn on if RUN/SS is tied to V_{IN} than if the turn-on is controlled by raising RUN/SS when V_{IN} is in the required operating range. This is shown in Figure 1.

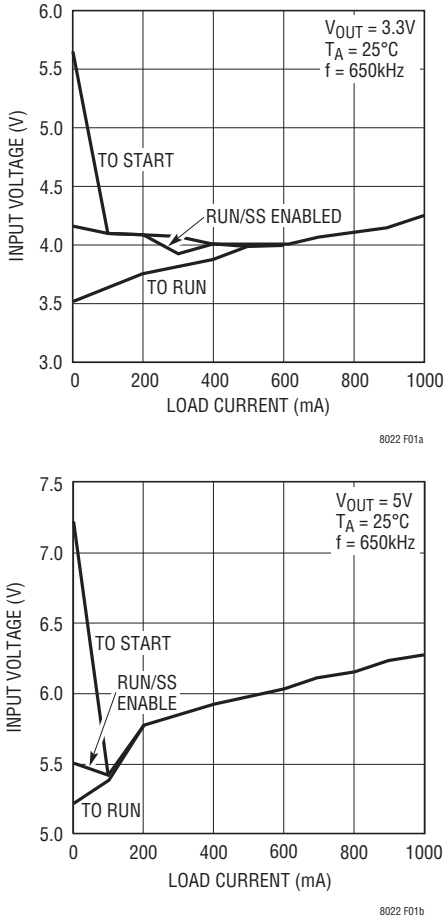


Figure 1. The LTM8022 Needs More Voltage to Start Than to Run

APPLICATIONS INFORMATION

Load Sharing

Two or more LTM8022's may be paralleled to produce higher currents. To do this, tie the V_{IN}, V_{OUT} and SHARE pins of all the paralleled LTM8022's together. Synchronize the LTM8022s to avoid beat frequencies if required. To ensure that paralleled modules start up together, the RUN/SS pins may be tied together, as well. If the RUN/SS pins are not tied together, make sure that the same valued soft-start capacitors are used for each module. An example of two LTM8022 modules configured for load sharing is given in the Typical Applications section.

Soft-Start

The RUN/SS pin can be used to soft-start the LTM8022, reducing the maximum input current during start-up. The RUN/SS pin is driven through an external RC filter to create a voltage ramp at this pin. Figure 2 shows the start-up and shutdown waveforms with the soft-start circuit. By choosing an appropriate RC time constant, the peak start-up current can be reduced to the current that is required to regulate the output, with no overshoot. Choose the value of the resistor so that it can supply at least 20µA when the RUN/SS pin reaches 2.5V.

Synchronization

The internal oscillator of the LTM8022 can be synchronized by applying an external 250kHz to 2MHz clock signal to the SYNC pin. The resistor tied from the R_T pin to ground should be chosen such that the LTM8022 would free run 20% lower than the intended synchronization frequency (see Frequency Selection section).

When the LTM8022 is synchronized to an external clock source, Burst Mode operation is disabled. The part will skip power switching cycles as necessary to maintain regulation. Ensure that the SYNC pin is not left floating. Tie it to GND if not used.

Shorted Input Protection

Care needs to be taken in systems where the output will be held high when the input to the LTM8022 is absent. This may occur in battery charging applications, or in battery backup systems where a battery or some other supply is diode ORed with the LTM8022's output. If the V_{IN} pin is allowed to float, and the RUN/SS pin is held high (either by a logic signal or because it is tied to V_{IN}), then the LTM8022's internal circuitry will pull its quiescent current through its internal power switch. This is fine if your system can tolerate a few milliamps in this state. If you ground the RUN/SS pin, the internal switch current will drop to essentially zero. However, if the V_{IN} pin is grounded while the output is held high, then parasitic diodes inside the LTM8022 can pull large currents from the output through the V_{IN} pin. Figure 3 shows a circuit that will run only when the input voltage is present and that protects against a shorted or reversed input.

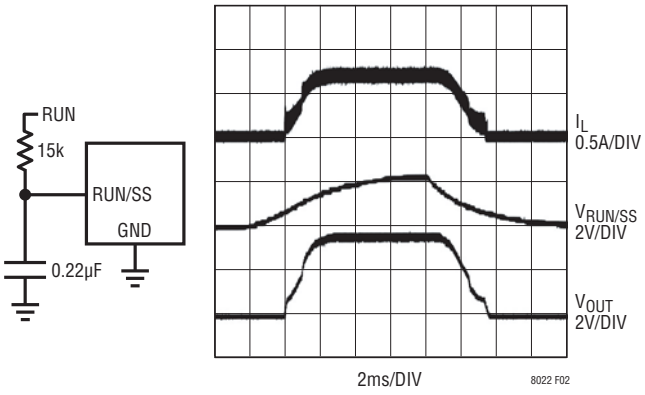


Figure 2. To Soft-Start the LTM8022, Add a Resistor and Capacitor to the RUN/SS Pin

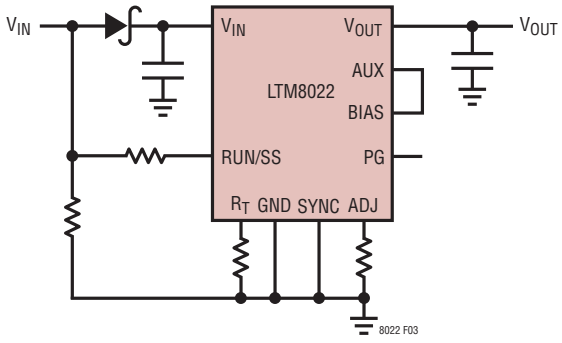


Figure 3. The Input Diode Prevents a Shorted Input from Discharging a Back-Up Battery Tied to the Output. It Also Protects the Circuit From a Reversed Input. The LTM8022 Runs Only When the Input is Present

APPLICATIONS INFORMATION

PCB Layout

Most of the headaches associated with PCB layout have been alleviated or even eliminated by the high level of integration of the LTM8022. The LTM8022 is nevertheless a switching power supply, and care must be taken to minimize EMI and ensure proper operation. Even with the high level of integration, you may fail to achieve specified operation with a haphazard or poor layout. See Figure 4 for a suggested layout.

Ensure that the grounding and heatsinking are acceptable. A few rules to keep in mind are:

1. Place the R_{ADJ} and R_T resistors as close to their respective pins as possible.
2. Place the C_{IN} capacitor as close as possible to the V_{IN} and GND connection of the LTM8022.
3. Place the C_{OUT} capacitor as close as possible to the V_{OUT} and GND connection of the LTM8022.
4. Place the C_{IN} and C_{OUT} capacitors such that their ground current flow directly adjacent or underneath the LTM8022.
5. Connect all of the GND connections to as large a copper pour or plane area as possible on the top layer. Avoid breaking the ground connection between the external components and the LTM8022.
6. Use vias to connect the GND copper area to the boards internal ground plane. Liberally distribute these GND vias to provide both a good ground connection and thermal path to the internal planes of the printed circuit board.

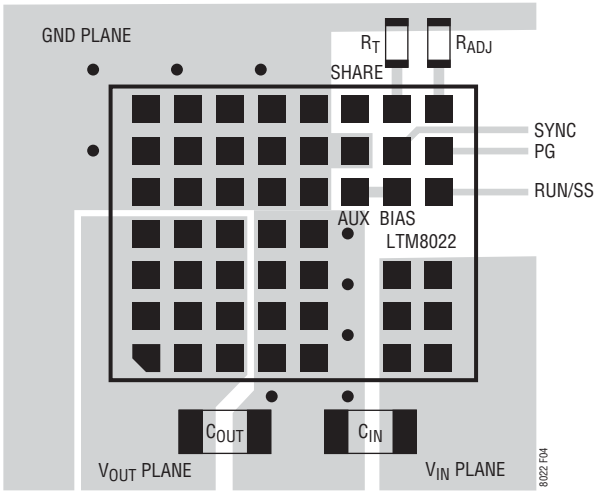


Figure 4. Layout Showing Suggested External Components, GND Plane and Thermal Vias

APPLICATIONS INFORMATION

Hot-Plugging Safely

The small size, robustness and low impedance of ceramic capacitors make them an attractive option for the input bypass capacitor of LTM8022. However, these capacitors can cause problems if the LTM8022 is plugged into a live supply (see Linear Technology Application Note 88 for a complete discussion). The low loss ceramic capacitor combined with stray inductance, in series with the power source, forms an underdamped tank circuit. In this case, the voltage at the V_{IN} pin of the LTM8022 can ring to twice the nominal input voltage, possibly exceeding the LTM8022's rating and damaging the part. If the input supply is poorly controlled or the user will be plugging the LTM8022 into an energized supply, the input network should be designed to prevent this overshoot. Figure 5 shows the waveforms that result when an LTM8022 circuit is connected to a 24V supply through six feet of 24-gauge twisted pair. The first plot is the response with a 2.2µF ceramic capacitor at the input. The input voltage rings as high as 35V and the input current peaks at 20A. One method of damping the tank circuit is to add another capacitor with a series resistor to the circuit. In Figure 5b an aluminum electrolytic capacitor has been added. This capacitor's high equivalent series resistance damps the circuit and eliminates the voltage overshoot. The extra capacitor improves low frequency ripple filtering and can slightly improve the efficiency of the circuit, though it is likely to be the largest component in the circuit. An alternative solution is shown in Figure 5c. A 0.7Ω resistor is added in series with the input to eliminate the voltage overshoot (it also reduces the peak input current). A 0.1µF capacitor improves high frequency filtering. This solution is smaller and less expensive than the electrolytic capacitor. For high input voltages its impact on efficiency is minor, reducing efficiency less than one half percent for a 5V output at full load operating from 24V.

Thermal Considerations

The LTM8022 output current may need to be derated if it is required to operate in a high ambient temperature or deliver a large amount of power. The amount of current derating is dependent upon the input voltage, output power and ambient temperature. The derating curves in the Typical Performance Characteristics section can be used as a guide. These curves were generated by an LTM8022 mounted to a 33cm^2 4-layer FR4 printed circuit board. Boards of other sizes and layer count can exhibit different thermal behavior, so it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental operating conditions.

The junction to air and junction to board thermal resistances given in the Pin Configuration diagram may also be used to estimate the LTM8022 internal temperature. These thermal coefficients are determined per JESD 51-9 (JEDEC standard, test boards for area array surface mount package thermal measurements) through analysis and physical correlation. Bear in mind that the actual thermal resistance of the LTM8022 to the printed circuit board depends upon the design of the circuit board. The die temperature of the LTM8022 must be lower than the maximum rating of 125°C, so care should be taken in the layout of the circuit to ensure good heat sinking of the LTM8022.

The bulk of the heat flow out of the LTM8022 is through the bottom of the module and the LGA pads into the printed circuit board. Consequently a poor printed circuit board design can cause excessive heating, resulting in impaired performance or reliability. Please refer to the PCB Layout section for printed circuit board design suggestions.

Finally, be aware that at high ambient temperatures the internal Schottky diode will have significant leakage current (see Typical Performance Characteristics) increasing the quiescent current of the LTM8022.

APPLICATIONS INFORMATION

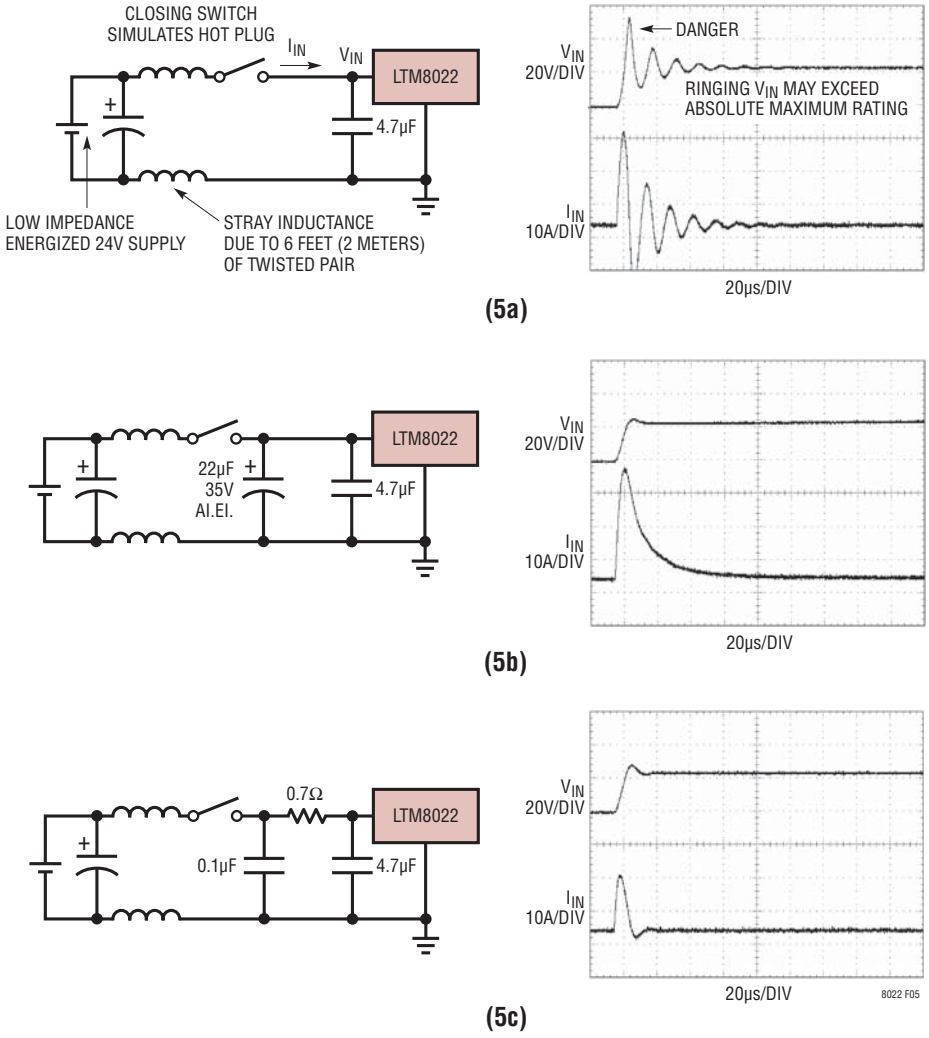
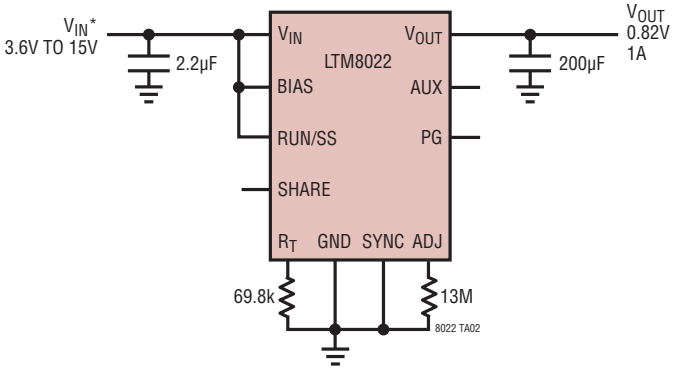


Figure 5. A Well Chosen Input Network Prevents Input Voltage Overshoot and Ensures Reliable Operation When the LTM8022 is Connected to a Live Supply

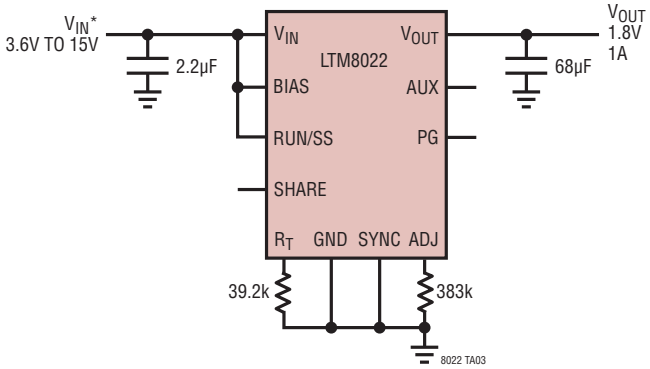
TYPICAL APPLICATIONS

0.82V Step-Down Converter



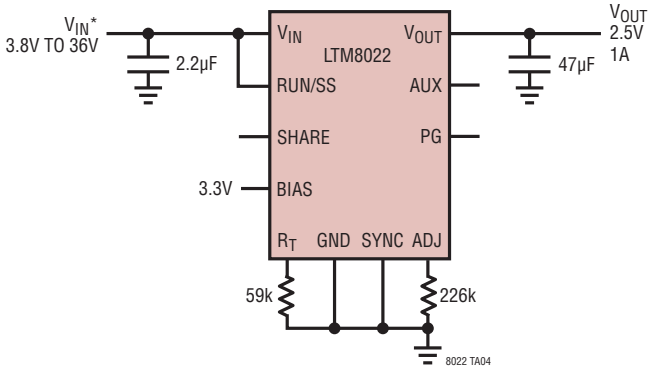
*RUNNING VOLTAGE RANGE. PLEASE REFER TO APPLICATIONS INFORMATION FOR START-UP DETAILS

1.8V Step-Down Converter



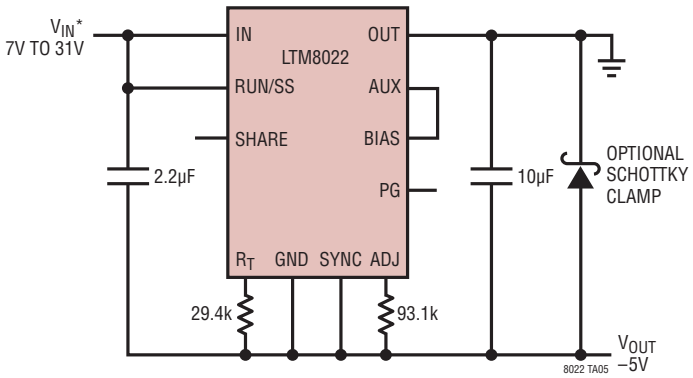
*RUNNING VOLTAGE RANGE. PLEASE REFER TO APPLICATIONS INFORMATION FOR START-UP DETAILS

2.5V Step-Down Converter



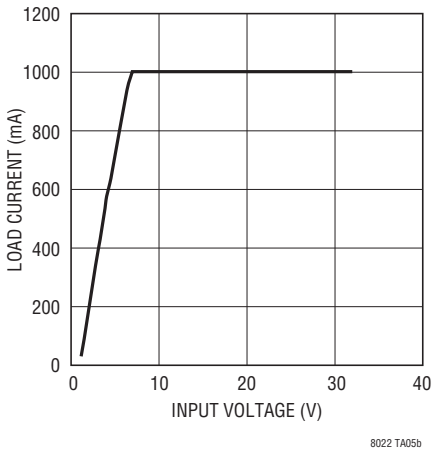
*RUNNING VOLTAGE RANGE. PLEASE REFER TO APPLICATIONS INFORMATION FOR START-UP DETAILS

–5V at 1A Positive-to-Negative Converter



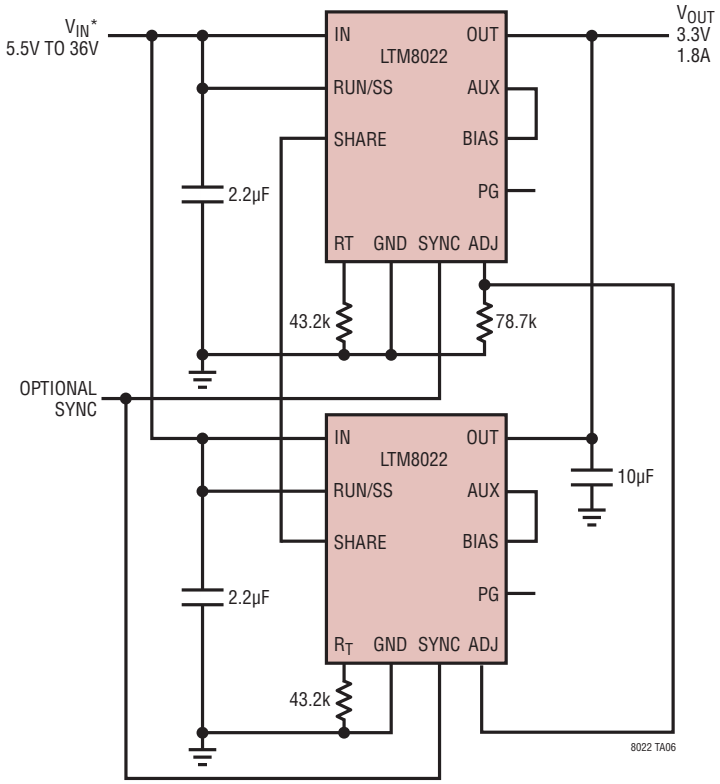
*RUNNING VOLTAGE RANGE. PLEASE REFER TO APPLICATIONS INFORMATION FOR START-UP DETAILS

–5V at 1A Positive-to-Negative Converter Load Current vs Input Voltage



TYPICAL APPLICATIONS

Two LTM8022's in Parallel, 3.3V at 1.8A

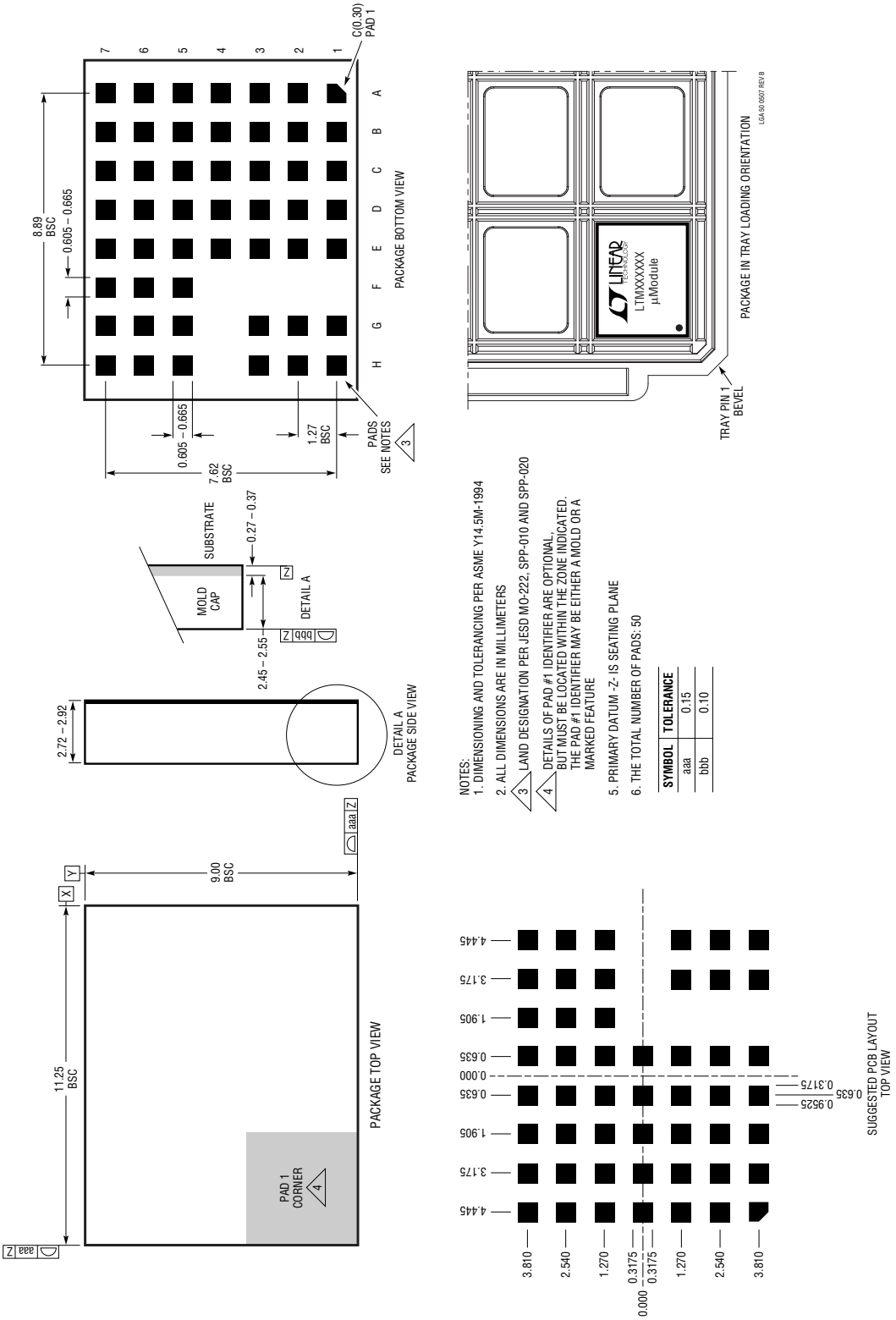


*RUNNING VOLTAGE RANGE. PLEASE REFER TO APPLICATIONS INFORMATION FOR START-UP DETAILS

NOTE: SYNCRONIZE THE TWO MODULES TO AVOID BEAT FREQUENCIES IF REQUIRED. OTHERWISE, TIE EACH SYNC TO GND

PACKAGE DESCRIPTION

LGA Package
50-Lead (11.25mm × 9.00mm × 2.82mm)
(Reference LTC DWG # 05-08-1804 Rev B)



PACKAGE DESCRIPTION

Table 3. LTM8022 Pinout (Sorted by Pin Number)

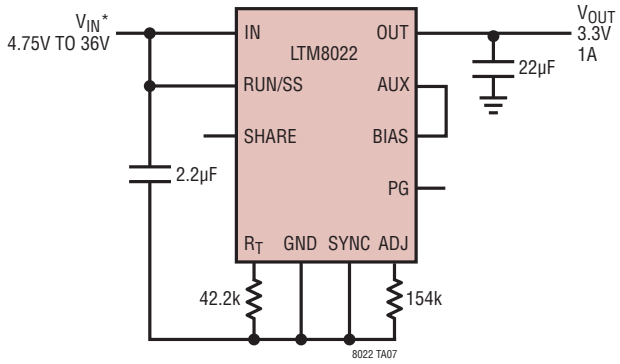
PIN	SIGNAL DESCRIPTION	PIN	SIGNAL DESCRIPTION
A1	V_{OUT}	D5	GND
A2	V_{OUT}	D6	GND
A3	V_{OUT}	D7	GND
A4	V_{OUT}	E1	GND
A5	GND	E2	GND
A6	GND	E3	GND
A7	GND	E4	GND
B1	V_{OUT}	E5	GND
B2	V_{OUT}	E6	GND
B3	V_{OUT}	E7	GND
B4	V_{OUT}	F5	AUX
B5	GND	F6	GND
B6	GND	F7	SHARE
B7	GND	G1	V_{IN}
C1	V_{OUT}	G2	V_{IN}
C2	V_{OUT}	G3	V_{IN}
C3	V_{OUT}	G5	BIAS
C4	V_{OUT}	G6	SYNC
C5	GND	G7	R_T
C6	GND	H1	V_{IN}
C7	GND	H2	V_{IN}
D1	GND	H3	V_{IN}
D2	GND	H5	RUN/SS
D3	GND	H6	PG
D4	GND	H7	ADJ

REVISION HISTORY (Revision history begins at Rev D)

REV	DATE	DESCRIPTION	PAGE NUMBER
D	8/10	Added Note 5	3

TYPICAL APPLICATION

3.3V Step Down Converter



*RUNNING VOLTAGE RANGE. PLEASE REFER TO APPLICATIONS INFORMATION FOR START-UP DETAILS

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4600/LTM4602	10A and 6A DC/DC µModule	Pin Compatible, 4.5V ≤ V_{IN} ≤ 28V
LTM4601/LTM4603	12A and 6A DC/DC µModule	Pin Compatible; Remote Sensing; PLL, Tracking and Margining, 4.5V ≤ V_{IN} ≤ 28V
LTM4604/LTM4608	4A, 8A Low Voltage DC/DC µModule	2.375V ≤ V_{IN} ≤ 5.5V, 9mm × 15mm × 2.3mm (LTM4604), 9mm × 15mm × 2.5mm (LTM4608)
LTM4605/LTM4607	Buck-Boost DC/DC µModule	Up to 160W, External Inductor; High Efficiency (Up to 98%), 15mm × 15mm × 2.8mm LGA
LTM8020	200mA, 36V DC/DC µModule	4V ≤ V_{IN} ≤ 36V, 1.25V ≤ V_{OUT} ≤ 5V, 6.25mm × 6.25mm × 2.32mm LGA
LTM8023	2A, 36V DC/DC µModule	3.6V ≤ V_{IN} ≤ 36V, 0.8V ≤ V_{OUT} ≤ 10V, 11.25mm × 9mm × 2.82mm LGA, Pin Compatible with LTM8022

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