ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise specified) (Note 1)			
PARAMETER	**SYMBOL**	**LIMIT**	**UNIT**
Input Voltage Range	V_{IN} to GND	-0.5 ~ +470	V
Internal Regulated Voltage	V_{DD} to GND	12	V
CS, LD, PWMD, Gate, RT to GND		-0.3 ~ (V_{DD}+0.3)	V
Continuous Power Dissipation (Note 2)	P_D	650	mW
Storage Temperature Range	T_A	-65 to +150	°C
Junction Temperature Range	T_J	-40 to +150	°C

THERMAL PERFORMANCE (Note 3)			
PARAMETER	**SYMBOL**	**LIMIT**	**UNIT**
Thermal Resistance – Junction to Ambient	$R_{\theta JA}$	128	°C/W

ELECTRICAL SPECIFICATIONS (T_A= 25°C, V_{IN}= 12V, V_{LD}=PWM=V_{DD}, unless otherwise noted) (Note 4)						
PARAMETER	**SYMBOL**	**CONDITION**	**MIN**	**TYP**	**MAX**	**UNIT**
Input						
DC Input Voltage Range	V_{INDC}	DC input voltage	8.0	--	450	V
Shut-down Mode Supply Current	I_{INSD}	Pin PWMD to GND	--	0.5	1.0	mA
Internal Regulator						
Internally Regulated Voltage	V_{DD}	V_{IN}=8V, $I_{DD(EXT)}$=0, 500pF at Gate, R_T=226kΩ	7.25	7.5	7.75	V
Line Regulation of V_{DD}	ΔV_{DDLine}	V_{IN}=8~450V, $I_{DD(EXT)}$=0 500pF at Gate, R_T=226kΩ	0	--	1.0	V
Load Regulation of V_{DD}	ΔV_{DDLoad}	$I_{DD(EXT)}$= 0 ~ 1mA 500pF at Gate, R_T=226kΩ	0	--	100	mV
Undervoltage Lockout Threshold	UVLO	V_{IN} rising	6.45	6.7	6.95	V
Undervoltage Lockout Hysteresis	ΔUVLO	V_{IN} falling	--	500	--	mV
Maximum Input Current	$I_{IN\ (MAX)}$	V_{IN}=8V	3.5	--	--	mA
Dimming						
PWMD Input Low Voltage	V_{ENL}	V_{IN}=8V~450V	--	--	0.8	V
PWMD Input High Voltage	V_{ENH}	V_{IN}=8V~450V	2.0	--	--	V
PWMD Pull-down resistance at PWMD	R_{EN}	V_{PWMD}=5V	50	100	150	kΩ

ELECTRICAL SPECIFICATIONS (T_A= 25°C, V_{IN}= 12V, V_{LD}=PWM=V_{DD}, unless otherwise noted)						
PARAMETER	**SYMBOL**	**CONDITION**	**MIN**	**TYP**	**MAX**	**UNIT**
Average Current Sense Logic						
Current Sense Reference Voltage	V_{CS}		238	250	262	mV
LD to Current Sense Ratio	$Av_{(LD)}$		--	0.18	--	mV
LD input Voltage Shutdown	$V_{LD(OFF)}$	V_{LD} falling	--	150	--	mV
LD input Voltage Enable	$\Delta V_{LD(OFF)}$	V_{LD} rising	--	200	--	mV
Current Sense Blanking Interval	T_{BLANK}		150	--	280	ns
Minimum On-Time	$T_{ON(min)}$	V_{CS}= V_{CS} + 30mV	--	--	1	µS
Off Time	T_{OFF}	R_T=1MΩ	32	--	48	µS
		R_T=226kΩ	8	--	12	
Max. Steady-State Duty Cycle	D_{MAX}		75	--	--	%
Short Circuit Protection						
Hiccup Threshold Voltage	V_{CS}		410	--	470	mV
Current Limit Delay CS to Gate	T_{DELAY}	V_{CS}= V_{CS} + 30mV	--	--	150	ns
Short Circuit Hiccup Time	T_{HICCUP}		330	--	460	µS
Minimum On-Time (Short Circuit)	$T_{ON(min)}$	V_{CS}= V_{DD}	--	--	430	µS
Gate Driver						
Gate Sourcing Current	I_{SOURCE}	V_{GATE}=0V, V_{DD}=7.5V	165	--	--	mA
Gate Sinking Current	I_{SINK}	V_{GATE}=V_{DD}, V_{DD}=7.5V	165	--	--	mA
Gate Output Rise Time	T_{RISE}	C_{GATE}=500pF, V_{DD}=7.5V	--	30	50	ns
Gate Output Fall Time	T_{FALL}	C_{GATE}=500pF, V_{DD}=7.5V	--	30	50	ns

Note:

1. Stresses listed as the above “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.
2. Limited by package power dissipation, whichever is lower.
3. Thermal Resistance is specified with the component mounted on a low effective thermal conductivity test board in free air at T_A=25°C.
4. Denotes the specifications which apply over the full operating ambient temperature range of -40ºC<T_A<+125ºC.

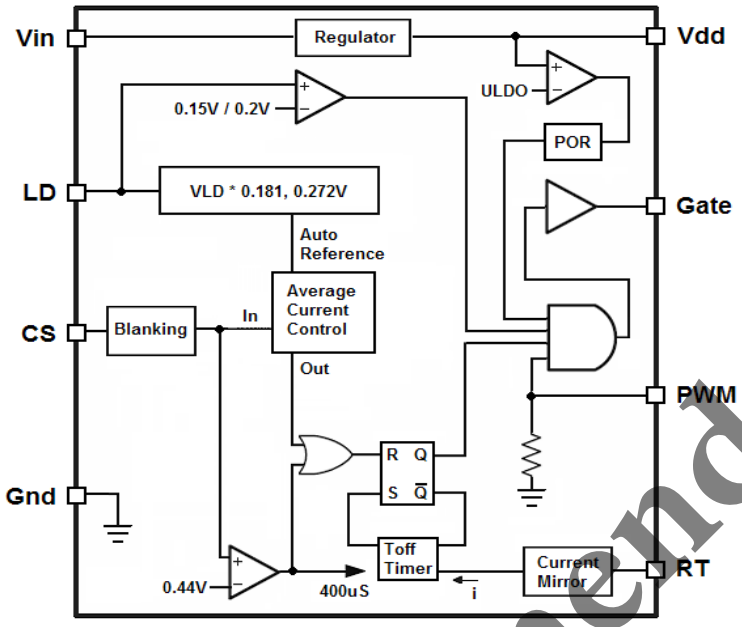
ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TS19460CS RLG	SOP-8	2,500pcs / 13” Reel

Note:

1. Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC.
2. Halogen-free according to IEC 61249-2-21 definition.

FUNCTION BLOCK DIAGRAM



PIN DESCRIPTION

PIN NO.	NAME	FUNCTION
1	VIN	This pin is the input of 8V~450V linear regulator
2	CS	This pin is the current sense pin used to sense the MOSFET current by means of an external sense resistor.
3	GND	Ground return for all internal circuitry. This pin must be electrically connected to the ground of the power train.
4	GATE	This pin is the output GATE driver for an external N-CH Power MOSFET
5	PWMD	This is the PWM dimming input of the IC. When this pin is pulled to GND, the Gate Driver is turned off. When the pin is pulled high, the GATE driver operates normally.
6	VDD	This is the power supply pin for all internal circuits. It must be bypassed with a low ESR capacitor to GND (≥0.1μF)
7	LD	This pin is the linear dimming input and sets the current sense threshold as long as the voltage at the pin is less than 1.5V, The Gate output is disable when LD voltage <150mV(typ.) and recovery when LD voltage >200mV (typ.)
8	RT	A resistor is connected between RT and GND to program the Gate off-time.

APPLICATION INFORMATION

The TS19460 is optimized to drive buck LED drivers using average current mode control. This method of control enables fairly accurate LED current control without the need for high side current sensing or the design of any closed loop controllers. The IC uses very few external components and enables both linear and PWM dimming of the LED current.

A resistor connected to the RT pin programs the off-time. Constant off-time control average current mode is used for stability and to improve the LED current regulation over a wide range of input voltages.

The current through the switching MOSFET source is averaged and used to give constant-current feedback. This current is detected from a sense resistor at the CS pin, the feedback operates in a fast open-loop mode, there is no compensation required, the output current is programmed as

$$I_{LED} = 0.25V / R_{CS}$$

When the Voltage at the LD input >1.5V, otherwise

$$I_{LED} = (V_{LD} * 0.181) / R_{CS}$$

When application to design the inductor witching ripple current in it is 40% of average peak to peak, full load current, the inductance can be calculated as follow:

$$L_{OUT} = (V_{OUT(max)} * T_{OFF}) / (0.4 * I_{OUT})$$

The duty cycle range of current control feedback is limited to duty <75%, A reduction in the LED current string voltage is greater than 75% of input voltage.

Reducing the output LED voltage is below $V_{OUT(MIN)} = V_{IN} * D_{(MIN)}$, where $D_{(MIN)} = 1uS / (T_{OFF} + 1uS)$, may also result in the loss of regulation of LED current. This condition will cause an increase in the LED current and can be possible to trip the short circuit protection comparator.

The short circuit protection comparator trips when the voltage at CS exceeds 0.44V, the Gate off time (T_{HICCUP} = 400μs) is generated to prevent stair-casing of inductor current and potentially its saturation due to insufficient output voltage.

The leading edge blanking delay is provided at CS to prevent false triggering of current feedback and short circuit protection.

Input Voltage Regulator

The TS19460 can be powered directly from its V_{IN} pin and can work from $8.0V_{DC}$~$450V_{DC}$ at its V_{IN} pin. When a voltage is applied at the V_{IN} pin, the TS19460 maintains a constant 7.5V at the V_{DD} pin. This voltage is used to power the IC and any external resistor dividers needed to control the IC. The V_{DD} pin must be bypassed by a low ESR capacitor to provide a low impedance path for the high frequency current of the output GATE driver. The TS19460 can be also operated by supplying a voltage at the V_{DD} pin greater than the internally regulated voltage. Please note that this external voltage at the V_{DD} pin should not exceed 12V.

Although the V_{IN} pin of the TS19460 is rated up to 450V, the actual maximum voltage that can be applied is limited by the power dissipation in the IC. For example, if an SOP-8 (junction to ambient thermal resistance $R\theta_{JA}$ = 128°C/W) TS19460 draws about I_{IN} = 2.0mA from the V_{IN} pin, and has a maximum allowable temperature rise of the junction temperature limited to about the maximum voltage at the V_{IN} pin would be:

$$V_{IN(MAX)} = (T_{J(MAX)} - T_A) / (R\theta_{JA} * I_{IN}) = 390V$$

APPLICATION INFORMATION (CONTINUE)

In these cases, to operate the TS19460 from higher input voltages, a Zener diode can be added in series with the VIN pin to divert some of the power loss from the TS19460 to the Zener diode. In the above example, using a 100V Zener diode will allow the circuit to easily work up to 490V.

The input current drawn from the V_{IN} pin is a sum of the 1.0mA current drawn by the internal circuit and the current drawn by the GATE driver (which in turn depends on the switching frequency and the GATE charge of the external.

$$\mathbf{I_{IN} \approx 1mA + Q_G \times f_S}$$

In the above equation, f_S is the switching frequency and Q_G is the GATE charge of the external MOSFET (which can be obtained from the datasheet of the MOSFET).

Oscillator

The oscillator in the TS19460 is controlled by a single resistor connected at the RT pin. The equation governing the off-time of the GATE output is given by:

$$\mathbf{T_{OFF(\mu S)} = (RT_{(k\Omega)} / 25) + 0.3}$$

*within the range of $30k\Omega \le R_T \le 1M\Omega$

Linear Dimming

The Linear Dimming pin is used to control the LED current, when voltage at LD is fall below 1.5V, the internal reference voltage (250mV) to the constant current feedback become over ridden by V_{LD} * 0.181, and the current in the inductor remain continuous, the LED current is given by $I_{LED} = (V_{LD} * 0.181) / R_{CS}$, The Gate output is disable when LD voltage <150mV(typ.) and recovery when LD voltage >200mV (typ.)

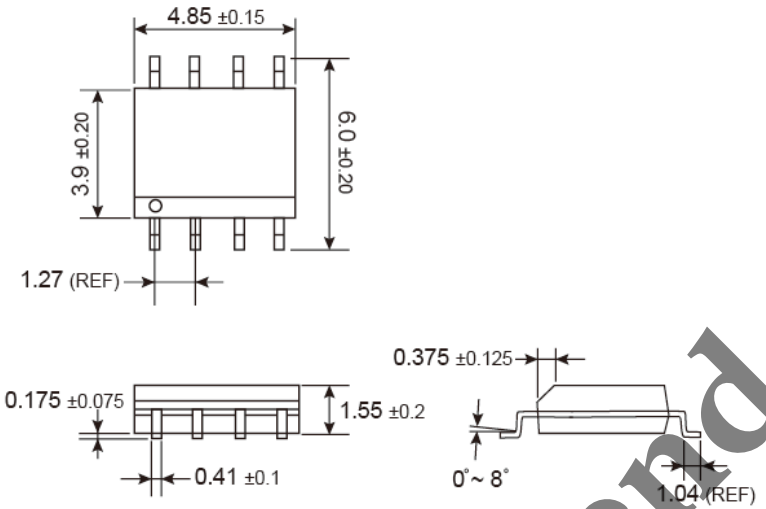
The Linear Dimming input could also be used for mixed-mode dimming to expand the dimming ratio, in this kind of application condition, the pulse-width modulated signal of a measured amplitude below 1.5V should be applied at LD.

PWM Dimming

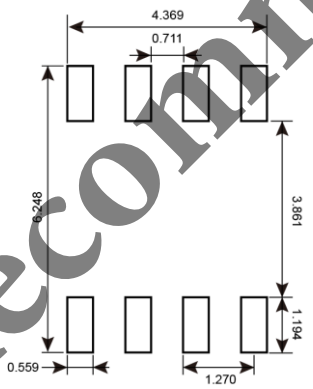
PWM Dimming can be achieved by driving the PWMD pin with a square wave signal. The rising and falling edges are limited by current slew rate in inductor, the first switching cycle is terminated upon reaching the level (250mV) at CS, the circuit is further reaching its steady state within 3~5 switching cycle regardless of the switching frequency.

PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

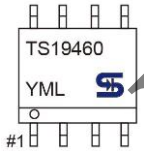
SOP-8



SUGGESTED PAD LAYOUT (Unit: Millimeters)



Marking Diagram



Y = Year Code
M = Month Code for Halogen Free Product

O =Jan	**P** =Feb	**Q** =Mar	**R** =Apr
S =May	**T** =Jun	**U** =Jul	**V** =Aug
W =Sep	**X** =Oct	**Y** =Nov	**Z** =Dec

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