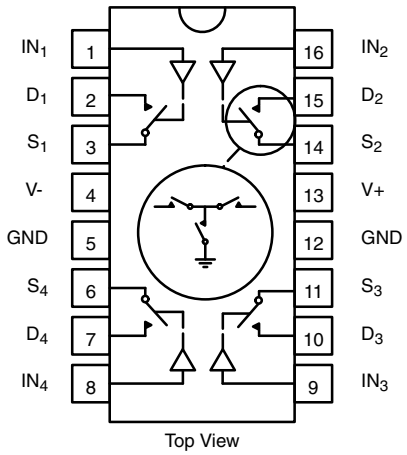
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG541

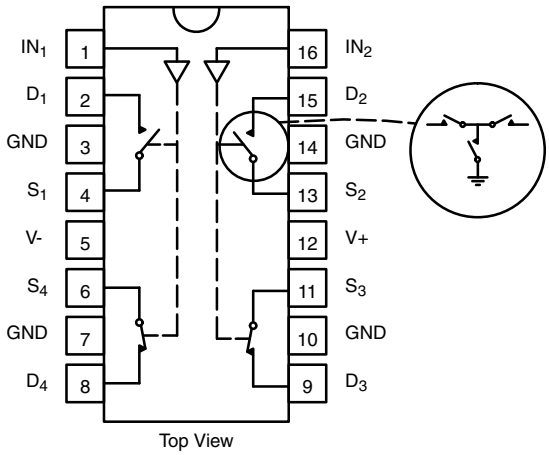
Dual-In-Line and SOIC



Top View

DG542

Dual-In-Line and SOIC



Top View

TRUTH TABLE - DG541	
Logic	**Switch**
0	OFF
1	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2 V

TRUTH TABLE - DG542		
Logic	**SW_1, SW_2**	**SW_3, SW_4**
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2 V

ORDERING INFORMATION		
Temp Range	**Package**	**Part Number**
DG540		
- 40 to 85 °C	20-Pin Plastic DIP	DG540DJ-E3
	20-Pin PLCC	DG540DN-E3
- 55 to 125 °C	20-Pin Sidebraze	DG540AP
		DG540AP/883
DG541		
- 40 to 85 °C	16-Pin Plastic DIP	DG541DJ-E3
	16-Pin Narrow SOIC	DG541DY-T1-E3
- 55 to 125 °C	16-Pin Sidebraze	DG541AP
		DG541AP/883, 5962-9076401MEA
DG542		
- 40 to 85 °C	16-Pin Plastic DIP	DG542DJ-E3
	16-Pin Narrow SOIC	DG542DY-T1-E3
- 55 to 125 °C	16-Pin Sidebraze	DG542AP
		DG542AP/883, 5962-91555201MEA

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)				
Parameter		**Symbol**	**Limit**	**Unit**
V+ to V-			- 0.3 to 21	V
V+ to GND			- 0.3 to 21	
V- to GND			- 19 to + 0.3	
Digital Inputs			(V-) - 0.3 to (V+) + 0.3 or 20 mA, whichever occurs first	
V_S, V_D			(V-) - 0.3 to (V+) + 14 or 20 mA, whichever occurs first	
Continuous Current (Any Terminal)			20	mA
Current, S or D (Pulsed at 1 ms, 10 % duty cycle max)			40	
Storage Temperature	(AP Suffix)		- 65 to 150	°C
	(DJ, DN, DY Suffixes)		- 65 to 125	
Power Dissipation (Package)[a]	16-Pin Plastic DIP[b]		470	mW
	20-Pin Plastic DIP[c]		800	
	16-Pin Narrow Body SOIC[d]		640	
	20-Pin PLCC[d]		800	
	16-, 20-Pin Sidebraze DIP[e]		900	

Notes:
a. All leads welded or soldered to PC Board.
b. Derate 6.5 mW/°C above 25 °C.
c. Derate 7 mW/°C above 25 °C.
d. Derate 10 mW/°C above 75 °C.
e. Derate 12 mW/°C above 75 °C.

SCHEMATIC DIAGRAM (typical channel)

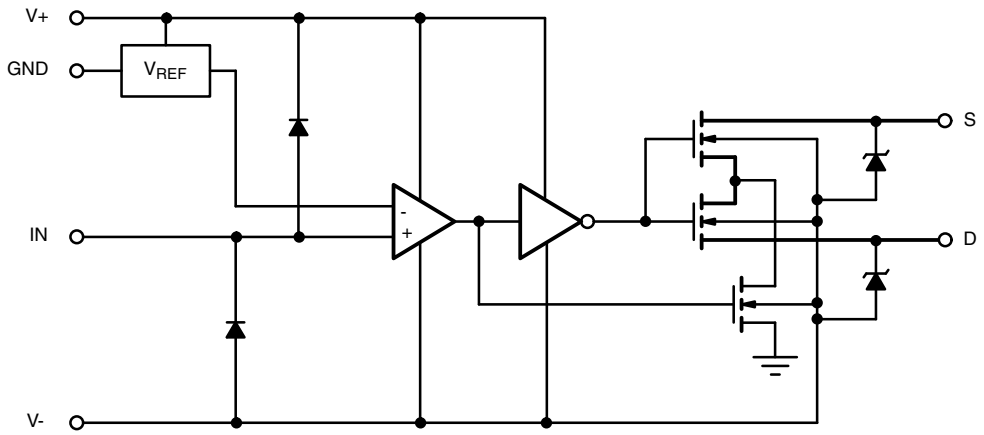


Figure 1.

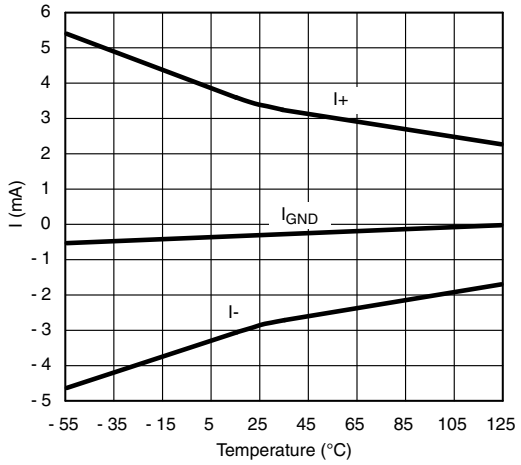
SPECIFICATIONS[a]

Parameter	Symbol	Test Conditions Unless Specified V+ = 15 V, V- = - 3 V V_{INH} = 2 V, V_{INL} = 0.8 V[f]		Temp.[b]	Typ.[c]	A Suffix - 55 °C to 125 °C Min.[d]	A Suffix - 55 °C to 125 °C Max.[d]	D Suffixes - 40 °C to 85 °C Min.[d]	D Suffixes - 40 °C to 85 °C Max.[d]	Unit
Analog Switch										
Analog Signal Range	V_{ANALOG}	V- = - 5 V, V+ = 12		Full		- 5	5	- 5	5	V
Drain-Source On-Resistance	$R_{DS(on)}$	I_S = - 10 mA, V_D = 0 V		Room Full	30		60 100		60 75	Ω
$R_{DS(on)}$ Match	$\Delta R_{DS(on)}$			Room	2		6		6	
Source Off Leakage Current	$I_{S(off)}$	V_S = 0 V, V_D = 10 V		Room Full	- 0.05	- 10 - 500	10 500	- 10 - 100	10 100	nA
Drain Off Leakage Current	$I_{D(off)}$	V_S = 10 V, V_D = 0 V		Room Full	- 0.05	- 10 - 500	10 500	- 10 - 100	10 100	
Channel On Leakage Current	$I_{D(on)}$	V_S = V_D = 0 V		Room Full	- 0.05	- 10 - 1000	10 1000	- 10 - 100	10 100	
Digital Control										
Input Voltage High	V_{INH}			Full		2		2		V
Input Voltage Low	V_{INL}			Full			0.8		0.8	
Input Current	I_{IN}	V_{IN} = GND or V+		Room Full	0.05	- 1 - 20	1 20	- 1 - 20	1 20	µA
Dynamic Characteristics										
On State Input Capacitance[e]	$C_{S(on)}$	V_S = V_D = 0 V		Room	14		20		20	pF
Off State Input Capacitance[e]	$C_{S(off)}$	V_S = 0 V		Room	2		4		4	
Off State Output Capacitance[e]	$C_{D(off)}$	V_D = 0 V		Room	2		4		4	
Bandwidth	BW	R_L = 50 Ω , See Figure 5		Room	500					MHz
Turn-On Time	t_{ON}	R_L = 1 kΩ C_L = 35 pF 50 % to 90 % See Figure 2	DG540 DG541	Room Full	45		70 130		70 130	ns
			DG542	Room Full	55		100 160		100 160	
Turn-Off Time	t_{OFF}		DG540 DG541	Room Full	20		50 85		50 85	
			DG542	Room Full	25		60 85		60 85	
Charge Injection	Q	C_L = 1000 pF, V_S = 0 V See Figure 3		Room	- 25					pC
Off Isolation	OIRR	R_{IN} = 75 Ω, R_L = 75 Ω f = 5 MHz See Figure 4	DG540	Room	- 80					dB
			DG541	Room	- 60					
			DG542	Room	- 75					
All Hostile Crosstalk	$X_{TALK(AH)}$	R_{IN} = 10 Ω, R_L = 75 Ω f = 5 MHz, See Figure 6		Room	- 85					
Power Supplies										
Positive Supply Current	I+	All Channels On or Off		Room Full	3.5		6 9		6 9	mA
Negative Supply Current	I-			Room Full	- 3.2	- 6 - 9		- 6 - 9		

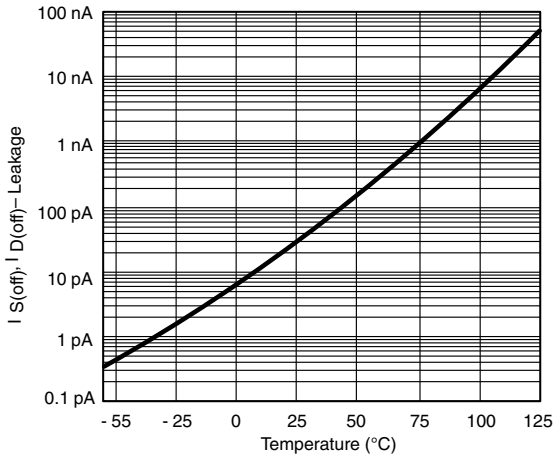
Notes:
a. Refer to PROCESS OPTION FLOWCHART .
b. Room = 25 °C, full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

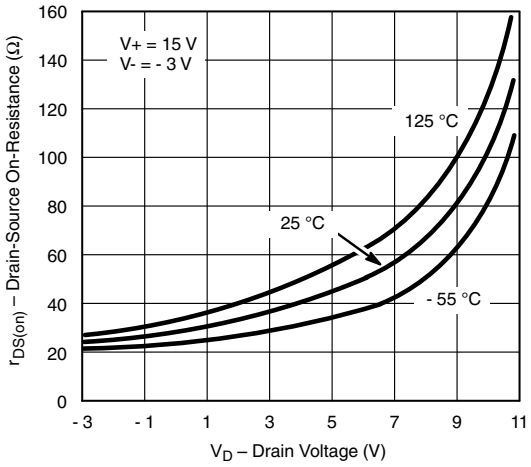
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



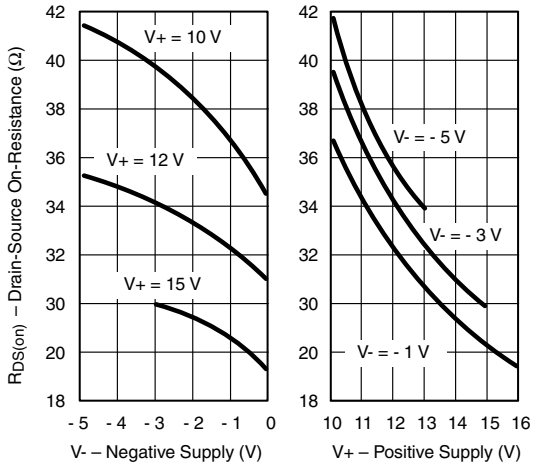
Supply Curent vs. Temperature



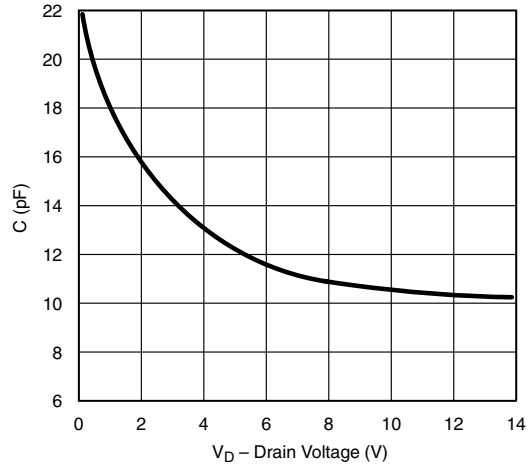
$I_{D(off)}$, $I_{S(off)}$ vs. Temperature



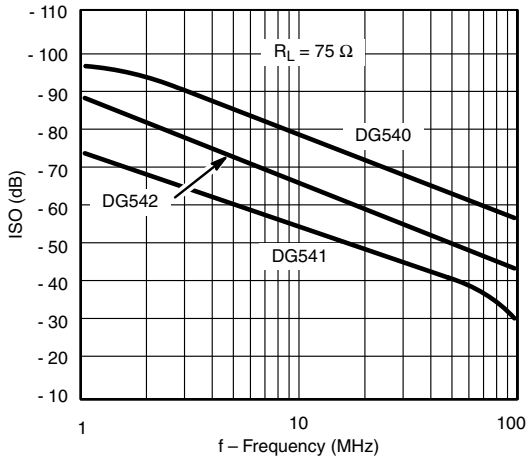
$R_{DS(on)}$ vs. Drain Voltage



V+ Constant **V- Constant**

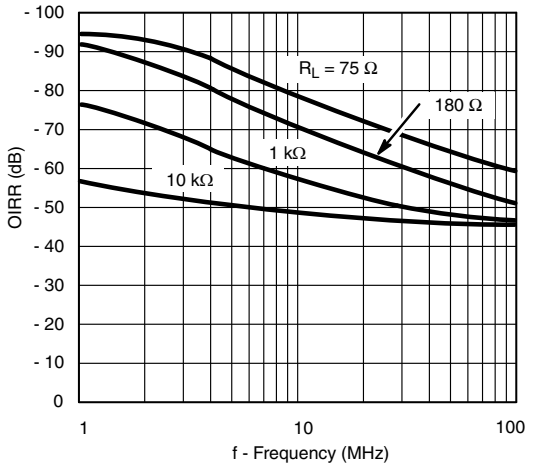


On Capacitance

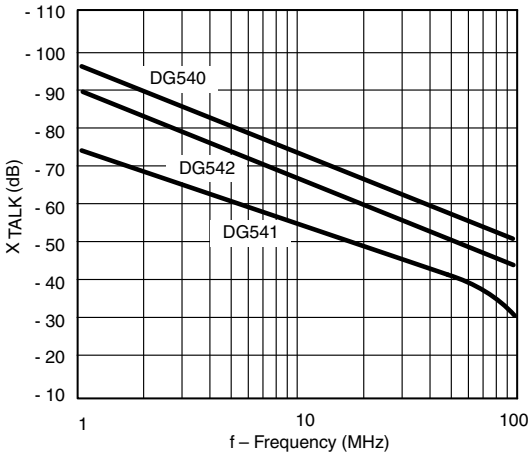


Off Isolation

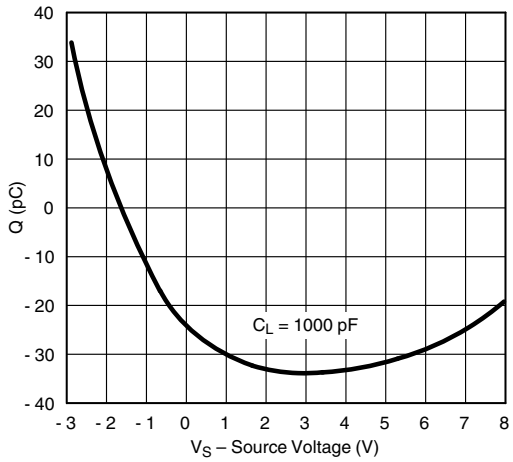
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



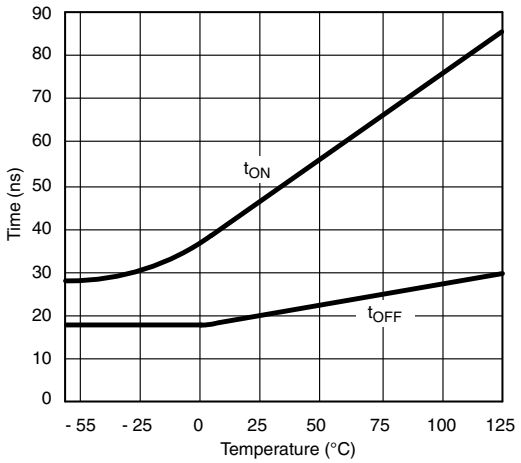
Off Isolation vs. Frequency and Load Resistance (DG540)



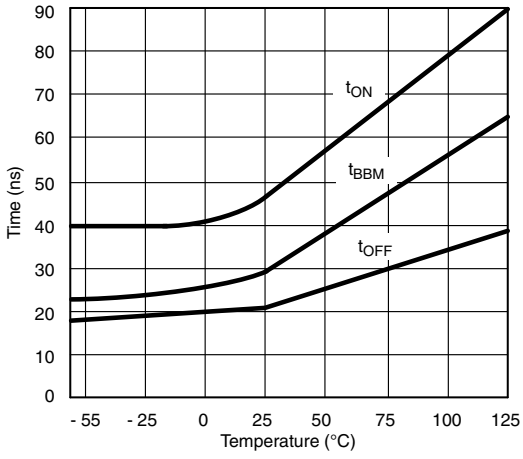
All Hostile Crosstalk



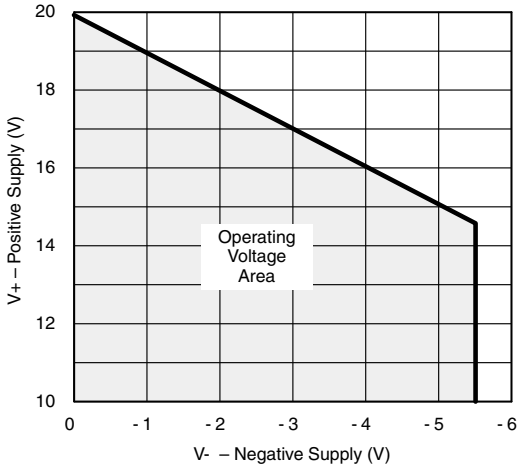
Charge Injection vs. V_S



Switching Times vs. Temperature (DG540/541)

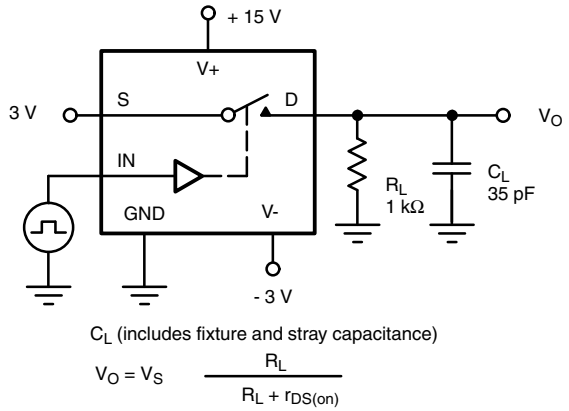


Switching and Break-Before-Make Time vs. Temperature (DG542)



Operating Supply Voltage Range

TEST CIRCUITS



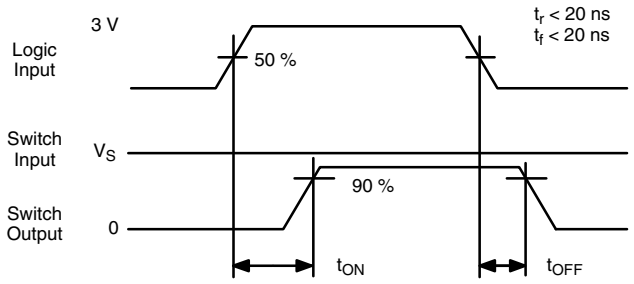
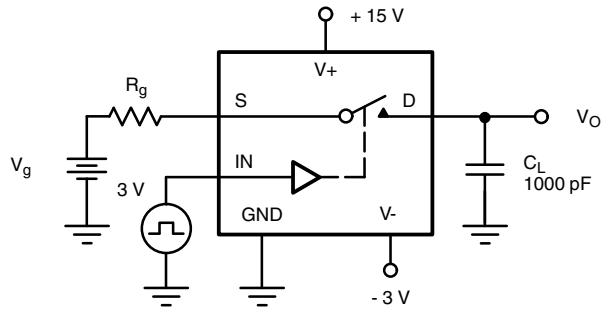
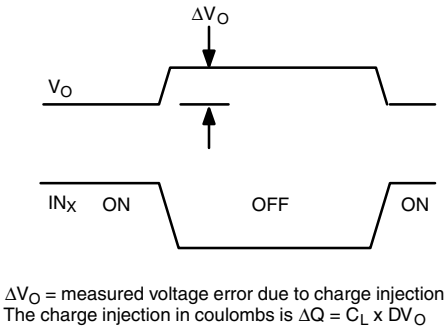


Figure 2. Switching Time





ΔV_O = measured voltage error due to charge injection
The charge injection in coulombs is $\Delta Q = C_L \times DV_O$

Figure 3. Charge Injection

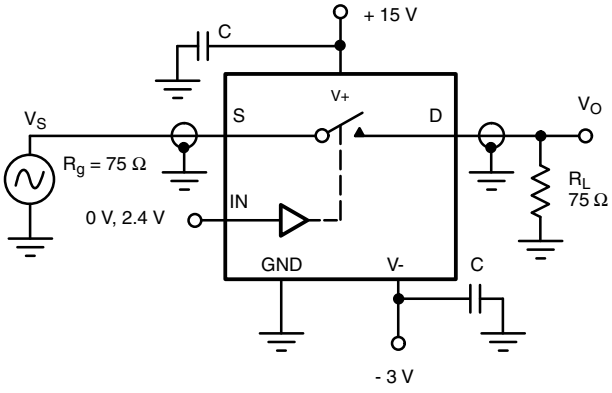


Figure 4. Off Isolation

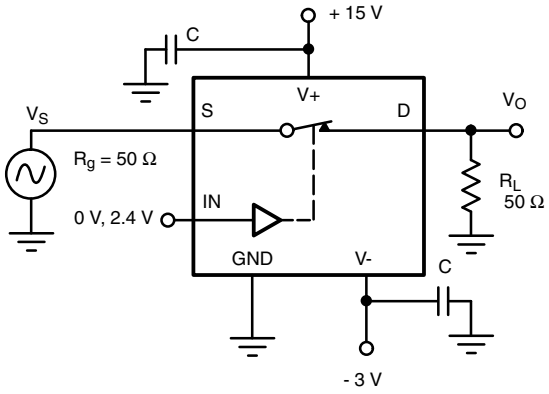


Figure 5. Bandwidth

TEST CIRCUITS

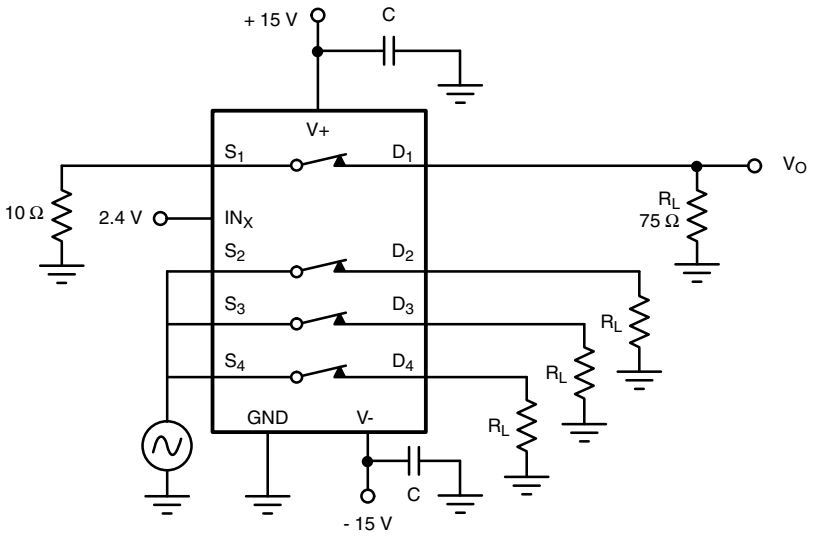


Figure 6. All Hostile Crosstalk

APPLICATIONS

Device Description

The DG540, DG541, DG542 family of wideband switches offers true bidirectional switching of high frequency analog or digital signals with minimum signal crosstalk, low insertion loss, and negligible non-linearity distortion and group delay. Built on the Siliconix D/CMOS process, these "T" switches provide excellent off-isolation with a bandwidth of around 500 MHz (350 MHz for DG541). Silicon-gate D/CMOS processing also yields fast switching speeds.

An on-chip regulator circuit maintains TTL input compatibility over the whole operating supply voltage range, easing control logic interfacing.

Circuit layout is facilitated by the interchangeability of source and drain terminals.

Frequency Response

A single switch on-channel exhibits both resistance ($R_{DS(on)}$) and capacitance ($C_{S(on)}$). This RC combination has an attenuation effect on the analog signal – which is frequency dependent (like an RC low-pass filter). The - 3-dB bandwidth of the DG540 is typically 500 MHz (into 50 Ω). This measured figure of 500 MHz illustrates that the switch channel can not be represented by a two stage RC combination. The on capacitance of the channel is distributed along the on-resistance, and hence becomes a more complex multi stage network of R's and C's making up the total $R_{DS(on)}$ and $C_{S(on)}$. See Application Note AN502 for more details.

Off-Isolation and Crosstalk

Off-isolation and crosstalk are affected by the load resistance and parasitic inter-electrode capacitances. Higher off-isolation is achieved with lower values of R_L. However, low values of R_L increase insertion loss requiring gain adjustments down the line. Stray capacitances, even a fraction of 1 pF, can cause a large crosstalk increase. Good layout and ground shielding techniques can considerably improve your ac circuit performance.

APPLICATIONS

Power Supplies

A useful feature of the DG54X family is its power supply flexibility. It can be operated from a single positive supply (V+) if required (V- connected to ground).
Note that the analog signal must not exceed V- by more than - 0.3 V to prevent forward biasing the substrate p-n junction. The use of a V- supply has a number of advantages:

1. It allows flexibility in analog signal handling, i.e., with V- = - 5 V and V+ = 12 V; up to ± 5 V ac signals can be controlled.

2. The value of on capacitance [$C_{S(on)}$] may be reduced. A property known as 'the body-effect' on the DMOS switch devices causes various parametric effects to occur. One of these effects is the reduction in $C_{S(on)}$ for an increasing V body-source. Note, however, that to increase V- normally requires V+ to be reduced (since V+ to V- = 21 V max.). Reduction in V+ causes an increase in $R_{DS(on)}$, hence a compromise has to be achieved. It is also useful to note that optimum video linearity performance (e.g., differential phase and gain) occurs when V- is around - 3 V.

3. V- eliminates the need to bias the analog signal using potential dividers and large coupling capacitors.

Decoupling

It is an established RF design practice to incorporate sufficient bypass capacitors in the circuit to decouple the power supplies to all active devices in the circuit. The dynamic performance of the DG54X is adversely affected by poor decoupling of power supply pins. Also, of even more significance, since the substrate of the device is connected to the negative supply, adequate decoupling of this pin is essential.

Rules:

1. Decoupling capacitors should be incorporated on all power supply pins (V+, V-). (See Figure 7.)

2. They should be mounted as close as possible to the device pins.

3. Capacitors should have good high frequency characteristics - tantalum bead and/or monolithic ceramic types are adequate.
Suitable decoupling capacitors are 1- to 10 µF tantalum bead, plus 10- to 100 nF ceramic.

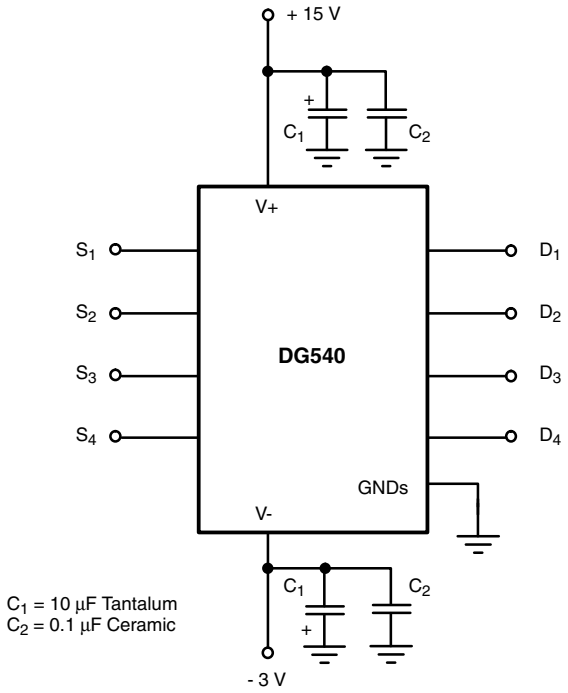


Figure 7. Supply Decoupling

Board Layout

PCB layout rules for good high frequency performance must be observed to achieve the performance boasted by the DG540. Some tips for minimizing stray effects are:

1. Use extensive ground planes on double sided PCB, separating adjacent signal paths. Multilayer PCB is even better.

2. Keep signal paths as short as practically possible, with all channel paths of near equal length.

3. Careful arrangement of ground connections is also very important. Star connected system grounds eliminate signal current flowing through ground path parasitic resistance from coupling between channels.

APPLICATIONS

Figure 8 shows a 4 Channel video multiplexer using a DG540.

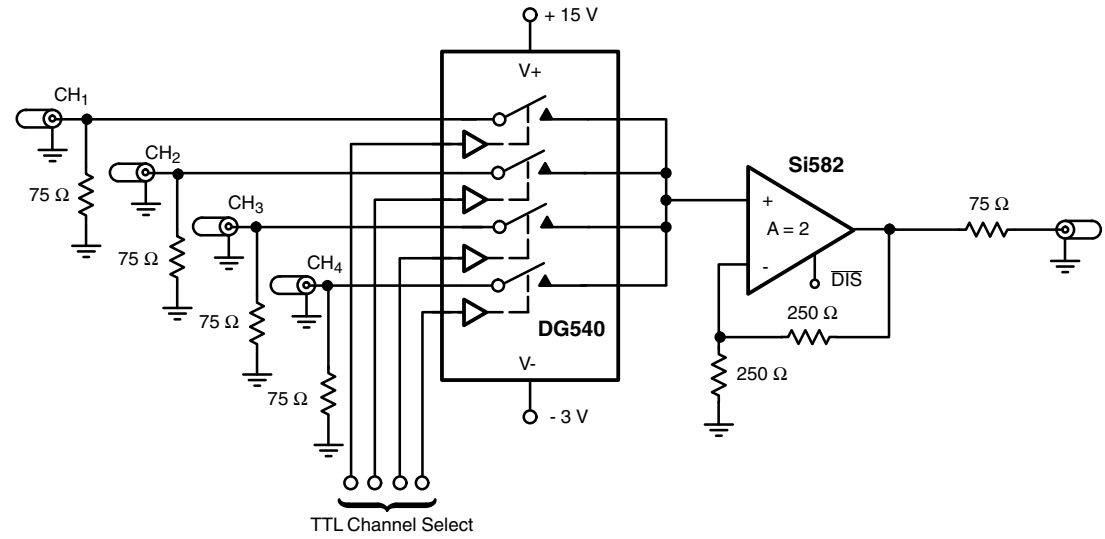


Figure 8. 4 by 1 Video Multiplexing Using the DG540

Figure 9 shows an RGB selector switch using two DG542s.

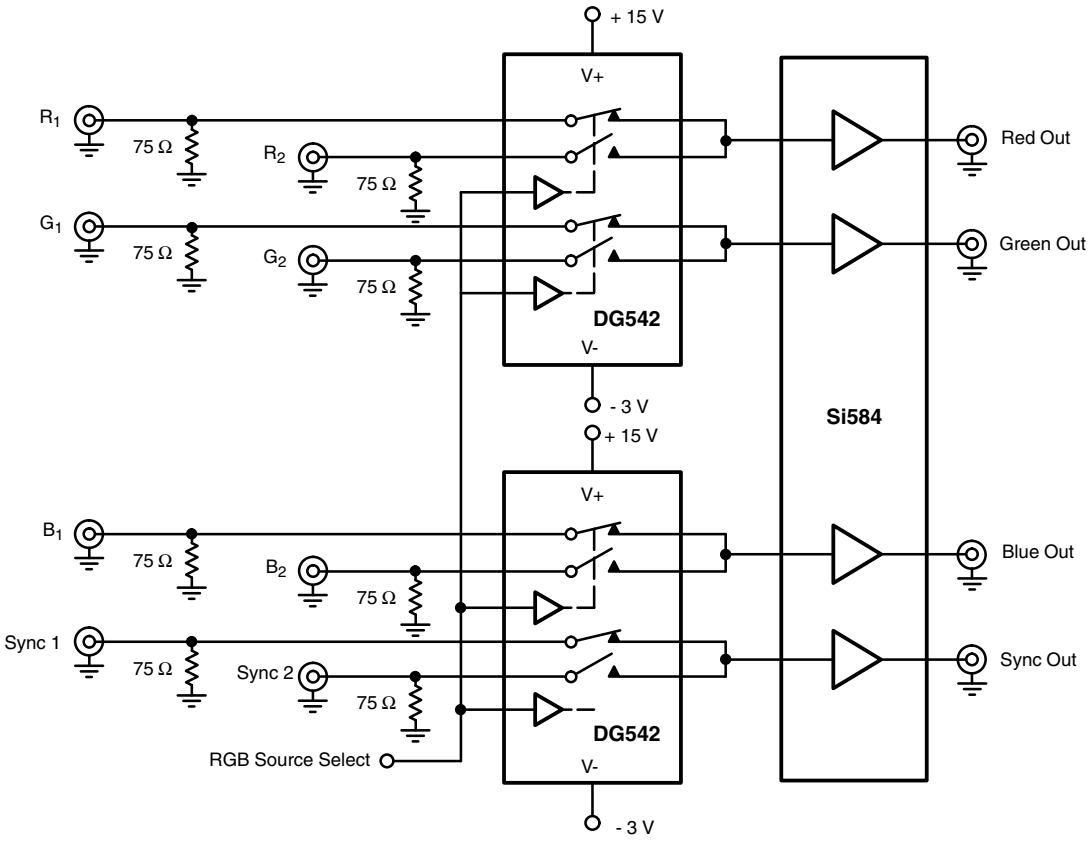


Figure 9. RGB Selector Using Two DG542s

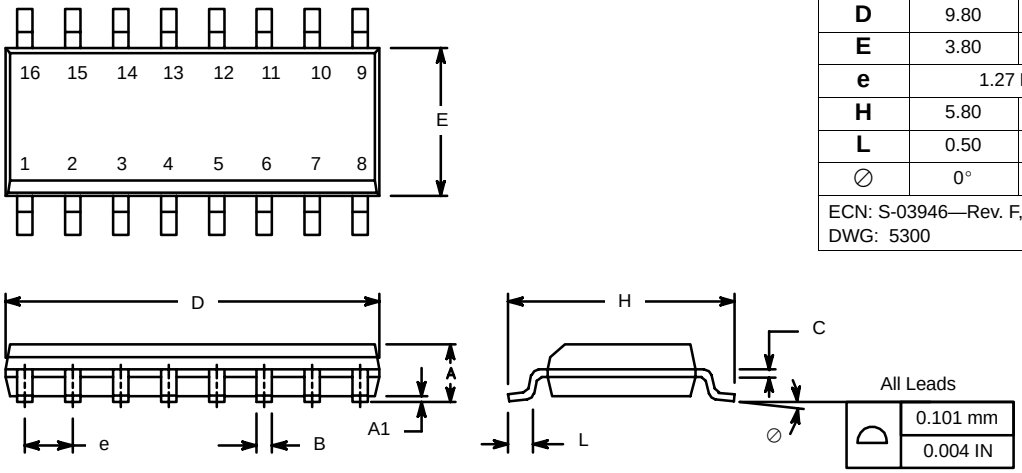
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?70055.

SOIC (NARROW): 16-LEAD

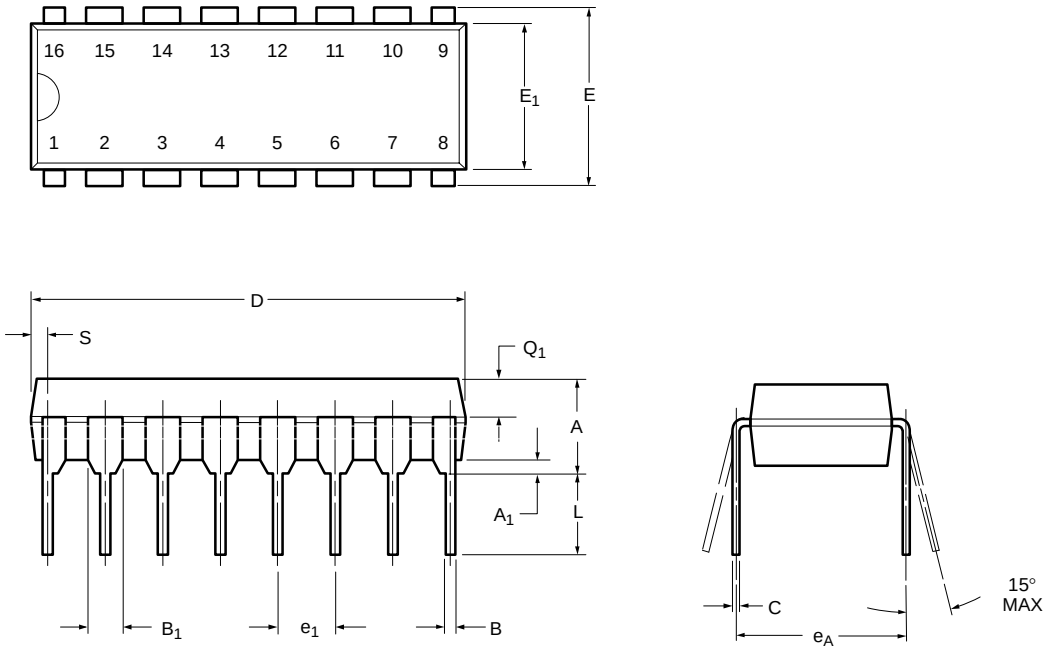
JEDEC Part Number: MS-012

Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.38	0.51	0.015	0.020
C	0.18	0.23	0.007	0.009
D	9.80	10.00	0.385	0.393
E	3.80	4.00	0.149	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.50	0.93	0.020	0.037
⊘	0°	8°	0°	8°

ECN: S-03946—Rev. F, 09-Jul-01
DWG: 5300

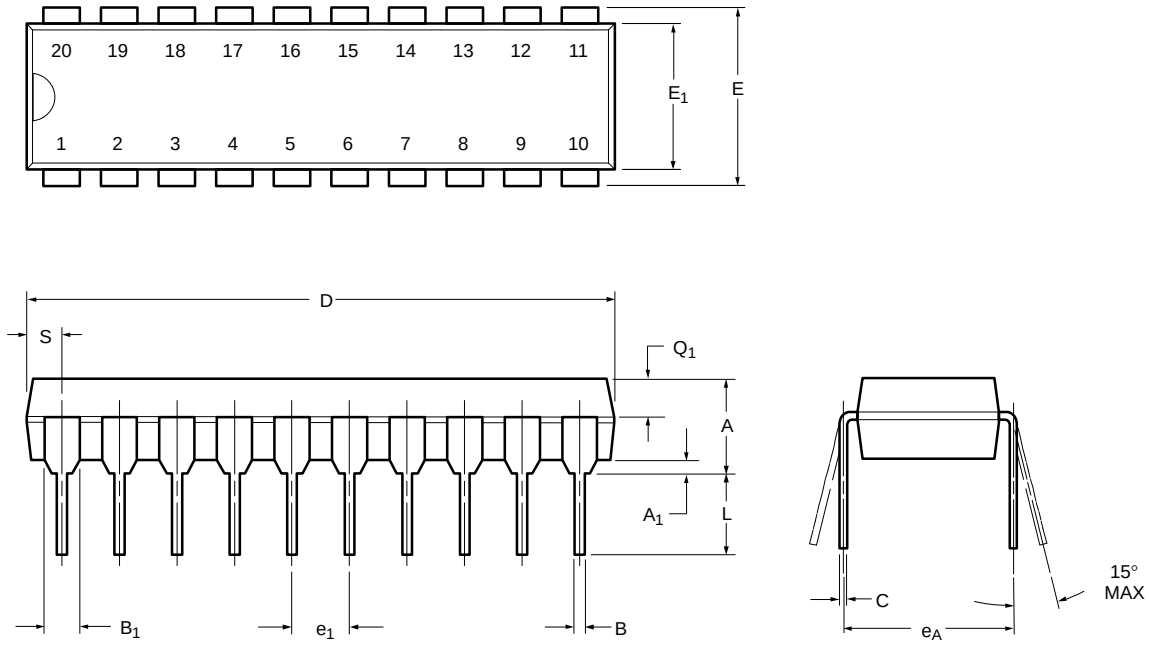


PDIP: 16-LEAD



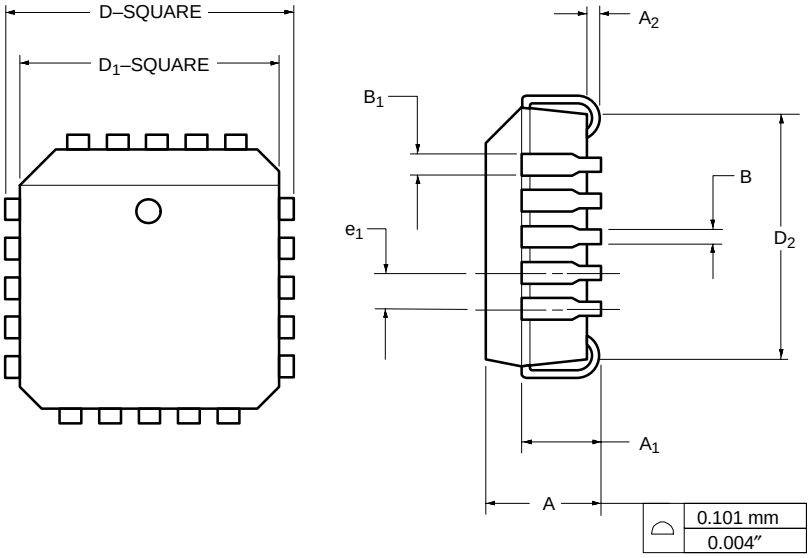
Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	3.81	5.08	0.150	0.200
A_1	0.38	1.27	0.015	0.050
B	0.38	0.51	0.015	0.020
B_1	0.89	1.65	0.035	0.065
C	0.20	0.30	0.008	0.012
D	18.93	21.33	0.745	0.840
E	7.62	8.26	0.300	0.325
E_1	5.59	7.11	0.220	0.280
e_1	2.29	2.79	0.090	0.110
e_A	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
Q_1	1.27	2.03	0.050	0.080
S	0.38	1.52	.015	0.060
ECN: S-03946—Rev. D, 09-Jul-01 DWG: 5482				

PDIP: 20-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	3.81	5.08	0.150	0.200
A_1	0.38	1.27	0.015	0.050
B	0.38	0.51	0.015	0.020
B_1	0.89	1.65	0.035	0.065
C	0.20	0.30	0.008	0.012
D	24.89	26.92	0.980	1.060
E	7.62	8.26	0.300	0.325
E_1	5.59	7.11	0.220	0.280
e_1	2.29	2.79	0.090	0.110
e_A	7.37	7.87	0.290	0.310
L	3.175	3.81	0.123	0.150
Q_1	1.27	2.03	0.050	0.080
S	1.02	2.03	0.040	0.080
ECN: S-03946—Rev. B, 09-Jul-01 DWG: 5484				

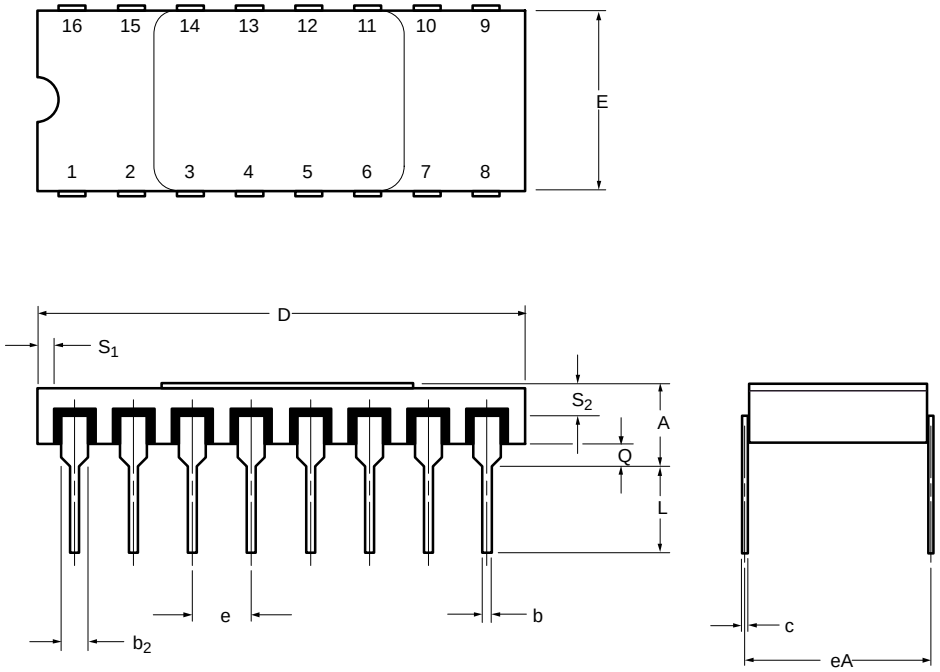
PLCC: 20-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	4.20	4.57	0.165	0.180
A_1	2.29	3.04	0.090	0.120
A_2	0.51	–	0.020	–
B	0.331	0.553	0.013	0.021
B_1	0.661	0.812	0.026	0.032
D	9.78	10.03	0.385	0.395
D_1	8.890	9.042	0.350	0.356
D_2	7.37	8.38	0.290	0.330
e_1	1.27 BSC		0.050 BSC	

ECN: S-03946—Rev. C, 09-Jul-01
DWG: 5306

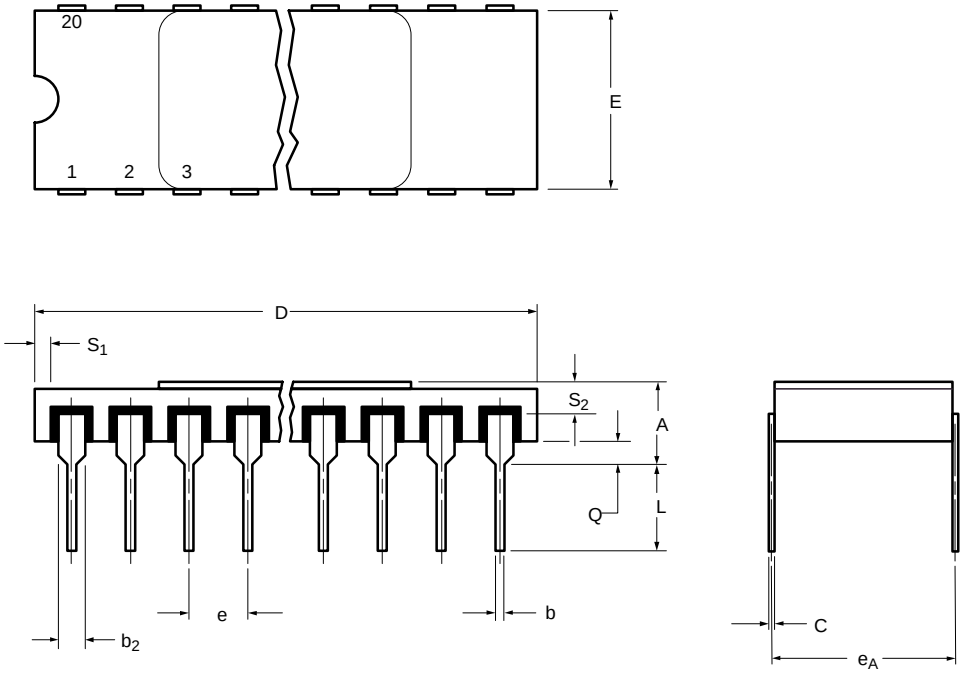
SIDEBRAZE: 16-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	2.67	4.45	0.105	0.175
b	0.38	0.53	0.015	0.021
b_2	1.14	1.65	0.045	0.065
c	0.20	0.30	0.008	0.012
D	19.56	21.08	0.770	0.830
E	7.11	7.87	0.280	0.310
e	2.54 BSC		0.100 BSC	
e_A	7.62 BSC		0.300 BSC	
L	3.18	4.45	0.125	0.175
Q	0.64	1.40	0.025	0.055
S_2	0.25	–	0.010	–
S_1	0.13	–	0.005	–
ECN: S-03946—Rev. G, 09-Jul-01 DWG: 5418				

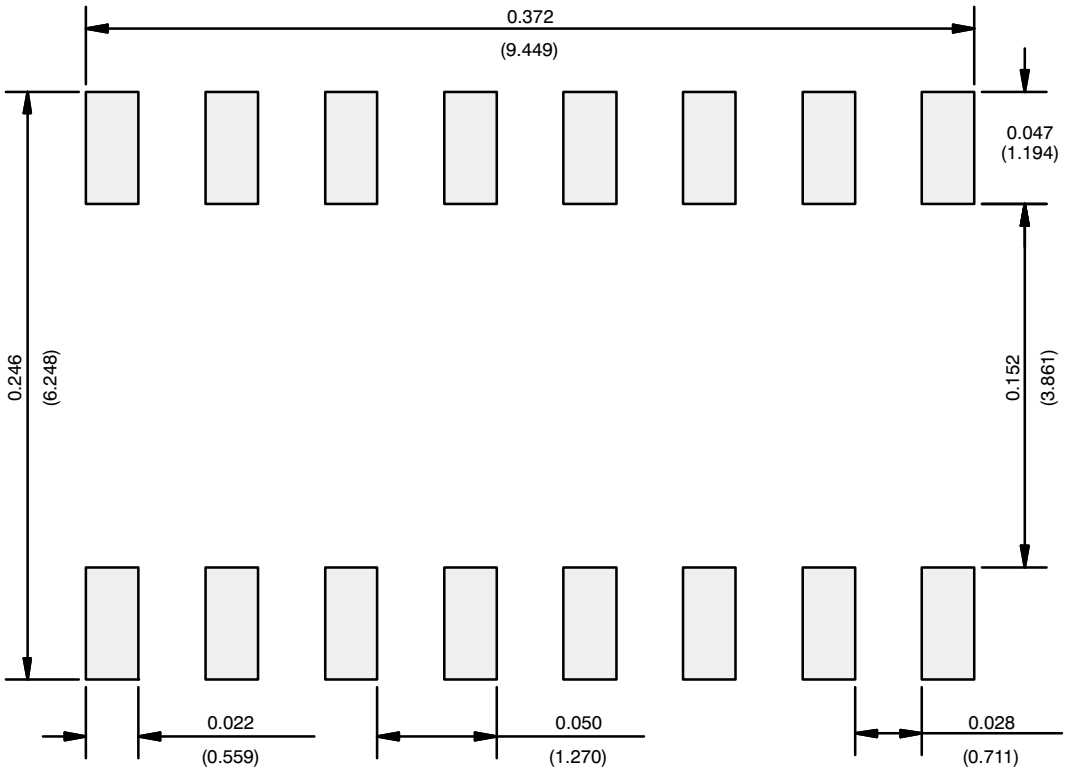
SIDEBRAZE: 20-LEAD

Meets MIL-STD-1835, D8, Configuration C



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	2.67	4.45	0.105	0.175
b	0.38	0.53	0.015	0.021
b_2	1.14	1.65	0.045	0.065
c	0.20	0.30	0.008	0.012
D	24.89	26.16	0.980	1.030
E	7.11	7.87	0.280	0.310
e	2.54 BSC		0.100 BSC	
e_A	7.62 BSC		0.300 BSC	
L	3.18	4.45	0.125	0.175
Q	0.64	1.40	0.025	0.055
S_2	0.25	–	0.010	–
S_1	0.13	–	0.005	–
ECN: S-03946—Rev. D, 09-Jul-01 DWG: 5309				

RECOMMENDED MINIMUM PADS FOR SO-16



Recommended Minimum Pads
Dimensions in Inches/(mm)

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