ABSOLUTE MAXIMUM RATINGS			
PARAMETER	**SYMBOL**	**LIMIT**	**UNIT**
Terminal Voltage (with respect to GND)	V_{CC}	GND - 0.3 to GND +6.5	V
RESET low output voltage	V_{RESET}	GND - 0.3 to V_{CC} +0.3	V
Input Current, V_{CC}	I_{CC}	20	mA
RESET Output Current	I_O	5	mA
Power Dissipation	P_D	$(T_J-T_A)/R_{\theta JA}$	mW
Operating Junction Temperature Range	$T_{J.OPR}$	-40 ~ +125	°C
Storage Temperature Range	T_{STG}	-65 ~ +150	°C
Lead Soldering Temperature (260°C)	t_{LEAD}	10	s

THERMAL PERFORMANCE			
PARAMETER	**SYMBOL**	**MAXIMUM**	**UNIT**
Thermal Resistance from Junction to Case	$R_{\theta JC}$	110	°C/W
Thermal Resistance from Junction to Ambient (Note 1)	$R_{\theta JA}$	250	°C/W

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C unless otherwise noted)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Input Supply Voltage	T_A=-40°C~+85°C	V_{CC}	1.0	--	6	V
Supply Current	$V_{CC}=V_{TH}$ + 1V	I_{CC}	--	25	35	µA
Reset Threshold	TS3809CXD	V_{TH}	3.02	3.08	3.15	V
	TS3809CXE		2.87	2.93	3.00	
	TS3809CXF		2.57	2.63	2.69	
Reset Threshold Temperature Coefficient	T_A=0~+85°C	V_{THT}	--	50	--	ppm/°C
Set-up Time	V_{CC} = 0 ~ (V_{TH} - 100mV)	t_{SET}	1	--	--	µs
V_{CC} to Reset Delay	V_{CC} = V_{TH} ~ (V_{TH} - 100mV)	t_{RD}	--	20	--	µs
Reset Active Timeout Period	T_A=0~+85°C	t_{DELAY}	140	200	260	ms
RESET Output Voltage Low	1.8V<V_{CC}<$V_{TH(MAX)}$, I_{SINK} =1.2mA	V_{OL}	--	--	0.3	V
	1.2V<V_{CC}<1.8V, I_{SINK} =50µA					
RESET Output Voltage High	V_{CC} > $V_{TH(MAX)}$, I_{SOURCE} =500µA	V_{OH}	0.8 V_{CC}	--	--	V
Hysteresis at V_{CC}	Input Voltage	V_{HVS}	--	40	--	mV

Note :

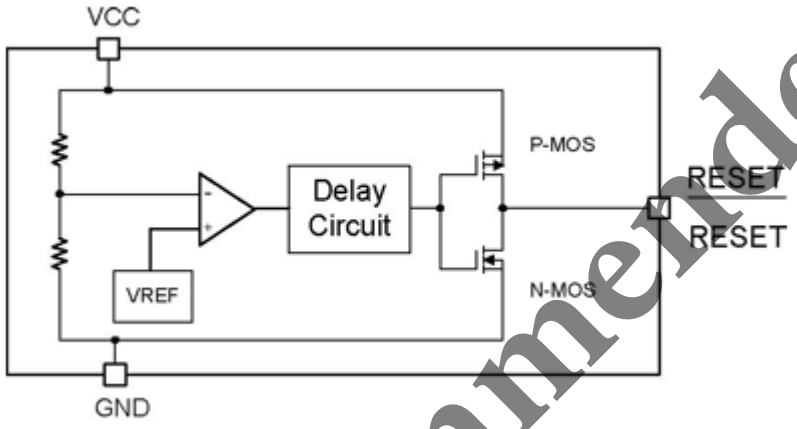
1. $R_{\theta JA}$ is measured the PCB copper area of approximately 1in^2 (Multi-layer). Needs to connect to V_{SS} pin.

Not Recommended

ORDERING INFORMATION

RESET VOLTAGE	PART NO.	PACKAGE	PACKING
3.08V	TS3809CXD RFG	SOT-23	3,000pcs / 7” Reel
2.93V	TS3809CXE RFG	SOT-23	3,000pcs / 7” Reel
2.63V	TS3809CXF RFG	SOT-23	3,000pcs / 7” Reel

BLOCK DIAGRAM



Not Recommended

CHARACTERISTICS CURVES

(T_C = 25°C unless otherwise noted)

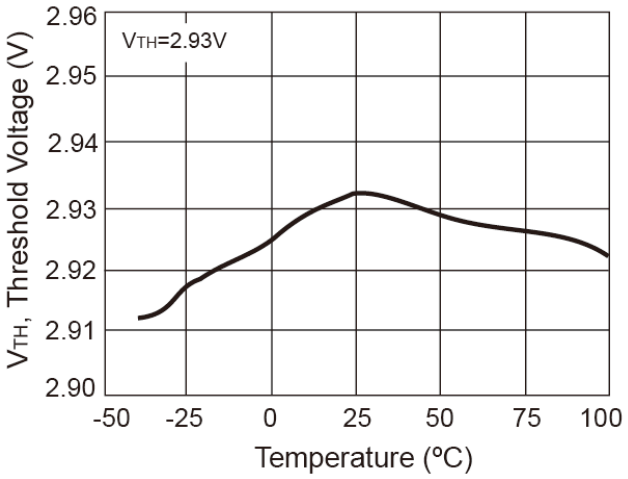


Figure 1. Threshold Voltage vs. Temperature

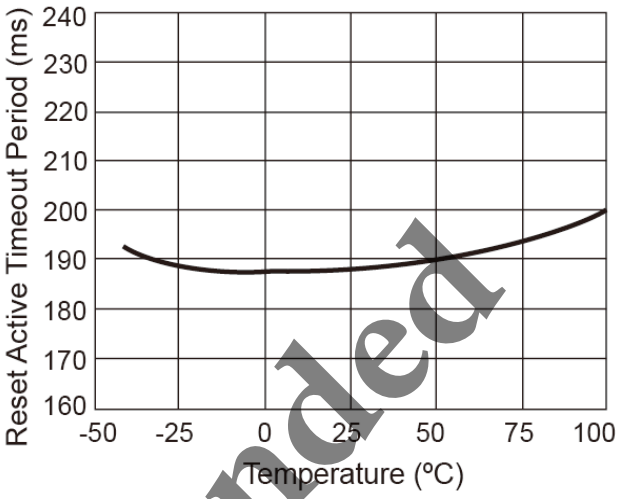


Figure 2. T_{DELAY} vs. Temperature

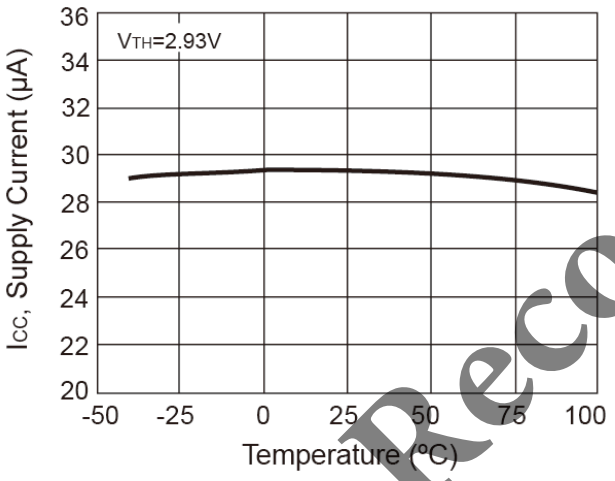


Figure 3. Supply Current vs. Temperature

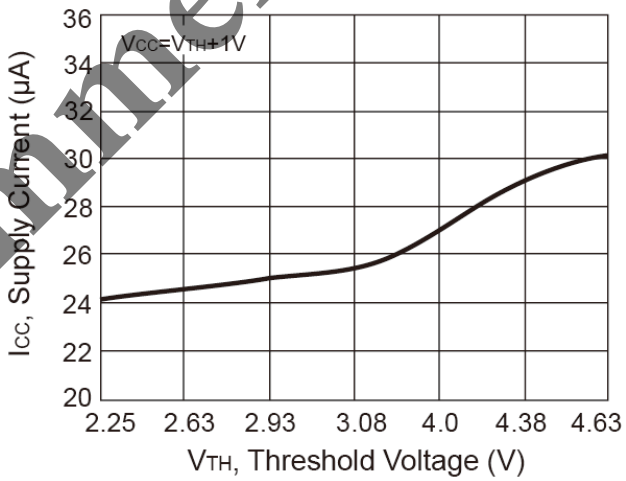


Figure 4. Supply Current vs. Threshold Voltage

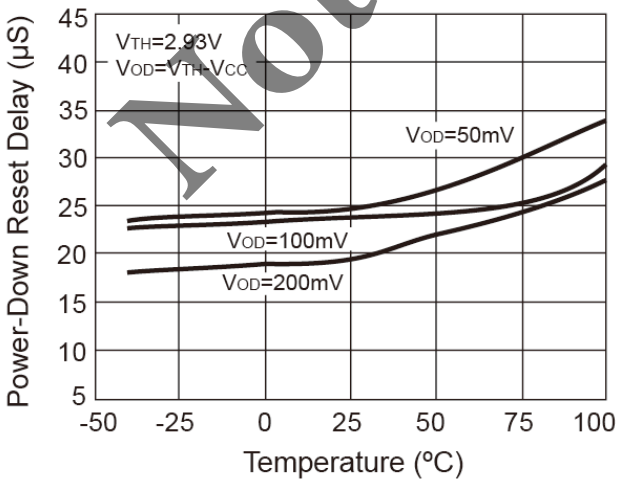


Figure 5. Power-Down T_{DELAY} vs. Temperature

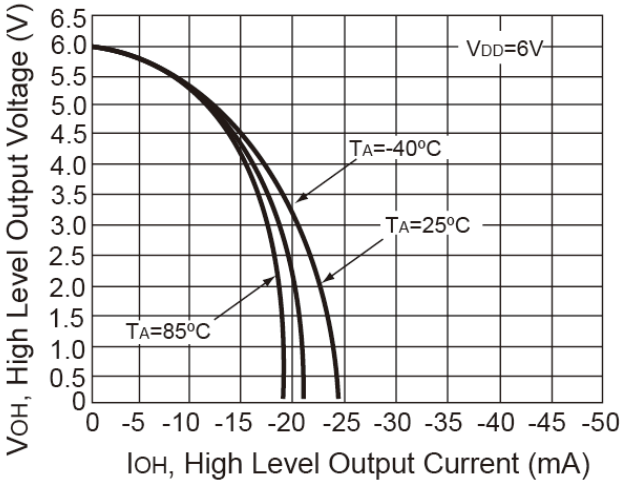


Figure 6. Output Voltage vs. Output Current

Not Recommended

APPLICATION INFORMATION

Negative-Going V_{CC} transients in addition to issuing a reset to the µP during power-up, power-down, and brownout conditions, the TS3809 are relatively immune to short-duration negative-going V_{CC} transients (glitches).
The TS3809/3810 does not generate a reset pulse. The graph was generated using a negative going pulse applied to V_{CC}, starting 0.5V above the actual reset threshold and ending below it by the magnitude indicated (reset comparator overdrive). The graph indicates the maximum pulse width a negative going V_{CC} transient can have without causing a reset pulse. As the magnitude of the transient increases (goes farther below the reset threshold), the maximum allowable pulse width decreases. Typically, a V_{CC} transient that goes 100mV below the reset threshold and lasts 20µS or less will not cause a reset pulse. A 0.1µF bypass capacitor mounted as close as possible to the V_{CC} pin provides additional transient immunity.

FUNCTION DESCRIPTION

A microprocessor's reset input starts the µP in a known state. The TS3809 assert reset to prevent code-execution errors during power-up, power-down, or brownout conditions. They assert a reset signal whenever the V_{CC} supply voltage declines below a preset threshold, keeping it asserted for at least 140ms after V_{CC} has risen above the reset threshold. The TS3809 have a push-pull output stage.

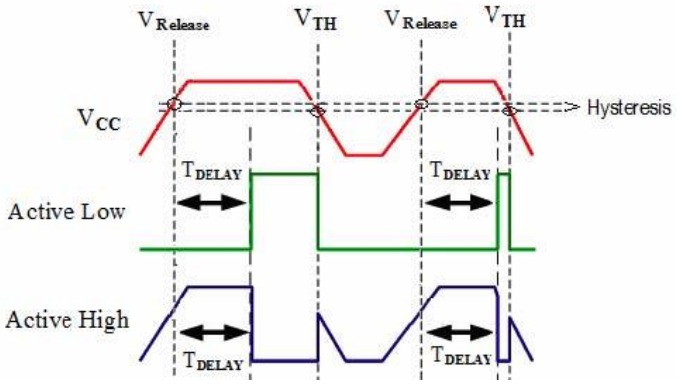
ENSURING A VALID RESET OUTPUT DOWN TO V_{CC}=0

RESET is guaranteed to be a logic low for V_{CC} > 1.0V. Once V_{CC} exceeds the reset threshold, an internal timer keeps RESET low for the reset timeout period; after this interval, RESET goes high. If a brownout condition occurs (V_{CC} dips below the reset threshold), RESET goes low. Any time V_{CC} goes below the reset threshold, the internal timer resets to zero, and RESET goes low. The internal timer starts after V_{CC} returns above the reset threshold, and RESET remains low for the reset timeout period. When V_{CC} falls below 1V, the TS3809 reset output no longer sinks current - it becomes an open circuit. Therefore, high impedance CMOS logic input connected to reset can drift to undetermined voltages. This present no problem in most applications since most µP and other circuitry is inoperative with V_{CC} below 1V.However, in applications where reset must be valid down to 0V, adding a pull down resistor to reset causes and stray leakage currents to flow to ground, holding reset low (Figure 2.) R1's value is not critical; 100K is large enough not to load reset and small enough to pull RESET to ground. For the TS3809 if reset is required to remain valid for V_{CC} <1V.

BENEFITS OF HIGHLY ACCURATE RESET THRESHOLD

Most µP supervisor ICs has reset threshold voltages between 5% and 10% below the value of nominal supply voltages. This ensures a reset will not occur within 5% of the nominal supply, but will occur when the supply is 10% below nominal. When using ICs rated at only the nominal supply ±5%, this leaves a zone of uncertainty where the supply is between 5% and 10% low, and where the reset many or may not be asserted.

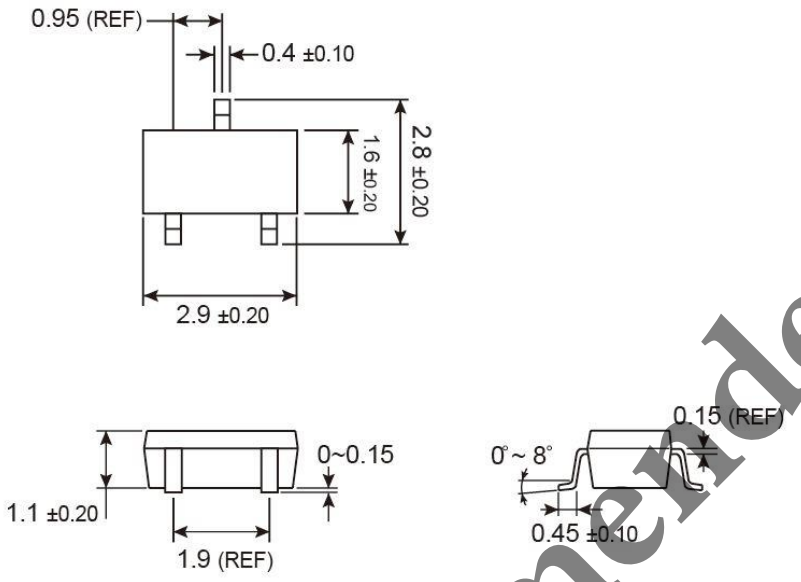
TIMMING DIAGRAM



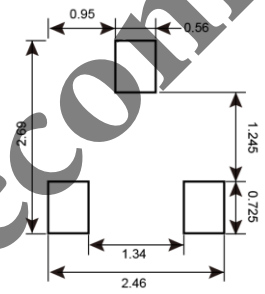
Not Recommended

PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

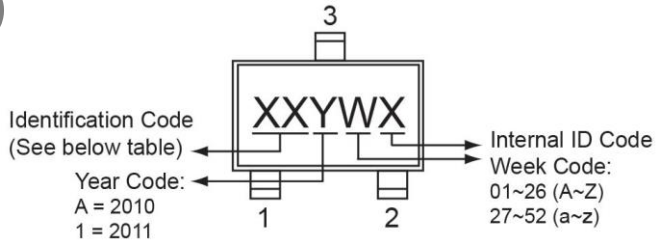
SOT-23



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



PART NO.	IDENTIFICATION CODE
TS3809CXD	CD
TS3809CXE	CE
TS3809CXF	CF

Not Recommended

Not Recommended

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