

# Quad Equalized 1.5/3.0/6.0GT/s SAS/SATA Redriver

## ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND.)

V <sub>CC</sub> .....	-0.3V to +4.0V
All Other Pins.....	-0.3V to (V <sub>CC</sub> + 0.3V)
Continuous Current (PE <sub>-</sub> , EQ <sub>-</sub> , MODE <sub>-</sub> ).....	±15mA
Peak Current (for 10kHz, 1% duty cycle) (IN <sub>-</sub> , OUT <sub>-</sub> ).....	±100mA
Continuous Power Dissipation (T <sub>A</sub> = +70°C) 42-Pin TQFN (derate 35.7mW/°C above +70°C).....	2857mW

Junction-to-Case Thermal Resistance (θ<sub>JC</sub>) (Note 1)

42-Pin TQFN.....2°C/W

Junction-to-Ambient Thermal Resistance (θ<sub>JA</sub>) (Note 1)

42-Pin TQFN.....28°C/W

Operating Temperature Range.....0°C to +70°C

Storage Temperature Range.....-55°C to +150°C

Junction Temperature.....+150°C

Lead Temperature (soldering, 10s).....+300°C

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations refer to [www.maxim-ic.com/thermal-tutorial](http://www.maxim-ic.com/thermal-tutorial).

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub> = +3.0V to +3.6V, C<sub>COUPLE</sub> = 12nF, R<sub>L</sub> = 50Ω, T<sub>A</sub> = 0°C to +70°C, unless otherwise noted. Typical values are at V<sub>CC</sub> = +3.3V, T<sub>A</sub> = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Power-Supply Range	V <sub>CC</sub>		3.0		3.6	V
Operating Supply Current	I <sub>CC</sub>	EQ <sub>-</sub> = PE <sub>-</sub> = GND		280	350	mA
		EQ <sub>-</sub> = PE <sub>-</sub> = V <sub>CC</sub>		350	440	
Standby Supply Current	I <sub>STBY</sub>	EN <sub>-</sub> = GND		32	40	mA
Input Termination	R <sub>RX-SE</sub>	Single-ended to V <sub>CC</sub>	42.5		57.5	Ω
Output Termination	R <sub>TX-SE</sub>	Single-ended to V <sub>CC</sub>	42.5		57.5	Ω
<b>AC PERFORMANCE</b>						
Differential Input Return Loss (Note 3)	S <sub>DD11</sub>	0.1GHz ≤ f ≤ 0.3GHz	-10			dB
		0.3GHz ≤ f ≤ 3.0GHz	-7.9			
		3.0GHz ≤ f ≤ 6.0GHz	0			
Common-Mode Input Return Loss (Note 3)	S <sub>CC11</sub>	0.1GHz ≤ f ≤ 0.3GHz	-6			dB
		0.3GHz ≤ f ≤ 3.0GHz	-5			
		3.0GHz ≤ f ≤ 6.0GHz	0			
Differential Output Return Loss (Note 3)	S <sub>DD22</sub>	0.1GHz ≤ f ≤ 0.3GHz	-10			dB
		0.3GHz ≤ f ≤ 3.0GHz	-7.9			
		3.0GHz ≤ f ≤ 6.0GHz	0			
Common-Mode Output Return Loss (Note 3)	S <sub>CC22</sub>	0.1GHz ≤ f ≤ 0.3GHz	-6			dB
		0.3GHz ≤ f ≤ 3.0GHz	-5			
		3.0GHz ≤ f ≤ 6.0GHz	0			
Differential Input Voltage	V <sub>IN-DIFF</sub>	SAS 1.5, 3.0, or 6.0GT/s, MODE <sub>-</sub> = GND	275		1600	mV <sub>P-P</sub>
		SATA 1.5, 3.0, or 6.0GT/s, MODE <sub>-</sub> = V <sub>CC</sub>	225		1600	
Input Equalization	EQ	EQ <sub>-</sub> = V <sub>CC</sub> (Note 4)		3		dB
Differential Output Voltage	V <sub>OUT-DIFF</sub>	f = 750MHz, PE <sub>-</sub> = GND	800		1200	mV <sub>P-P</sub>
Output Preemphasis	PE	PE <sub>-</sub> = V <sub>CC</sub> , Figure 1		3		dB

# Quad Equalized 1.5/3.0/6.0GT/s SAS/SATA Redriver

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## ELECTRICAL CHARACTERISTICS (continued)

(V<sub>CC</sub> = +3.0V to +3.6V, C<sub>COUPLE</sub> = 12nF, R<sub>L</sub> = 50Ω, T<sub>A</sub> = 0°C to +70°C, unless otherwise noted. Typical values are at V<sub>CC</sub> = +3.3V, T<sub>A</sub> = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay	t <sub>PD</sub>	PE <sub>-</sub> = EQ <sub>-</sub> = GND		300		ps
Output Transition Time	T <sub>TX-RF</sub>	PE <sub>-</sub> = GND, 20% to 80%	40			ps
Differential Output Skew Same Pair	T <sub>SK</sub>			10		ps
Deterministic Jitter	T <sub>DJ</sub>	K28.5 pattern, 6.0GT/s, PE <sub>-</sub> = EQ <sub>-</sub> = GND (Note 3)			20	psp-p
Random Jitter	T <sub>RJ</sub>	D10.2 pattern, 6.0GT/s, PE <sub>-</sub> = EQ <sub>-</sub> = GND			1.8	psRMS
OOB Squelch Threshold	V <sub>SQ-DIFF</sub>	MODE <sub>-</sub> = GND, f = 0.75GHz	120		220	mVp-p
		MODE <sub>-</sub> = V <sub>CC</sub> , f = 0.75GHz	50		150	
OOB Squelch Entry Time	T <sub>OOB,SQ</sub>	f = 0.75GHz (Note 3)			5	ns
OOB Exit Time	T <sub>OOB,EX</sub>	f = 0.75GHz (Note 3)			9	ns
OOB Differential Offset Delta	ΔV <sub>OOB,DIFF</sub>	Difference between OOB and active-mode output offset	-50		+50	mV
OOB Common-Mode Offset Delta	ΔV <sub>OOB,CM</sub>	Difference between OOB and active-mode output common-mode voltage	-30		+30	mV
OOB Output Disable	V <sub>OOB,OUT</sub>	OOB disabled output level			30	mVp-p
<b>CONTROL LOGIC INPUTS</b>						
Input Logic-High	V <sub>IH</sub>		1.4			V
Input Logic-Low	V <sub>IL</sub>				0.6	V
Input Logic Hysteresis	V <sub>HYST</sub>			75		mV
Input Leakage Current	I <sub>IN</sub>	V <sub>CC</sub> = 3.3V, V <sub>IN</sub> = 0.5V or 1.5V	-50		+50	μA

**Note 2:** All devices are 100% production tested at T<sub>A</sub> = +70°C. All temperature limits are guaranteed by design.

**Note 3:** Guaranteed by design.

**Note 4:** EQ (input equalization) as employed in this device refers to the equivalent of adding preemphasis before the input. For example, input EQ of 3dB would show the same waveform as output PE of 3dB (see Figure 1).

## Timing Diagram

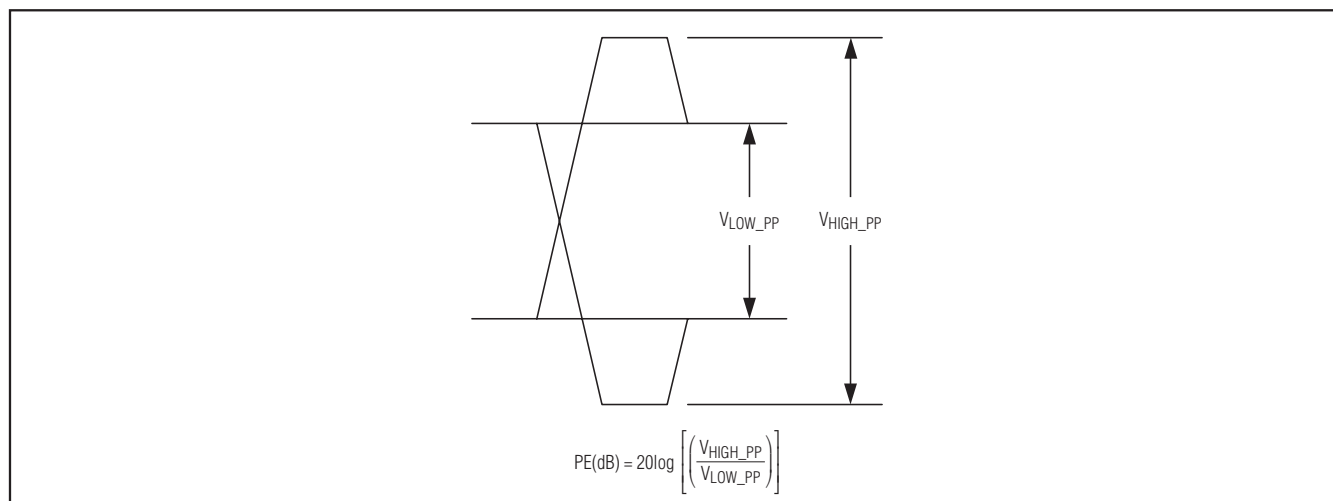
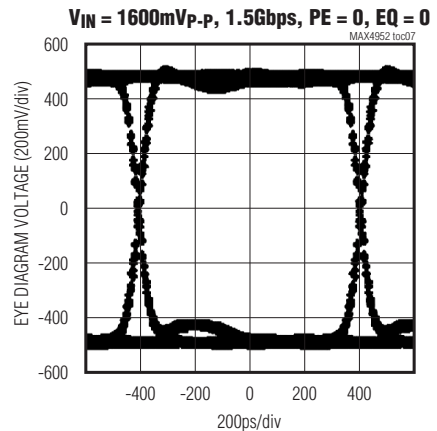
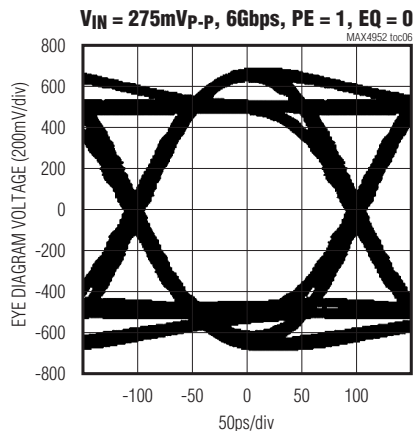
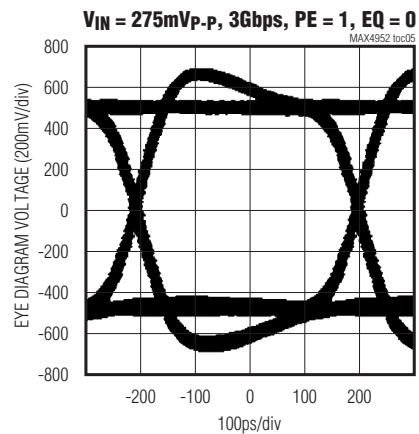
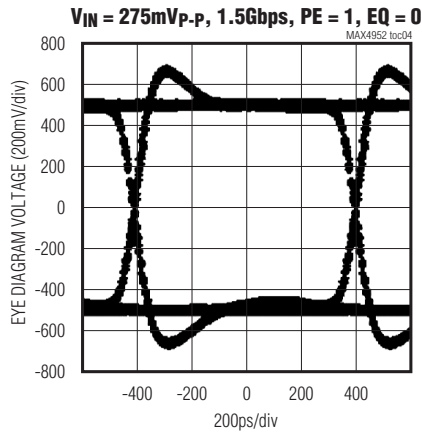
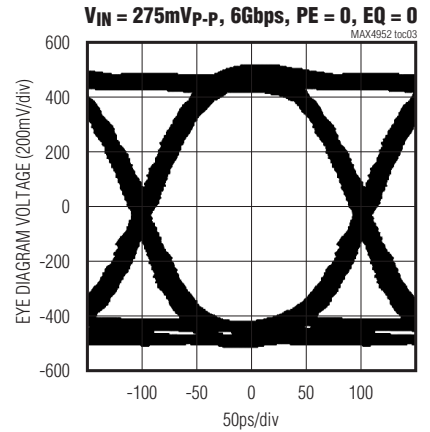
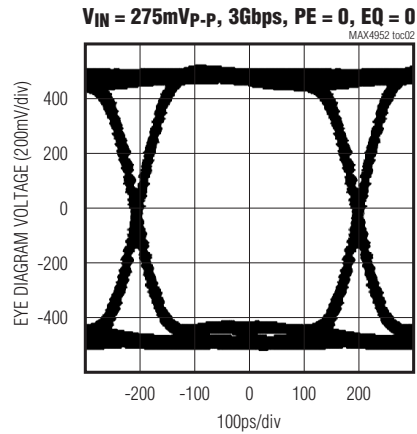
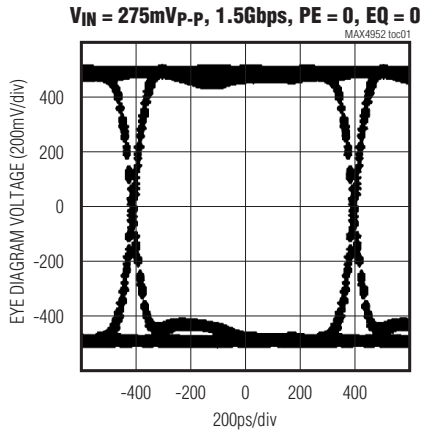


Figure 1. Output Preemphasis

# Quad Equalized 1.5/3.0/6.0GT/s SAS/SATA Redriver

## Typical Operating Characteristics

( $V_{CC} = +3.3V$ ,  $T_A = +25^\circ C$ , all eye diagrams measured using K28.5 pattern.)

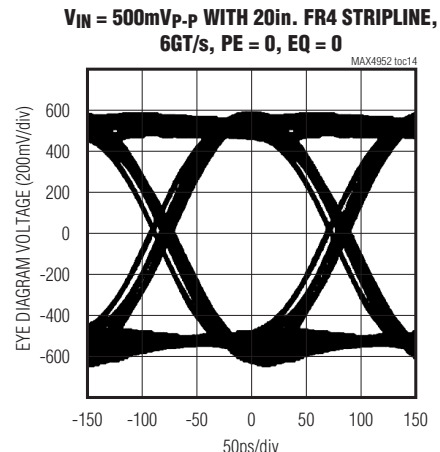
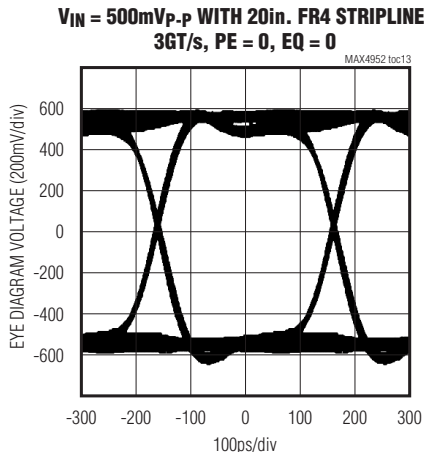
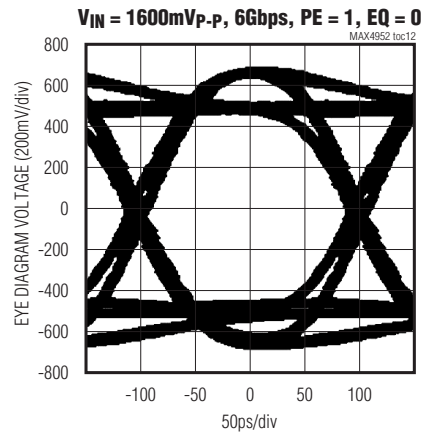
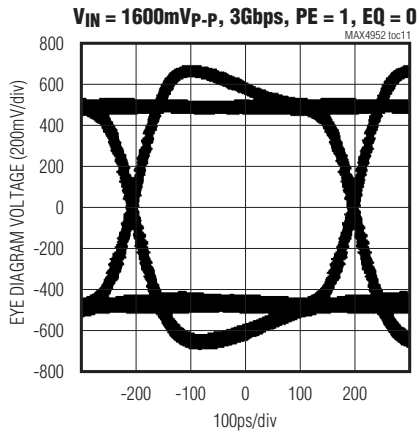
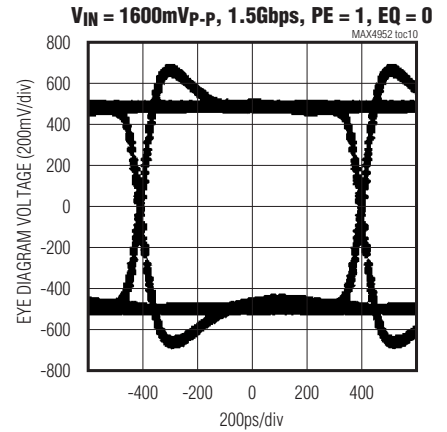
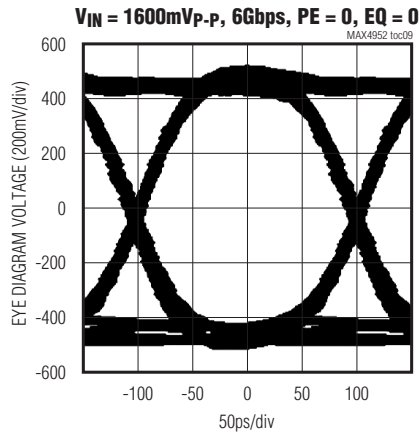
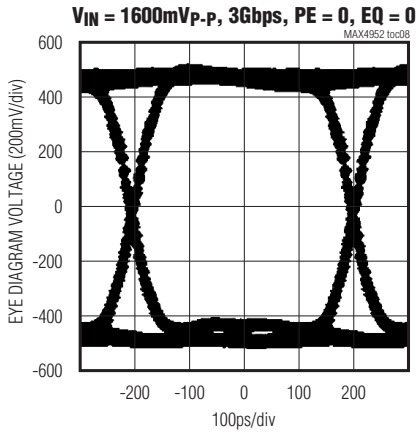


# Quad Equalized 1.5/3.0/6.0GT/s SAS/SATA Redriver

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## Typical Operating Characteristics (continued)

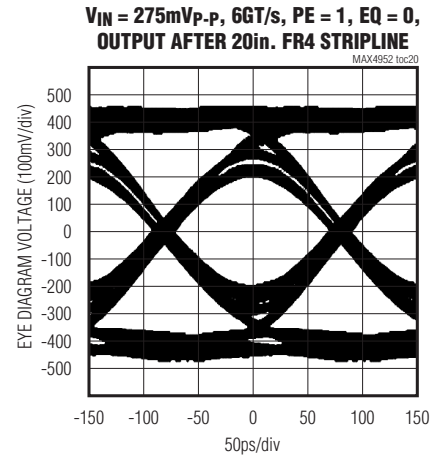
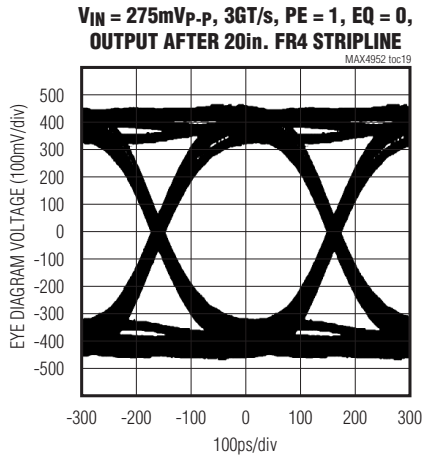
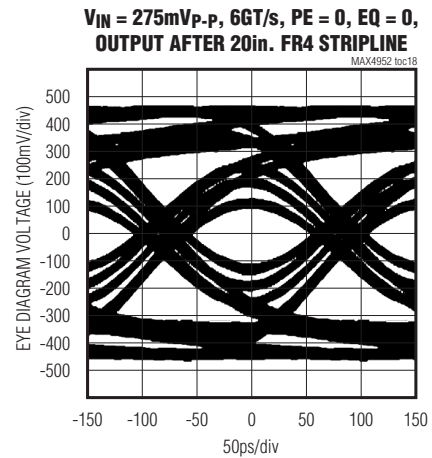
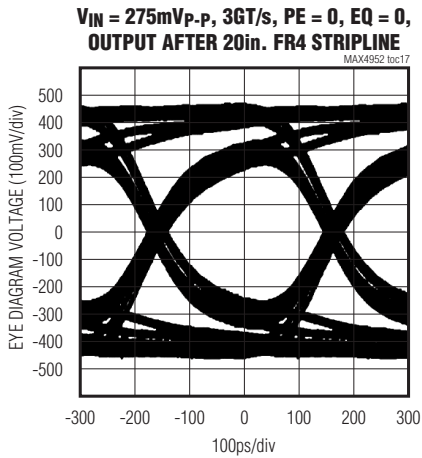
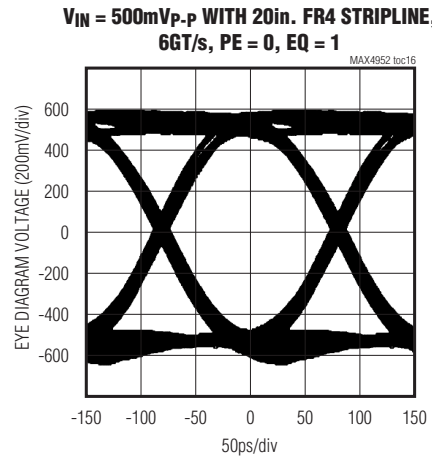
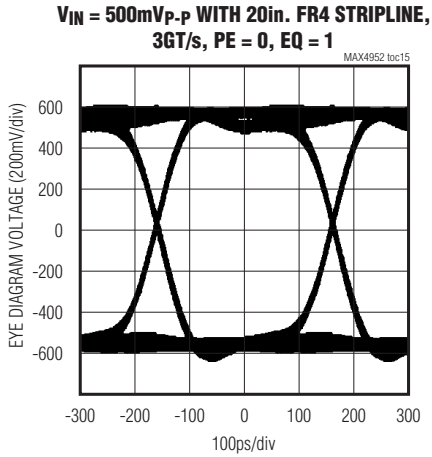
( $V_{CC} = +3.3V$ ,  $T_A = +25^\circ C$ , all eye diagrams measured using K28.5 pattern.)



# Quad Equalized 1.5/3.0/6.0GT/s SAS/SATA Redriver

## Typical Operating Characteristics (continued)

( $V_{CC} = +3.3V$ ,  $T_A = +25^\circ C$ , all eye diagrams measured using K28.5 pattern.)



# Quad Equalized 1.5/3.0/6.0GT/s SAS/SATA Redriver

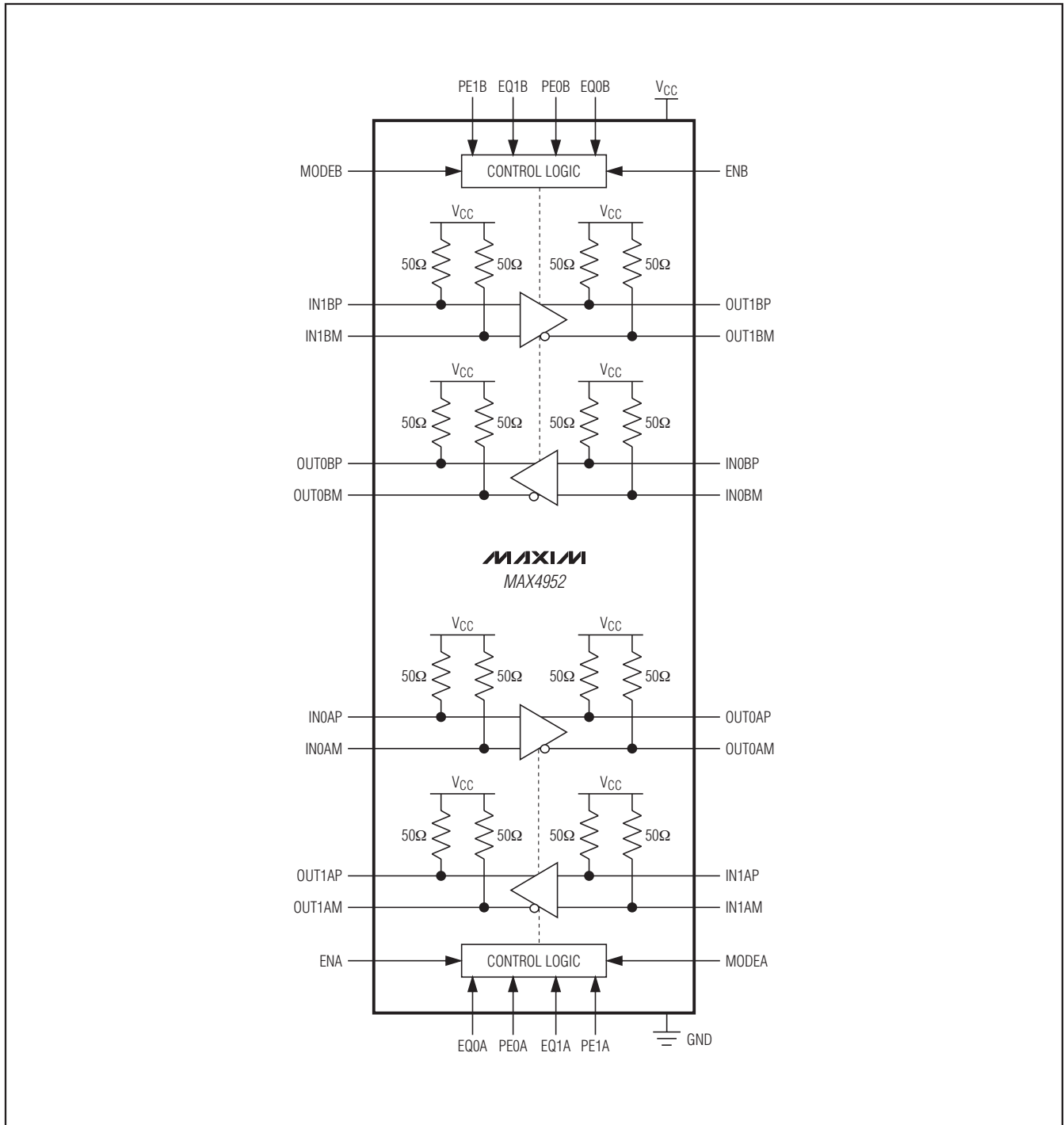
## Pin Description

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PIN	NAME	FUNCTION
1	MODEB	OOB Threshold Logic Input B. MODEB is internally pulled down.
2, 9, 16, 23, 30, 37	V <sub>CC</sub>	Positive Supply Voltage Input. Bypass V <sub>CC</sub> to GND with 2.2μF and 0.01μF capacitors in parallel as close to the device as possible, recommended on each V <sub>CC</sub> pin.
3, 6, 12, 15, 24, 27, 33, 36	GND	Ground
4	IN1BP	Noninverting Input 1B
5	IN1BM	Inverting Input 1B
7	OUT0BP	Noninverting Output 0B
8	OUT0BM	Inverting Output 0B
10	IN0AP	Noninverting Input 0A
11	IN0AM	Inverting Input 0A
13	OUT1AP	Noninverting Output 1A
14	OUT1AM	Inverting Output 1A
17	ENA	Active-High Enable Input A. Drive ENA low to put A channels in standby mode. Drive ENA high to put A channels in normal operation. ENA is internally pulled down.
18	EQ0A	Channel 0A Input Equalizer Logic Input. EQ0A is internally pulled down.
19	PE0A	Channel 0A Output Preemphasis Logic Input. PE0A is internally pulled down.
20	EQ1A	Channel 1A Input Equalizer Logic Input. EQ1A is internally pulled down.
21	PE1A	Channel 1A Output Preemphasis Logic Input. PE1A is internally pulled down.
22	MODEA	OOB Threshold Logic Input A. MODEA is internally pulled down.
25	IN1AM	Inverting Input 1A
26	IN1AP	Noninverting Input 1A
28	OUT0AM	Inverting Output 0A
29	OUT0AP	Noninverting Output 0A
31	IN0BM	Inverting Input 0B
32	IN0BP	Noninverting Input 0B
34	OUT1BM	Inverting Output 1B
35	OUT1BP	Noninverting Output 1B
38	ENB	Active-High Enable Input B. Drive ENB low to put B channels in standby mode. Drive ENB high to put B channels in normal operation. ENB is internally pulled down.
39	EQ0B	Channel 0B Input Equalizer Logic Input. EQ0B is internally pulled down.
40	PE0B	Channel 0B Output Preemphasis Logic Input. PE0B is internally pulled down.
41	EQ1B	Channel 1B Input Equalizer Logic Input. EQ1B is internally pulled down.
42	PE1B	Channel 1B Output Preemphasis Logic Input. PE1B is internally pulled down.
—	EP	Exposed Paddle. Internally connected to GND. EP must be electrically connected to a ground plane for proper thermal and electrical operation. Do not use EP as the sole ground connection.

# Quad Equalized 1.5/3.0/6.0GT/s SAS/SATA Redriver

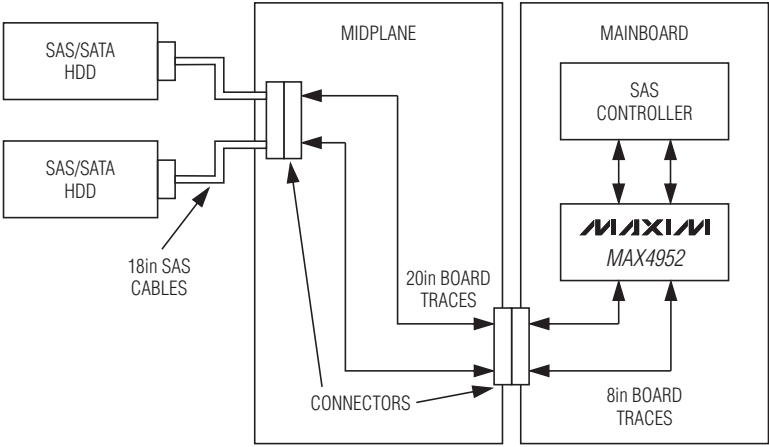
## Functional Diagram



# Quad Equalized 1.5/3.0/6.0GT/s SAS/SATA Redriver

## Typical Application Circuit

**MAX4952**





# Quad Equalized 1.5/3.0/6.0GT/s SAS/SATA Redriver

## Detailed Description

The MAX4952 consists of four identical redrivers with input equalization and output preemphasis useful for SAS or SATA signals up to 6.0GT/s.

### Input/Output Terminations

Inputs and outputs are internally 50Ω terminated to V<sub>CC</sub> (see the *Functional Diagram*) and must be AC-coupled using 12nF (max) capacitors to the SAS/SATA controller IC and SAS/SATA device for proper operation.

### Enable Inputs (ENA, ENB)

The MAX4952 features two active-high enable inputs (ENA, ENB). ENA and ENB have internal pulldown resistors of 70kΩ (typ). When ENA or ENB is driven low or left unconnected, the A or B channels enter low-power standby mode and the redrivers are disabled.

Drive ENA or ENB high to place channel A or B in normal operation (see Table 1).

### Out-of-Band Threshold Selector (MODEA, MODEB)

The MAX4952 provides full OOB signal support through high-speed amplitude detection circuitry. OOB differential input signals less than the internal OOB threshold (V<sub>SQ-DIFF</sub>) are detected as OFF and not passed to the output. This prevents the system from responding to unwanted noise. OOB differential input signals higher than V<sub>SQ-DIFF</sub> are detected as ON and passed to the output, allowing OOB signals to transmit through the MAX4952. The logic level of the MODE inputs sets V<sub>SQ-DIFF</sub> for either SAS or SATA OOB signals (see Table 2). MODEA and MODEB have internal pulldown resistors of 70kΩ (typ).

**Table 1. Enable Inputs (ENA, ENB)**

ENA	ENB	CHANNEL 1A	CHANNEL 0A	CHANNEL 1B	CHANNEL 0B
0	0	STANDBY	STANDBY	STANDBY	STANDBY
0	1	STANDBY	STANDBY	ENABLED	ENABLED
1	0	ENABLED	ENABLED	STANDBY	STANDBY
1	1	ENABLED	ENABLED	ENABLED	ENABLED

**Table 2. Out-of-Band Logic Threshold (MODEA, MODEB)**

MODEA	MODEB	CHANNEL 1A	CHANNEL 0A	CHANNEL 1B	CHANNEL 0B
0	0	SAS	SAS	SAS	SAS
0	1	SAS	SAS	SATA	SATA
1	0	SATA	SATA	SAS	SAS
1	1	SATA	SATA	SATA	SATA

# Quad Equalized 1.5/3.0/6.0GT/s SAS/SATA Redriver

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## Input Equalization (EQ0A, EQ1A, EQ0B, EQ1B)

The MAX4952 features control logic inputs (EQ0A, EQ1A, EQ0B, EQ1B) to enable input equalization on each channel, providing 3dB of boost (see Note 4 in the *Electrical Characteristics* table). Drive EQ\_ high to enable input equalization. Drive EQ\_ low to disable input equalization (see Table 3). EQ0A, EQ1A, EQ0B, and EQ1B have internal pulldown resistors of 70kΩ (typ).

**Table 3. Input Equalization (EQ0\_, EQ1\_)**

EQ1_	EQ0_	CHANNEL 1_ (dB)	CHANNEL 0_ (dB)
0	0	0	0
0	1	0	3 (typ)
1	0	3 (typ)	0
1	1	3 (typ)	3 (typ)

## Output Preemphasis (PE0A, PE1A, PE0B, PE1B)

The MAX4952 features control logic inputs (PE0A, PE1A, PE0B, PE1B) to enable output preemphasis on either channel, providing 3dB of boost. The MAX4952 true preemphasis; the transition signal is increased after a changing bit, thus increasing the total energy content of the signal when employed. Drive PE\_ high to enable output preemphasis. Drive PE\_ low to disable output preemphasis (see Table 4). PE0A, PE1A, PE0B, and PE1B have internal pulldown resistors of 70kΩ (typ).

**Table 4. Output Preemphasis (PE0\_, PE1\_)**

PE1_	PE0_	CHANNEL 1_ (dB)	CHANNEL 0_ (dB)
0	0	0	0
0	1	0	3 (typ)
1	0	3 (typ)	0
1	1	3 (typ)	3 (typ)

## Applications Information

### Exposed Pad Package

The exposed paddle, 42-pin TQFN package incorporates features that provide a very low thermal resistance path for heat removal from the IC. The exposed paddle on the MAX4952 must be soldered to GND for proper thermal and electrical performance. For more information on exposed paddle packages, refer to Maxim Application Note HFAN-08.1: *Thermal Considerations of QFN and Other Exposed-Paddle Packages*.

### Layout

Use controlled-impedance transmission lines to interface with high-speed inputs and outputs of the MAX4952. Place 2.2μF and 0.01μF power-supply bypass capacitors as close as possible to VCC, recommended on each VCC pin.

### Power-Supply Sequencing

**Caution: Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to the device.**

Proper power-supply sequencing is recommended for all devices. Always apply VCC before applying signals, especially if the signal is not current limited.

## Chip Information

PROCESS: BiCMOS

## Package Information

For the latest package outline information and land patterns, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
42 TQFN-EP	T423590M-1	<a href="#">21-0181</a>

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