

**TABLE 1. PIN DESCRIPTIONS**

Number	Name	Type		Description
1, 2	V <sub>CCO</sub>	Power		Output supply pins.
3, 4	nQ2, Q2	Output		Differential output pair. LVPECL interface levels.
5, 6	nQ1, Q1	Output		Differential output pair. LVPECL interface levels.
7, 8	nQ0, Q0	Output		Differential output pair. LVPECL interface levels.
9	PLL_BYPASS	Input	Pullup	Selects between the PLL and crystal inputs as the input to the dividers. When LOW, selects PLL. When HIGH, selects XTAL_IN, XTAL_OUT. LVCMOS / LVTTTL interface levels.
10	V <sub>CCA</sub>	Power		Analog supply pin.
11	V <sub>CC</sub>	Power		Core supply pin.
12	FB_SEL	Input	Pulldown	Feedback frequency select pin. LVCMOS/LVTTTL interface levels.
13, 14	XTAL_IN, XTAL_OUT	Input		Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output.
15, 18	N_SEL0 N_SEL1	Input	Pullup	Output frequency select pins. LVCMOS/LVTTTL interface levels.
16, 17	V <sub>EE</sub>			Negative supply pins.
19, 20	nQ5, Q5	Output		Differential output pair. LVPECL interface levels.
21, 22	nQ4, Q4	Output		Differential output pair. LVPECL interface levels.
23, 24	nQ3, Q3	Output		Differential output pair. LVPECL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		kΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ

**TABLE 3. TYPICAL APPLICATION FREQUENCY FUNCTION TABLE**

Inputs				Function			
XTAL (MHz)	FB_SEL	N_SEL1	N_SEL0	M	VCO (MHz)	N	Output (MHz)
25	0	0	0	20	500	2	250
25	0	0	1	20	500	4	125
25	0	1	0	20	500	5	100
25	0	1	1	20	500	8	62.5
25	1	0	0	24	600	3	200
25	1	0	1	24	600	4	150
25	1	1	0	24	600	6	100
25	1	1	1	24	600	12	50
26.5625	0	1	0	20	531.25	5	106.25
26.5625	1	0	0	24	637.5	3	212.5
26.5625	1	0	1	24	637.5	4	159.375
26.5625	1	1	0	24	637.5	6	106.25
26.5625	1	1	1	24	637.5	12	53.125
30	0	0	0	20	600	2	300
30	0	0	1	20	600	4	150
30	0	1	0	20	600	5	120
30	0	1	1	20	600	8	75
31.25	0	0	0	20	625	2	312.5
31.25	0	0	1	20	625	4	156.25
31.25	0	1	0	20	625	5	125
31.25	0	1	1	20	625	8	78.125
33.3333	0	0	0	20	666.6667	2	333.3333
33.3333	0	0	1	20	666.6667	4	166.6667
33.3333	0	1	0	20	666.6667	5	133.3333
33.3333	0	1	1	20	666.6667	8	83.3333

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage, $V_{CC}$	4.6V
Inputs, $V_I$	-0.5V to $V_{CC} + 0.5V$
Outputs, $I_O$	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, $\theta_{JA}$	37°C/W (0 mps)
Storage Temperature, $T_{STG}$	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{CC} = V_{CCO} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{CCA}$	Analog Supply Voltage		$V_{CC} - 0.10$	3.3	$V_{CC}$	V
$V_{CCO}$	Output Supply Voltage		3.135	3.3	3.465	V
$I_{EE}$	Power Supply Current				180	mA
$I_{CCA}$	Analog Supply Current				10	mA

**TABLE 4B. POWER SUPPLY DC CHARACTERISTICS,  $V_{CC} = 3.3V \pm 5\%$ ,  $V_{CCO} = 2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{CCA}$	Analog Supply Voltage		$V_{CC} - 0.10$	3.3	$V_{CC}$	V
$V_{CCO}$	Output Supply Voltage		2.375	2.5	2.625	V
$I_{EE}$	Power Supply Current				180	mA
$I_{CCA}$	Analog Supply Current				10	mA

**TABLE 4C. LVCMOS / LVTTTL DC CHARACTERISTICS,  $V_{CC} = 3.3V \pm 5\%$ ,  $V_{CCO} = 3.3V \pm 5\%$  OR  $2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage		2		$V_{CC} + 0.3$	V
$V_{IL}$	Input Low Voltage		-0.3		0.8	V
$I_{IH}$	Input High Current	FB_SEL	$V_{CC} = V_{IN} = 3.465V$		150	$\mu A$
		PLL_BYPASS, N_SEL0, N_SEL1	$V_{CC} = V_{IN} = 3.465V$		5	$\mu A$
$I_{IL}$	Input Low Current	FB_SEL	$V_{CC} = 3.465V, V_{IN} = 0V$	-5		$\mu A$
		PLL_BYPASS, N_SEL0, N_SEL1	$V_{CC} = 3.465V, V_{IN} = 0V$	-150		$\mu A$

**TABLE 4D. LVPECL DC CHARACTERISTICS,  $V_{CC} = 3.3V \pm 5\%$ ,  $V_{CCO} = 3.3V \pm 5\%$  OR  $2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage; NOTE 1		$V_{CCO} - 1.4$		$V_{CCO} - 0.9$	V
$V_{OL}$	Output Low Voltage; NOTE 1		$V_{CCO} - 2.0$		$V_{CCO} - 1.7$	V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CCO} - 2V$ .

**TABLE 5. CRYSTAL CHARACTERISTICS**

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		25		33.333	MHz
Equivalent Series Resistance (ESR)				50	$\Omega$
Shunt Capacitance				7	pF

NOTE: Characterized using an 18pF parallel resonant crystal.

**TABLE 6A. AC CHARACTERISTICS,  $V_{CC} = V_{CCO} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$F_{OUT}$	Output Frequency		40.833		340	MHz
$t_{jit}(\emptyset)$	RMS Phase Jitter (Random)	125MHz, Integration Range: 1.875MHz - 20MHz		0.41		ps
		312.5MHz, Integration Range: 1.875MHz - 20MHz		0.47		ps
$t_{sk}(o)$	Output Skew; NOTE 1, 2				40	ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle		45		55	%

See Parameter Measurement Information section.

NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions.

Measured at the output differential crossing points.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

**TABLE 6B. AC CHARACTERISTICS,  $V_{CC} = 3.3V \pm 5\%$ ,  $V_{CCO} = 2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$F_{OUT}$	Output Frequency		40.833		340	MHz
$t_{jit}(\emptyset)$	RMS Phase Jitter (Random)	125MHz, Integration Range: 1.875MHz - 20MHz		0.44		ps
		312.5MHz, Integration Range: 1.875MHz - 20MHz		0.46		ps
$t_{sk}(o)$	Output Skew; NOTE 1, 2				40	ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle		45		55	%

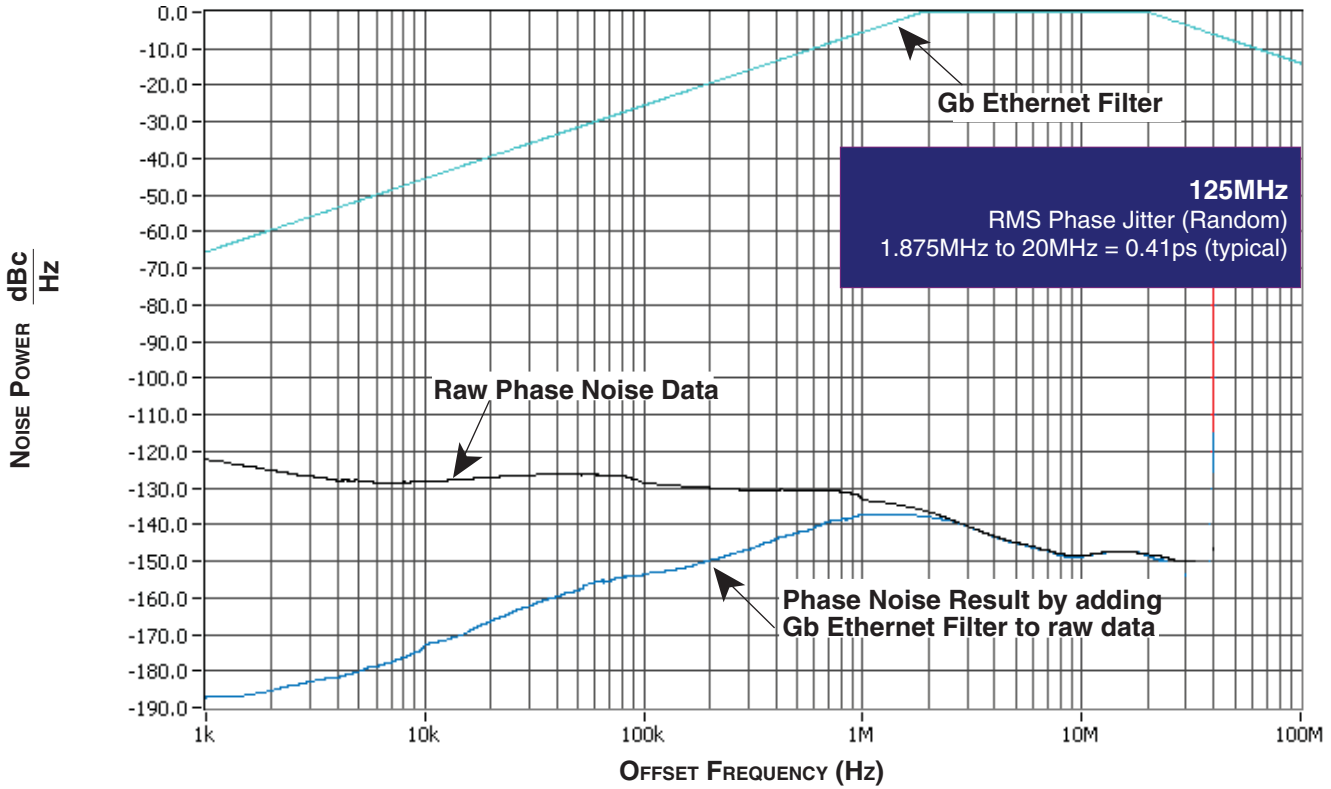
See Parameter Measurement Information section.

NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions.

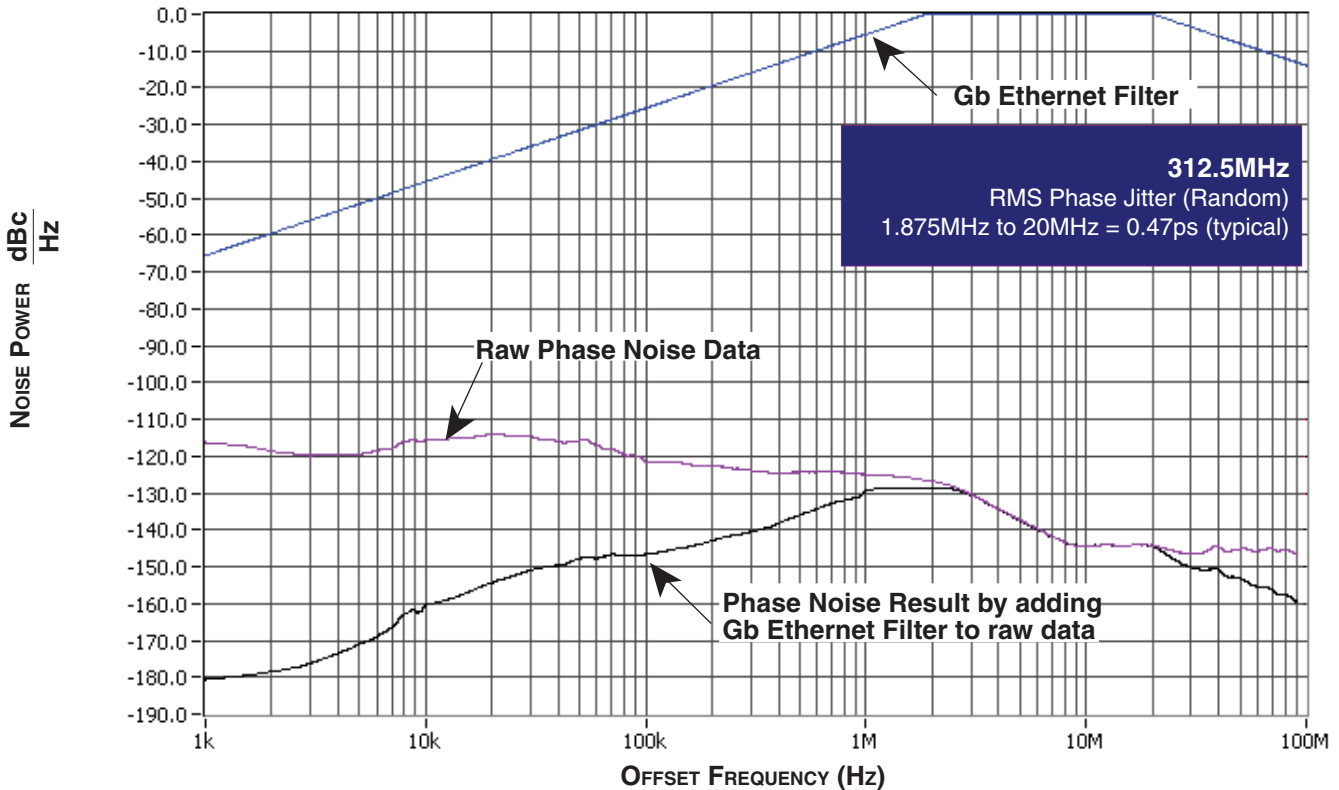
Measured at the output differential crossing points.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

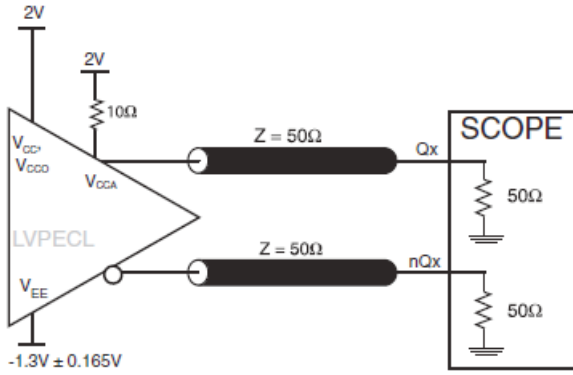
TYPICAL PHASE NOISE AT 125MHz @ 3.3V



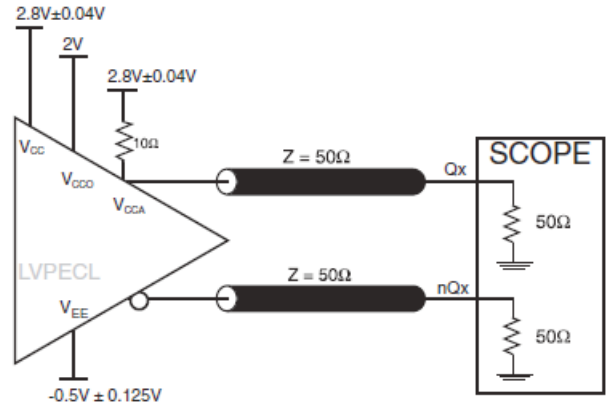
TYPICAL PHASE NOISE AT 312.5MHz @ 3.3V



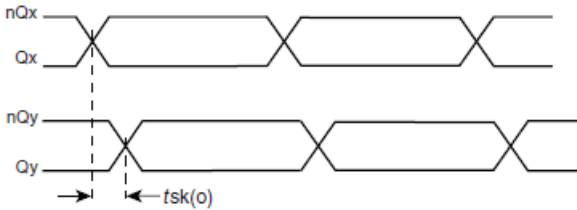
# PARAMETER MEASUREMENT INFORMATION



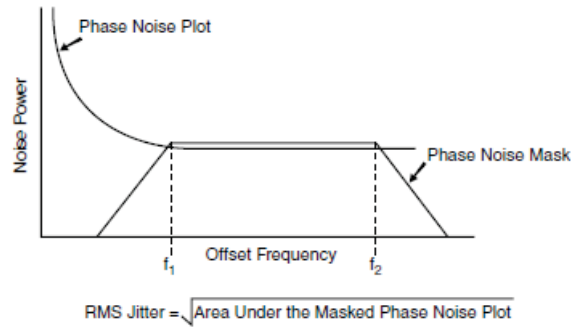
3.3V OUTPUT LOAD AC TEST CIRCUIT



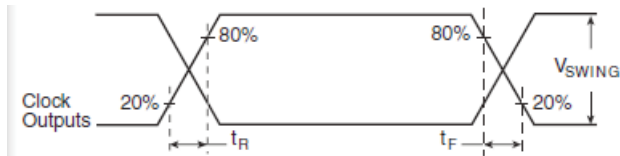
3.3V/2.5V OUTPUT LOAD AC TEST CIRCUIT



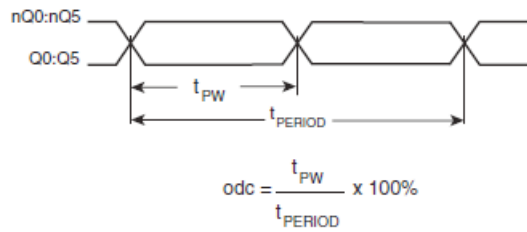
OUTPUT SKEW



RMS PHASE JITTER



OUTPUT RISE/FALL TIME



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

## APPLICATION INFORMATION

### POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The 843246I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{CC}$ ,  $V_{CCA}$  and  $V_{CCO}$  should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a  $10\Omega$  resistor along with a  $10\mu\text{F}$  and a  $.01\mu\text{F}$  bypass capacitor should be connected to each  $V_{CCA}$  pin.

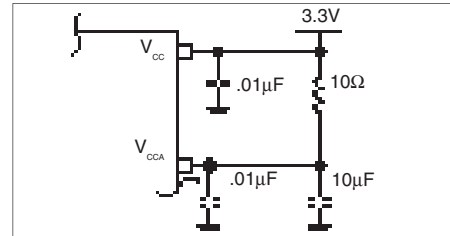


FIGURE 1. POWER SUPPLY FILTERING

### RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

#### INPUTS:

##### LVC MOS CONTROL PINS

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A  $1\text{k}\Omega$  resistor can be used.

#### OUTPUTS:

##### LVPECL OUTPUTS

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

### CRYSTAL INPUT INTERFACE

The 843246I has been characterized with  $18\text{pF}$  parallel resonant crystals. The capacitor values shown in *Figure 2*

below were determined using an  $18\text{pF}$  parallel resonant crystal and were chosen to minimize the ppm error.

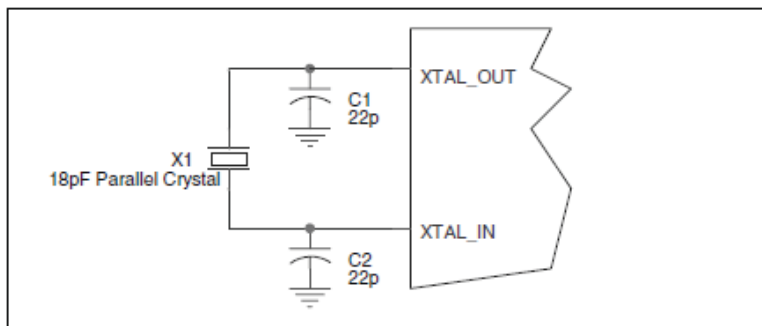


FIGURE 2. CRYSTAL INPUT INTERFACE

### LVC MOS TO XTAL INTERFACE

The XTAL\_IN input can accept a single-ended LVC MOS signal through an AC coupling capacitor. A general interface diagram is shown in Figure X. The XTAL\_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVC MOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output

impedance of the driver ( $R_o$ ) plus the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First,  $R_1$  and  $R_2$  in parallel should equal the transmission line impedance. For most 50Ω applications,  $R_1$  and  $R_2$  can be 100Ω. This can also be accomplished by removing  $R_1$  and making  $R_2$  50Ω.

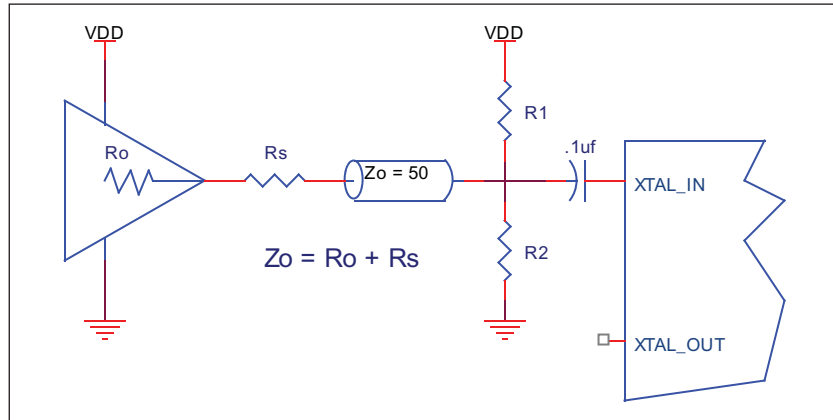


FIGURE 3. GENERAL DIAGRAM FOR LVC MOS DRIVER TO XTAL INPUT INTERFACE

### TERMINATION FOR 3.3V LVPECL OUTPUT

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to

drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. Figures 3A and 3B show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

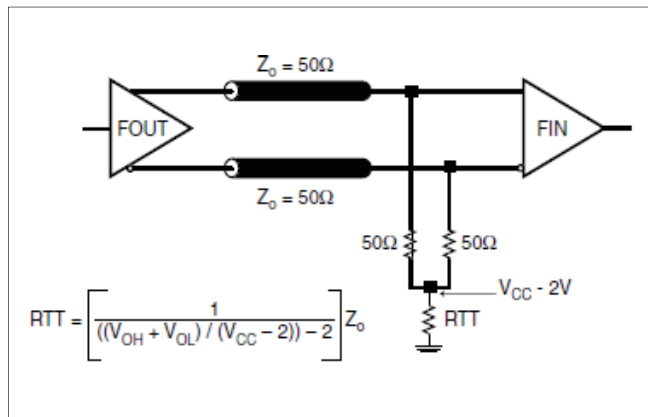


FIGURE 3A. LVPECL OUTPUT TERMINATION

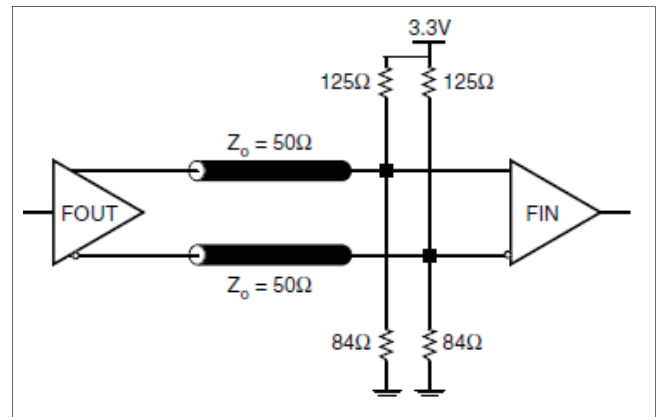


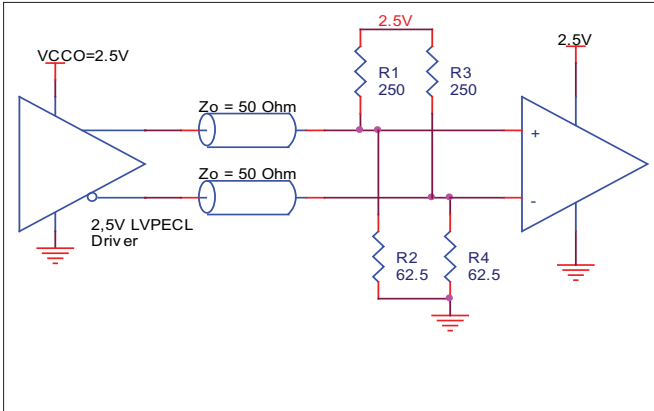
FIGURE 3B. LVPECL OUTPUT TERMINATION



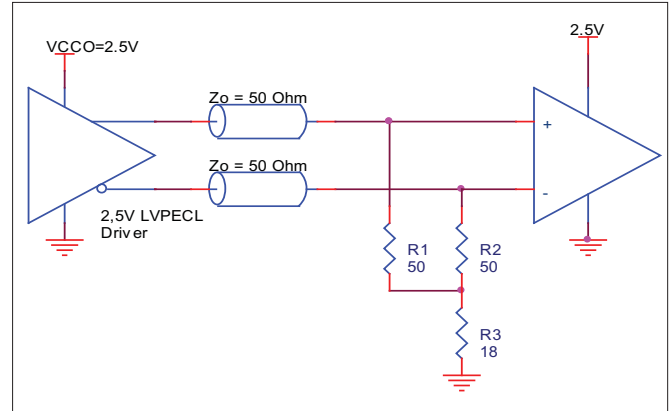
**TERMINATION FOR 2.5V LVPECL OUTPUT**

Figure 4A and Figure 4B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to  $V_{cc} - 2V$ . For  $V_{cc} = 2.5V$ , the  $V_{cc} - 2V$  is very

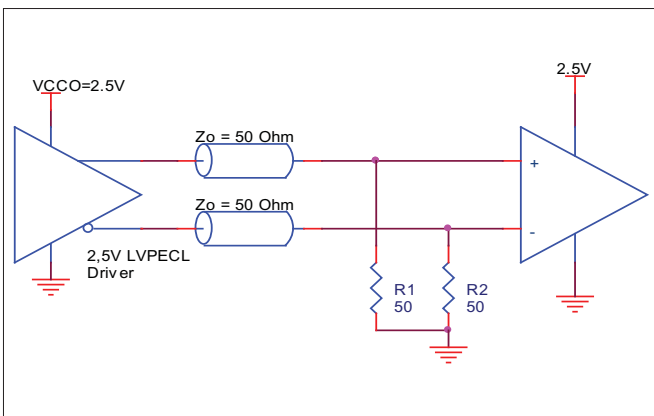
close to ground level. The R3 in Figure 4B can be eliminated and the termination is shown in Figure 4C.



**FIGURE 4A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE**



**FIGURE 4B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE**

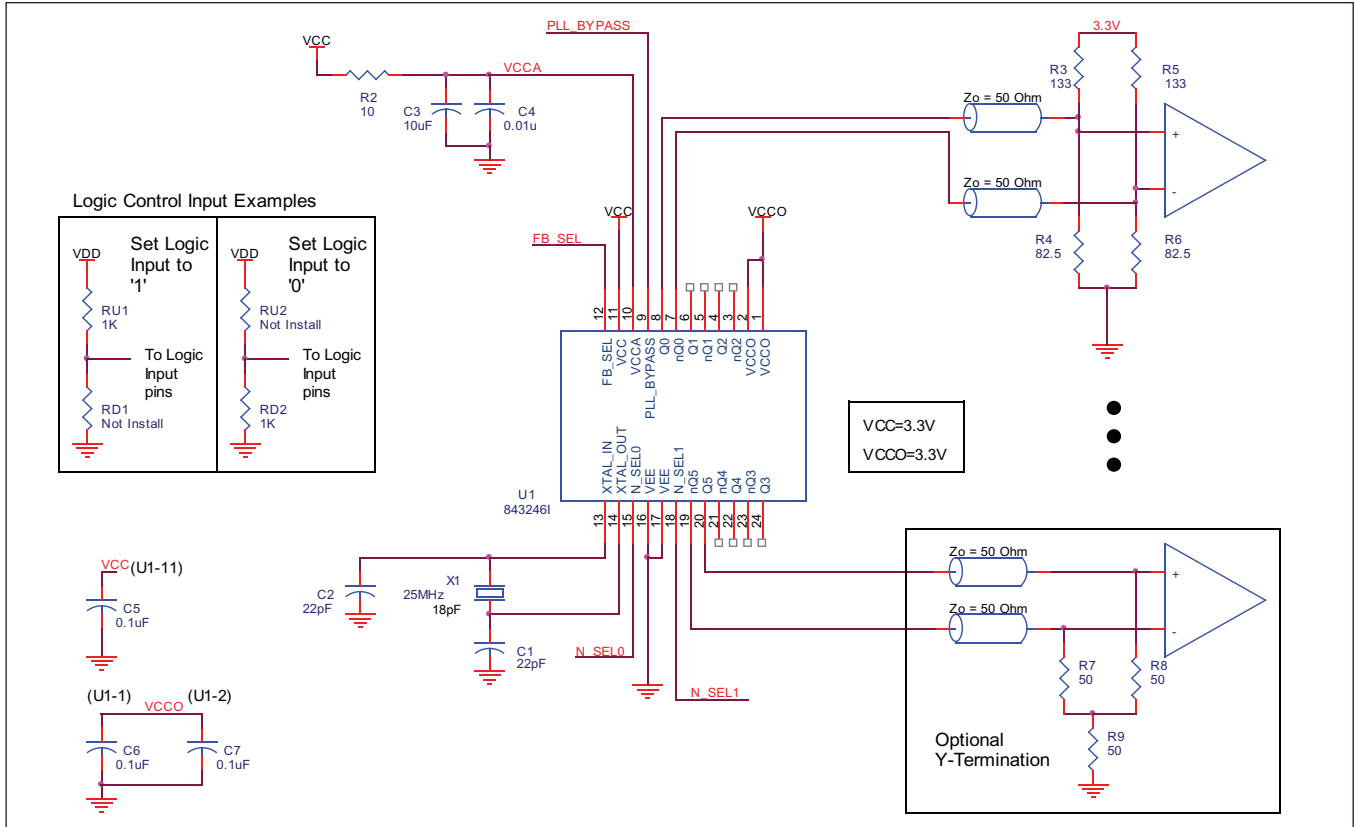


**FIGURE 4C. 2.5V LVPECL DRIVER TERMINATION EXAMPLE**

**LAYOUT GUIDELINE**

Figure 5 shows an example of 8432461 application schematic. In this example, the device is operated at  $V_{CC} = 3.3V$ . The 18pF parallel resonant 25MHz crystal is used. The  $C1 = 22pF$  and  $C2 = 22pF$  are recommended for frequency accuracy. For different board layout, the  $C1$  and  $C2$  may be slightly adjusted

for optimizing frequency accuracy. Two examples of LVPECL termination are shown in this schematic. Additional termination approaches are shown in the LVPECL Termination Application Note.

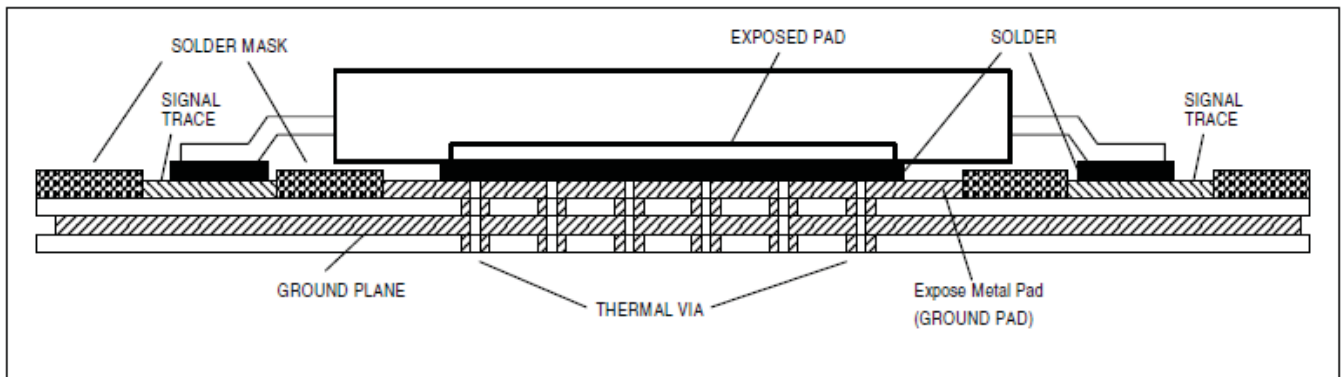


**FIGURE 5. SCHEMATIC OF RECOMMENDED LAYOUT**

**THERMAL RELEASE PATH**

The expose metal pad provides heat transfer from the device to the P.C. board. The expose metal pad is ground pad connected to ground plane through thermal via. The exposed pad on the device to the exposed metal pad on the PCB is contacted through solder

as shown in Figure 4. For further information, please refer to the Application Note on Surface Mount Assembly of Amkor's Thermally /Electrically Enhance Leadframe Base Package, Amkor Technology.



**FIGURE 6. P.C. BOARD FOR EXPOSED PAD THERMAL RELEASE PATH EXAMPLE**

## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 843246I. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the 843246I is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{EE\_MAX} = 3.465V * 180mA = 623.7mW$
- Power (outputs)<sub>MAX</sub> = **30mW/Loaded Output pair**  
If all outputs are loaded, the total power is  $6 * 30mW = 180mW$

**Total Power**<sub>MAX</sub> (3.465V, with all outputs switching) =  $623.7mW + 180mW = 803.7mW$

### 2. Junction Temperature.

Junction temperature, T<sub>j</sub>, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for T<sub>j</sub> is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

T<sub>j</sub> = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

Pd<sub>total</sub> = Total Device Power Dissipation (example calculation is in section 1 above)

T<sub>A</sub> = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 37°C/W per Table 7 below.

Therefore, T<sub>j</sub> for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ C + 0.804W * 37^\circ C/W = 114.7^\circ C. \text{ This is below the limit of } 125^\circ C.$$

This calculation is only an example. T<sub>j</sub> will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

**TABLE 7. THERMAL RESISTANCE  $\theta_{JA}$  FOR 24-PIN TSSOP, E-PAD FORCED CONVECTION**

	$\theta_{JA}$ by Velocity (Meters per Second)		
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	37°C/W	31°C/W	30°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 7*.

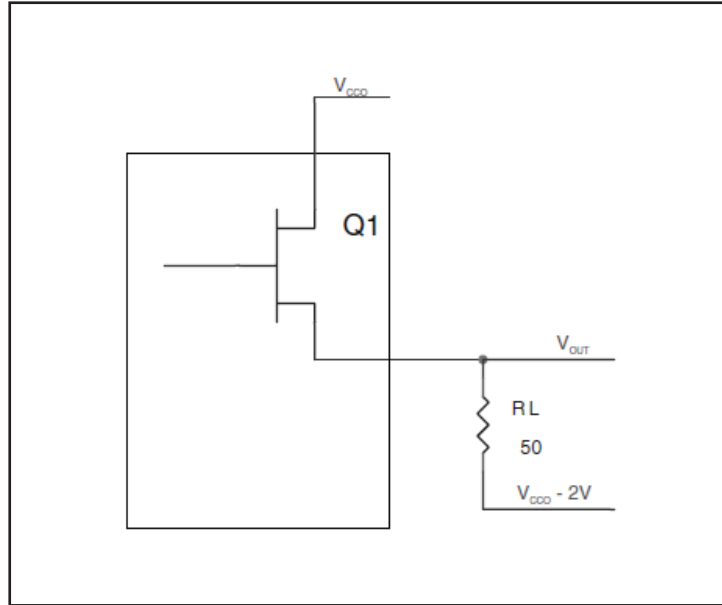


FIGURE 7. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of  $V_{CCO} - 2V$ .

- For logic high,  $V_{OUT} = V_{OH\_MAX} = V_{CCO\_MAX} - 0.9V$   
 $(V_{CCO\_MAX} - V_{OH\_MAX}) = 0.9V$
- For logic low,  $V_{OUT} = V_{OL\_MAX} = V_{CCO\_MAX} - 1.7V$   
 $(V_{CCO\_MAX} - V_{OL\_MAX}) = 1.7V$

Pd\_H is power dissipation when the output drives high.  
 Pd\_L is the power dissipation when the output drives low.

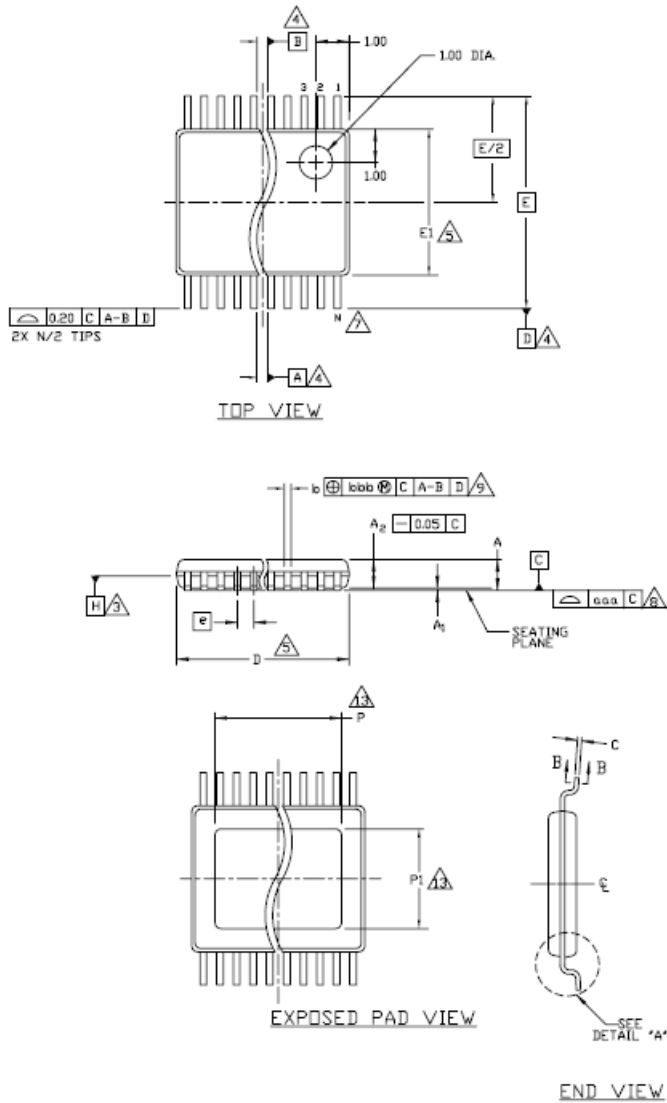
$$Pd\_H = [(V_{OH\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = 19.8mW$$

$$Pd\_L = [(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = 10.2mW$$

$$\text{Total Power Dissipation per output pair} = Pd\_H + Pd\_L = 30mW$$

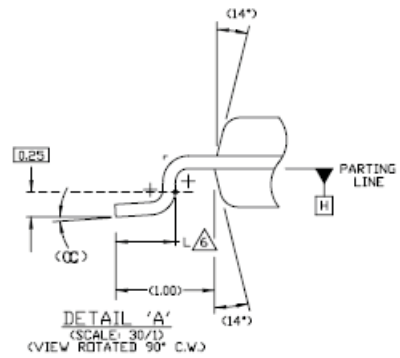
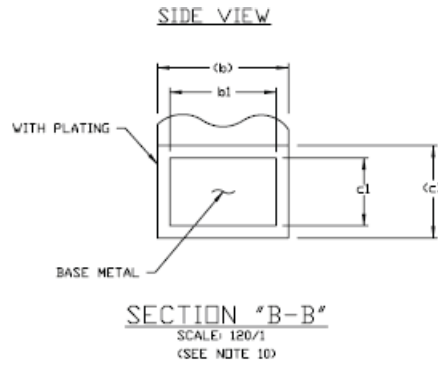
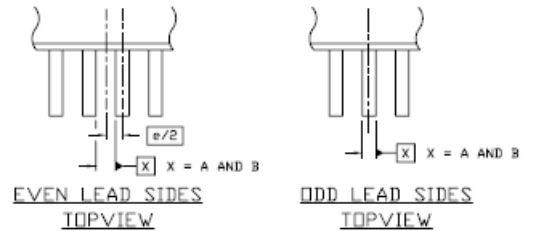
PACKAGE OUTLINE - G SUFFIX FOR 24 LEAD TSSOP, E-PAD

TABLE 9. PACKAGE DIMENSIONS FOR 24 LEAD TSSOP, E-PAD



SYMBOL	Millimeters		
	Minimum	Nominal	Maximum
N	24		
A	--		1.10
A1	0.05		0.15
A2	0.85	0.90	0.95
b	0.19		0.30
b1	0.19	0.22	0.25
c	0.09		0.20
c1	0.09	0.127	0.16
D	7.70	7.80	7.90
E	6.40 BASIC		
E1	4.30	4.40	4.50
e	0.65 BASIC		
L	0.50	0.60	0.70
P	5.0		5.5
P1	3.0		3.2
$\alpha$	0°		8°
aaa	0.076		
bbb	0.10		

Reference Document: JEDEC Publication 95, MO-153



## RELIABILITY INFORMATION

**TABLE 8.  $\theta_{JA}$  VS. AIR FLOW TABLE FOR 24 LEAD TSSOP, E-PAD**

$\theta_{JA}$ by Velocity (Meters per Second)			
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	37°C/W	31°C/W	30°C/W

### TRANSISTOR COUNT

The transistor count for 843246I is: 3863

**TABLE 10. ORDERING INFORMATION**

<b>Part/Order Number</b>	<b>Marking</b>	<b>Package</b>	<b>Shipping Packaging</b>	<b>Temperature</b>
843246BGILF	ICS843246BGIL	24 Lead "Lead-Free" TSSOP, E-Pad	tube	-40°C to 85°C
843246BGILFT	ICS843246BGIL	24 Lead "Lead-Free" TSSOP, E-Pad	tape & reel	-40°C to 85°C

**REVISION HISTORY SHEET**

<b>Rev</b>	<b>Table</b>	<b>Page</b>	<b>Description of Change</b>	<b>Date</b>
A	T10	16	Ordering Information - removed leaded devices, quantity from tape & reel, ICS from Part/Order number and LF note below the table. Updated datasheet header and footer.	12/8/15





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