# AD5165

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**REVISION HISTORY**

**4/04—Revision 0: Initial Version**

# ELECTRICAL CHARACTERISTICS—100 kΩ VERSION

$V_{DD}$ = 5 V ± 10%, or 3 V ± 10%; $V_A$ = $V_{DD}$; $V_B$ = 0 V; −40°C < $T_A$ < +125°C; unless otherwise noted.

**Table 1.**

| Parameter | Symbol | Conditions | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|
| DC CHARACTERISTICS—RHEOSTAT MODE | | | | | | |
| Resistor Differential Nonlinearity[2] | R-DNL | $R_{WB}$, $V_A$ = no connect | −1 | ±0.1 | +1 | LSB |
| Resistor Integral Nonlinearity[2] | R-INL | $R_{WB}$, $V_A$ = no connect | −2 | ±0.25 | +2 | LSB |
| Nominal Resistor Tolerance[3] | $\Delta R_{AB}/R_{AB}$ | $T_A$ = 25°C | −20 | | +20 | % |
| Resistance Temperature Coefficient | $(\Delta R_{AB}/R_{AB})/\Delta T \times 10^6$ | $V_{AB}$ = $V_{DD}$, wiper = no connect | | 35 | | ppm/°C |
| Wiper Resistance | $R_W$ | $V_{DD}$ = 2.7 V/5.5 V | | 85/50 | 150/120 | Ω |
| DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE | | | | | | |
| Resolution | N | | | | 8 | Bits |
| Differential Nonlinearity[4] | DNL | | −1 | ±0.1 | +1 | LSB |
| Integral Nonlinearity[4] | INL | | −1 | ±0.3 | +1 | LSB |
| Voltage Divider Temperature Coefficient | $(\Delta V_W/V_W)/\Delta T \times 10^6$ | Code = 0x80 | | 15 | | ppm/°C |
| Full-Scale Error | $V_{WFSE}$ | Code = 0xFF | −0.5 | −0.3 | 0 | LSB |
| Zero-Scale Error | $V_{WZSE}$ | Code = 0x00 | 0 | 0.1 | 0.5 | LSB |
| RESISTOR TERMINALS | | | | | | |
| Voltage Range[5] | $V_{A,B,W}$ | | GND | | $V_{DD}$ | V |
| Capacitance[6] A, B | $C_{A,B}$ | f = 1 MHz, measured to GND, Code = 0x80 | | 90 | | pF |
| Capacitance[6] W | $C_W$ | f = 1 MHz, measured to GND, Code = 0x80 | | 95 | | pF |
| Common-Mode Leakage | $I_{CM}$ | $V_A$ = $V_B$ = $V_{DD}/2$ | | 1 | | nA |
| DIGITAL INPUTS AND OUTPUTS | | | | | | |
| Input Logic High | $V_{IH}$ | $V_{DD}$ = 2.7 V to 5.5 V | 1.8 | | | V |
| Input Logic Low | $V_{IL}$ | $V_{DD}$ = 2.7 V to 5.5 V | | | 0.6 | V |
| Input Capacitance[6] | $C_{IL}$ | | | 5 | | pF |
| POWER SUPPLIES | | | | | | |
| Power Supply Range | $V_{DD\ RANGE}$ | | 2.7 | | 5.5 | V |
| Supply Current | $I_{DD}$ | Digital inputs = 0 V or $V_{DD}$ | | 0.05 | 1 | µA |
| | | $V_{DD}$ = 2.7 V, digital inputs = 1.8 V | | 10 | | µA |
| | | $V_{DD}$ = 5 V, digital inputs = 1.8 V | | 500 | | µA |
| Power Dissipation[7] | $P_{DISS}$ | Digital inputs = 0 V or $V_{DD}$ | | | 5.5 | µW |
| Power Supply Sensitivity | PSS | $V_{DD}$ = +5 V ± 10%, Code = Midscale | | ±0.001 | ±0.005 | %/% |
| DYNAMIC CHARACTERISTICS[6, 8] | | | | | | |
| Bandwidth −3 dB | BW | Code = 0x80 | | 55 | | kHz |
| Total Harmonic Distortion | $THD_W$ | $V_A$ = 1 V rms, $V_B$ = 0 V, f = 1 kHz, | | 0.05 | | % |
| $V_W$ Settling Time | $t_S$ | $V_A$ = 5 V, $V_B$ = 0 V, ±1 LSB error band | | 2 | | µs |
| Resistor Noise Voltage Density | $e_{N\_WB}$ | $R_{WB}$ = 50 kΩ | | 28 | | nV/√Hz |

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[1] Typical specifications represent average readings at +25°C and $V_{DD}$ = 5 V.

[2] Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.

[3] $V_{AB}$ = $V_{DD}$, wiper ($V_W$) = no connect.

[4] INL and DNL are measured at $V_W$ with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. $V_A$ = $V_{DD}$ and $V_B$ = 0 V.

[5] Resistor terminals A, B, and W have no limitations on polarity with respect to each other.

[6] Guaranteed by design and not subject to production test.

[7] $P_{DISS}$ is calculated from ($I_{DD} \times V_{DD}$). CMOS logic level inputs result in minimum power dissipation.

[8] All dynamic characteristics use $V_{DD}$ = 5 V.

# TIMING CHARACTERISTICS—100 kΩ VERSION

$V_{DD}$ = +5 V ± 10%, or +3 V ± 10%; $V_A$ = $V_{DD}$; $V_B$ = 0 V; −40°C < $T_A$ < +125°C; unless otherwise noted.

**Table 2.**

| Parameter | Symbol | Conditions | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|
| 3-WIRE INTERFACE TIMING CHARACTERISTICS[2, 3, 4] (specifications apply to all parts) | | | | | | |
| Clock Frequency | $f_{CLK}$= 1/( $t_{CH}$+ $t_{CL}$) | | | | 25 | MHz |
| Input Clock Pulse Width | $t_{CH}$, $t_{CL}$ | Clock level high or low | 20 | | | ns |
| Data Setup Time | $t_{DS}$ | | 5 | | | ns |
| Data Hold Time | $t_{DH}$ | | 5 | | | ns |
| CS Setup Time | $t_{CSS}$ | | 15 | | | ns |
| CS Low Pulse Width | $t_{CSW}$ | | 40 | | | ns |
| CLK Fall to CS Rise Hold Time | $t_{CSH0}$ | | 0 | | | ns |
| CLK Fall to CS Fall Hold Time | $t_{CSH1}$ | | 0 | | | ns |
| CS Fall to Clock Rise Setup | $t_{CS1}$ | | 10 | | | ns |

[1] Typical specifications represent average readings at +25°C and $V_{DD}$ = 5 V.
[2] Guaranteed by design and not subject to production test.
[3] All dynamic characteristics use $V_{DD}$ = 5 V.
[4] See Figure 34 and Figure 35 for location of measured values. All input control voltages are specified with $t_R$ = $t_F$ = 2 ns (10% to 90% of 3 V) and timed from a voltage level of 1.5 V.

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = +25°C, unless otherwise noted.[1,2]

**Table 3.**

| Parameter | Value |
|---|---|
| $V_{DD}$ to GND | −0.3 V to +7 V |
| $V_A$, $V_B$, $V_W$ to GND | $V_{DD}$ |
| Maximum Current | |
|   $I_{WB}$, $I_{WA}$ Pulsed | ±20 mA |
|   $I_{WB}$ Continuous ($R_{WB} \leq 1$ kΩ, A open)[2] | ±5 mA |
|   $I_{WA}$ Continuous ($R_{WA} \leq 1$ kΩ, B open)[2] | ±5 mA |
| Digital Inputs and Output Voltage to GND | 0 V to +7 V |
| Operating Temperature Range | −40°C to +125°C |
| Maximum Junction Temperature ($T_{JMAX}$) | 150°C |
| Storage Temperature | −65°C to +150°C |
| Lead Temperature (Soldering, 10 – 30 sec) | 245°C |
| Thermal Resistance[2] $\theta_{JA}$: TSOT-8 | 200°C/W |

[1] Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.
[2] Package power dissipation = ($T_{JMAX}$ − TA)/$\theta_{JA}$.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTIONAL DESCRIPTIONS



*Figure 4.*
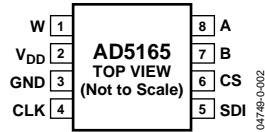
**Table 4.**

| Pin | Name | Description |
|---|---|---|
| 1 | W | Wiper terminal. GND ≤ $V_A$ ≤ $V_{DD.}$ |
| 2 | $V_{DD}$ | Positive Power Supply. |
| 3 | GND | Digital Ground. |
| 4 | CLK | Serial Clock Input. Positive-edge triggered. |
| 5 | SDI | Serial Data Input (data loads MSB first). |
| 6 | CS | Chip Select Input, active high. When CS returns low, data is loaded into the wiper register. |
| 7 | B | B terminal. GND ≤ $V_A$ ≤ $V_{DD}$. |
| 8 | A | A terminal. GND ≤ $V_A$ ≤ $V_{DD}$. |

# TYPICAL PERFORMANCE CHARACTERISTICS
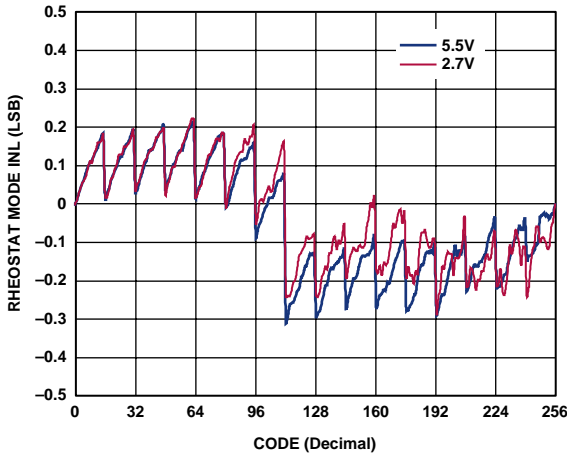


*Figure 5. R-INL vs. Code vs. Supply Voltages*
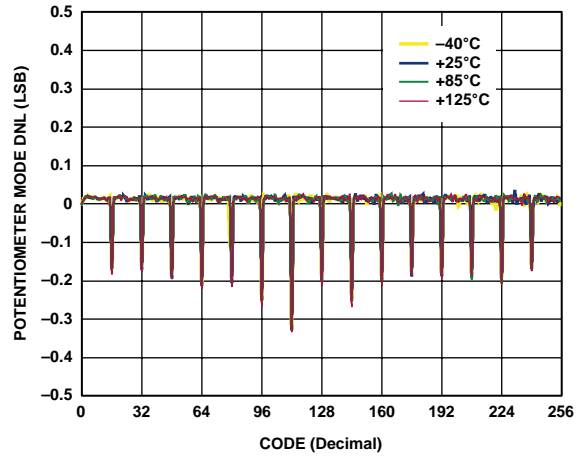


*Figure 8. DNL vs. Code vs. Temperature, $V_{DD}$ = 5 V*
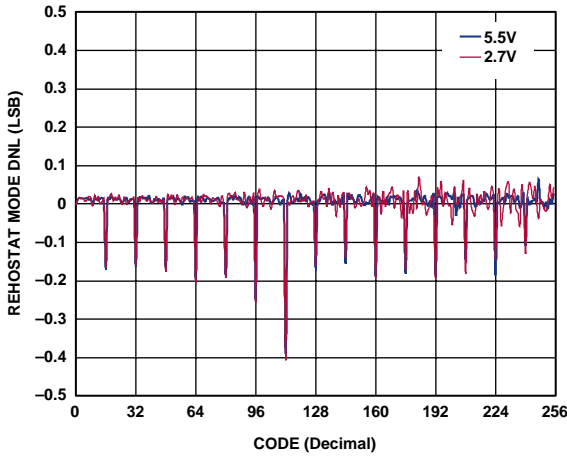


*Figure 6. R-DNL vs. Code vs. Supply Voltages*
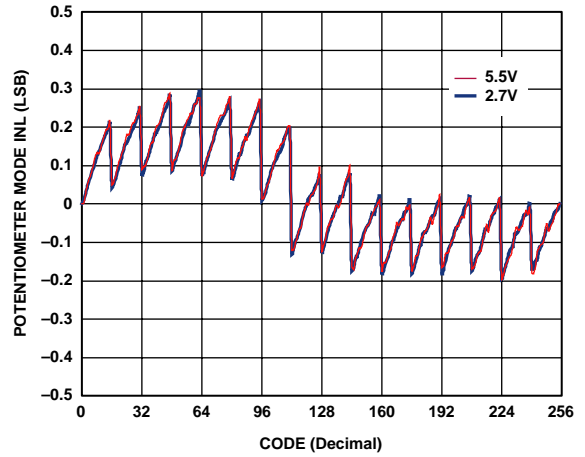


*Figure 9. INL vs. Code vs. Supply Voltages*
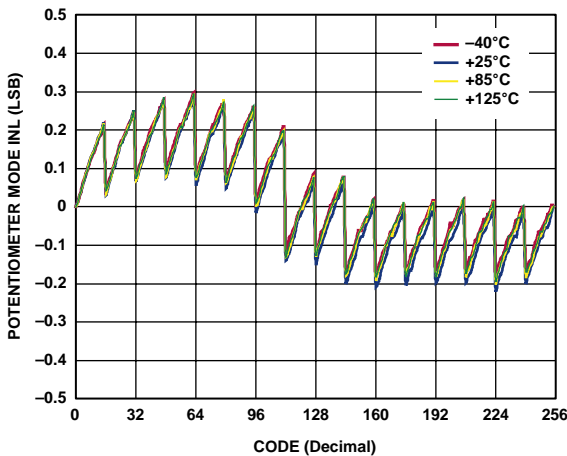


*Figure 7. INL vs. Code vs. Temperature , $V_{DD}$ = 5 V*
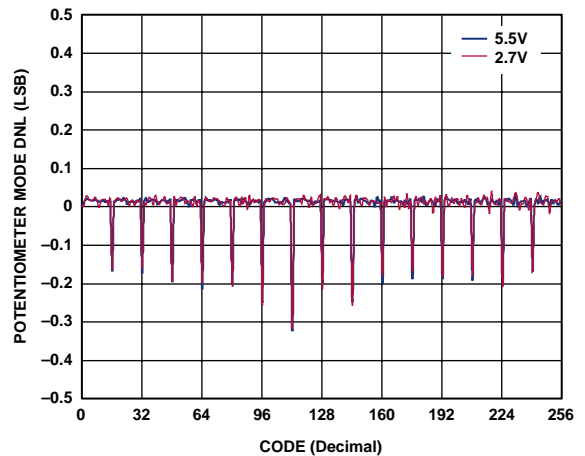


*Figure 10. DNL vs. Code vs. Supply Voltages*
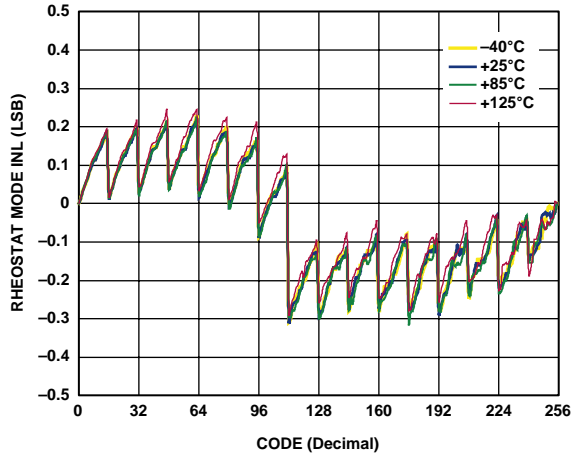
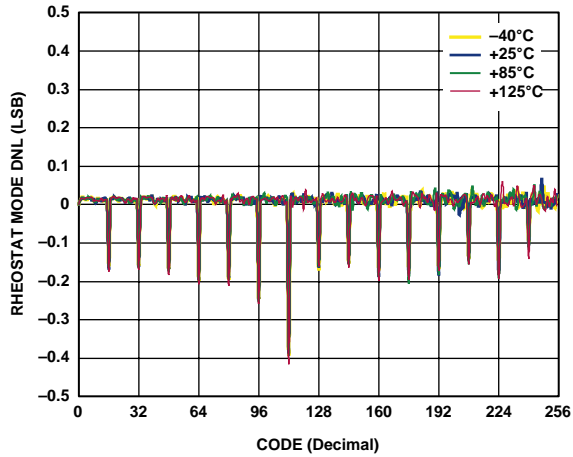Figure 11. R-INL vs. Code vs. Temperature, $V_{DD}$ = 5 V



Figure 14. Zero-Scale Error vs. Temperature



Figure 12. R-DNL vs. Code vs. Temperature, $V_{DD}$ = 5 V
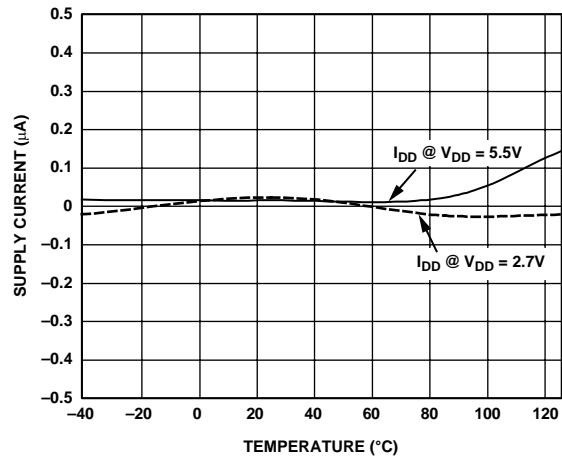


Figure 15. Supply Current vs. Temperature



Figure 13. Full-Scale Error vs. Temperature
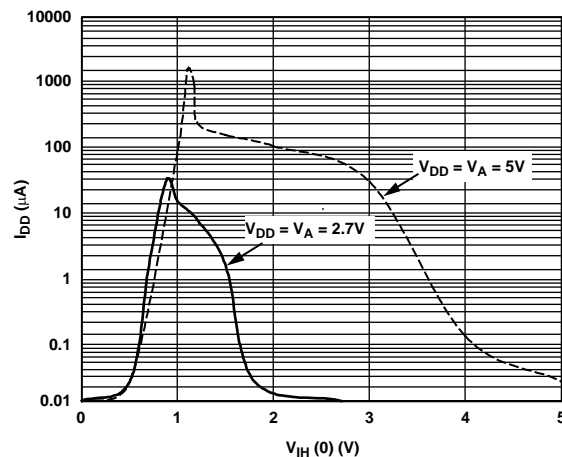


Figure 16. Supply Current vs. Digital Input Voltage
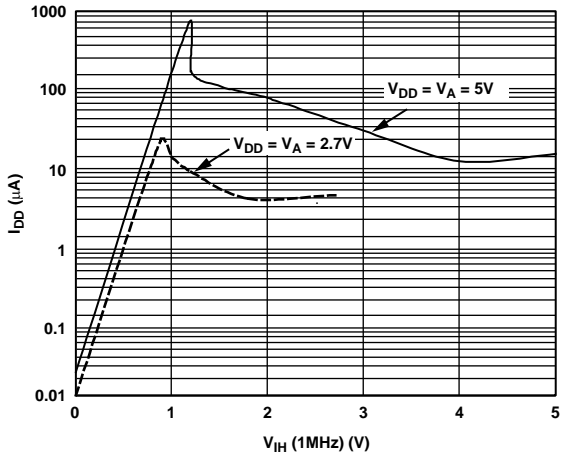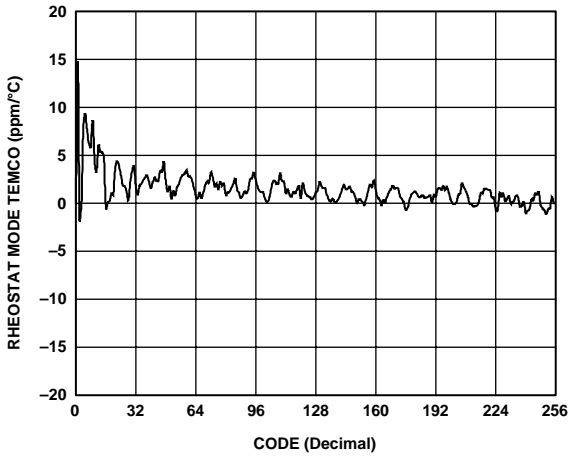
Figure 17. Supply Current vs. Digital Input Voltage



Figure 18. Rheostat Mode Tempco ΔR_WB/ΔT vs. Code
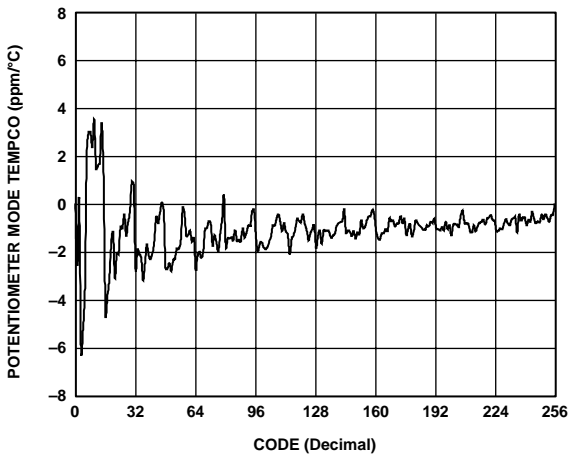


Figure 19. Potentiometer Mode Tempco ΔV_WB/ΔT vs. Code
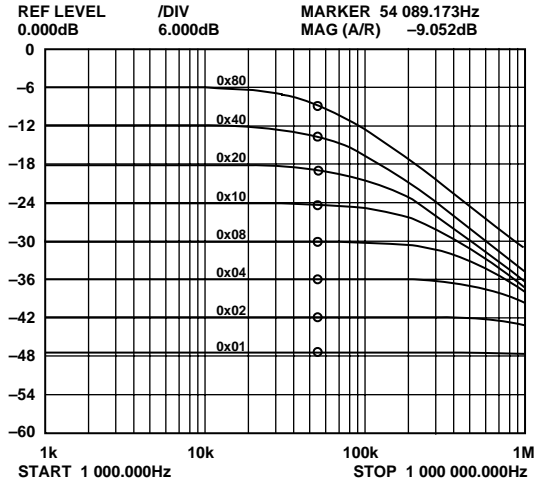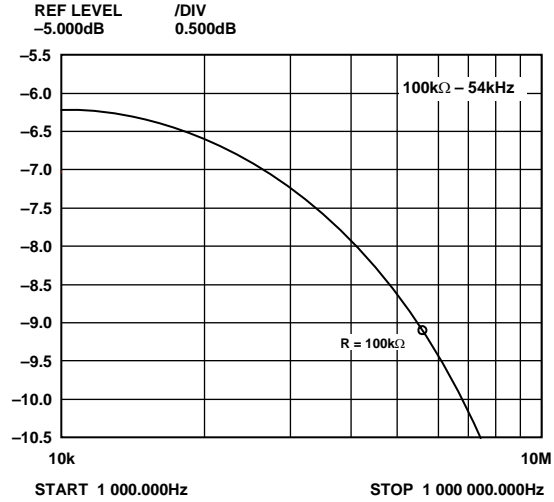


Figure 20. Gain vs. Frequency vs. Code, R_AB = 100 kΩ



Figure 21. −3 dB Bandwidth @ Code = 0x80



Figure 22. PSRR vs. Frequency
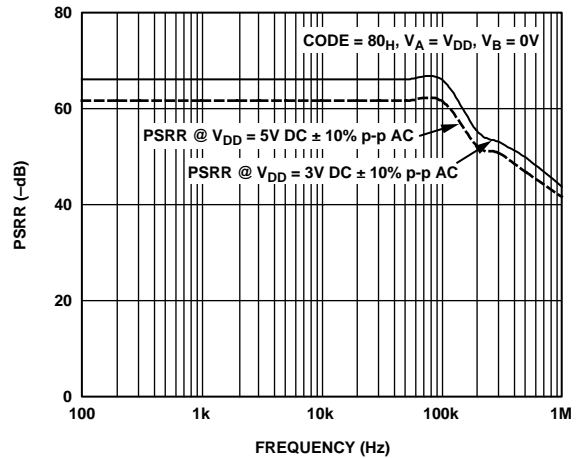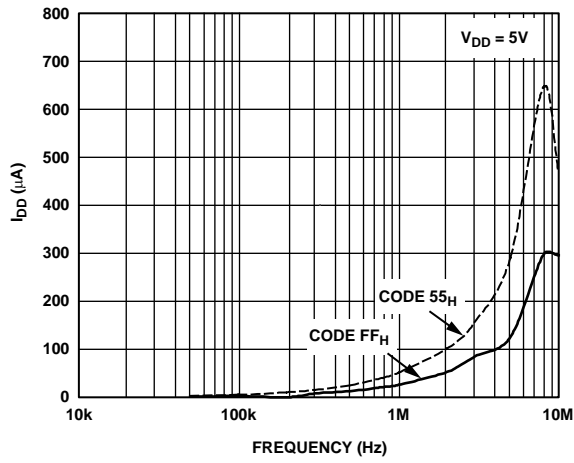
Figure 23. $I_{DD}$ vs. Frequency



Figure 24. Large Signal Settling Time, Code 0xFF–0x00
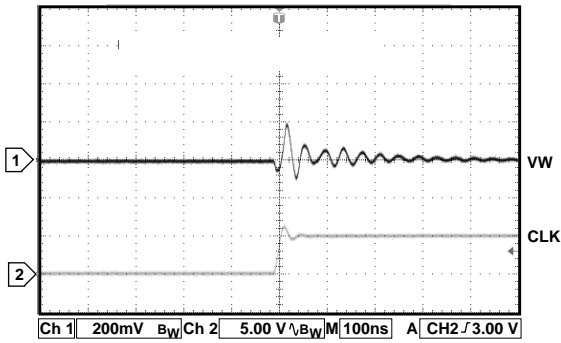


Figure 25. Digital Feedthrough



Figure 26. Midscale Glitch, Code 0x80–0x7F

# TEST CIRCUITS

Figure 27 to Figure 33 illustrate the test circuits that define the test conditions used in the product specification tables.
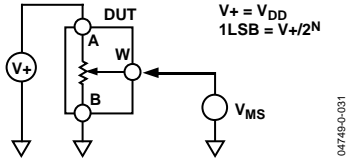


Figure 27. Test Circuit for Potentiometer Divider Nonlinearity Error
(INL, DNL)



Figure 28. Test Circuit for Resistor Position Nonlinearity Error
(Rheostat Operation; R-INL, R-DNL)



Figure 29. Test Circuit for Wiper Resistance



Figure 30. Test Circuit for Power Supply Sensitivity (PSS, PSSR)



Figure 31. Test Circuit for Gain vs. Frequency



Figure 32. Test Circuit for Incremental ON Resistance



Figure 33. Test Circuit for Common-Mode Leakage Current

# 3-WIRE DIGITAL INTERFACE

Note that in the AD5165 data is loaded MSB first.

**Table 5. AD5165 Serial Data-Word Format**

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| MSB | | | | | | | LSB |
| $2^7$ | | | | | | | $2^0$ |
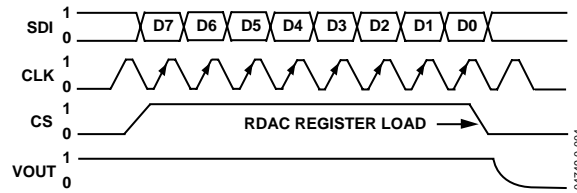


Figure 34. 3-Wire Digital Interface Timing Diagram
($V_A = 5\ V$, $V_B = 0\ V$, $V_W = V_{OUT}$)
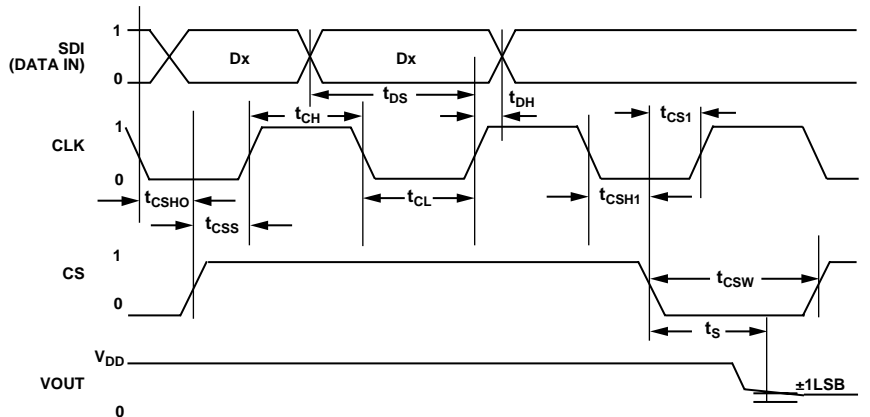


Figure 35. 3-Wire Digital Interface Detailed Timing Diagram ($V_A = 5\ V$, $V_B = 0\ V$, $V_W = V_{OUT}$)

# THEORY OF OPERATION

The AD5165 is a 256-position digitally controlled variable resistor (VR) device.

## PROGRAMMING THE VARIABLE RESISTOR
### Rheostat Operation

The nominal resistance of the RDAC between terminals A and B is available in 100 kΩ. The nominal resistance ($R_{AB}$) of the VR has 256 contact points accessed by the wiper terminal, plus the B terminal contact. The 8-bit data in the RDAC latch is decoded to select one of the 256 possible settings.



*Figure 36. Rheostat Mode Configuration*

Assuming that a 100 kΩ part is used, the wiper's first connection starts at the B terminal for data 0x00. Because there is a 50 Ω wiper contact resistance, such a connection yields a minimum of 100 Ω (2 × 50 Ω) resistance between terminals W and B. The second connection is the first tap point, which corresponds to 490 Ω ($R_{WB} = R_{AB}/256 + 2 \times R_W = 390\ \Omega + 2 \times 50\ \Omega$) for data 0x01. The third connect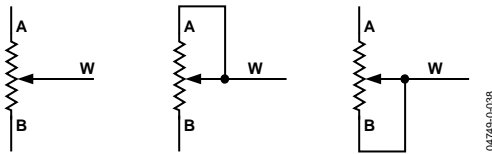ion is the next tap point, representing 880 Ω (2 × 390 Ω + 2 × 50 Ω) for data 0x02, and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 100,100 Ω ($R_{AB} + 2 \times R_W$).
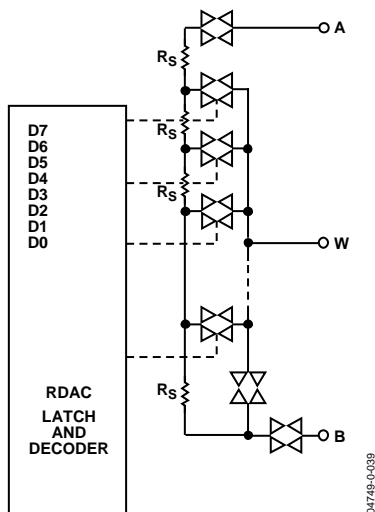


*Figure 37. AD5165 Equivalent RDAC Circuit*

The general equation determining the digitally programmed output resistance between W and B is

$$R_{WB}(D) = \frac{D}{256} \times R_{AB} + 2 \times R_W \qquad (1)$$

where:

$D$ is the decimal equivalent of the binary code loaded in the 8-bit RDAC register.

$R_{AB}$ is the end-to-end resistance.

$R_W$ is the wiper resistance contributed by the on resistance of the internal switch.

In summary, if $R_{AB}$ = 100 kΩ and the A terminal is open circuited, the following output resistance $R_{WB}$ is set for the indicated RDAC latch codes.

**Table 6. Codes and Corresponding R_WB Resistance**

| D (Dec.) | R_WB (Ω) | Output State |
|---|---|---|
| 255 | 99,710 | Full scale ($R_{AB}$ – 1 LSB + $R_W$) |
| 128 | 50,100 | Midscale |
| 1 | 490 | 1 LSB |
| 0 | 100 | Zero scale (wiper contact resistance) |

Note that, in the zero-scale condition, a finite wiper resistance of 100 Ω is present. Care should be taken to limit the current flow between W and B in this state to a maximum pulse current of no more than 20 mA. Otherwise, degradation or possible destruction of the internal switch contact can occur.

Similar to the mechanical potentiometer, the resistance of the RDAC between the wiper W and terminal A also produces a digitally controlled complementary resistance, $R_{WA}$. When these terminals are used, the B terminal can be opened. Setting the resistance value for $R_{WA}$ starts at a maximum value of resistance and decreases as the data loaded in the latch increases in value. The general equation for this operation is

$$R_{WA}(D) = \frac{256 - D}{256} \times R_{AB} + 2 \times R_W \qquad (2)$$

For $R_{AB}$ = 100 kΩ with the B terminal open circuited, the following output resistance $R_{WA}$ is set for the indicated RDAC latch codes.

**Table 7. Codes and Corresponding R_WA Resistance**

| D (Dec.) | R_WA (Ω) | Output State |
|---|---|---|
| 255 | 490 | Full scale |
| 128 | 50,100 | Midscale |
| 1 | 99, 710 | 1 LSB |
| 0 | 100,100 | Zero scale |

Typical device-to-device matching is process-lot dependent and may vary by up to ±20%. Because the resistance element is processed in thin film technology, the change in $R_{AB}$ with temperature has a very low 35 ppm/°C temperature coefficient.

# AD5165

## PROGRAMMING THE POTENTIOMETER DIVIDER
### Voltage Output Operation

The digital potentiometer easily generates a voltage divider at wiper-to-B and wiper-to-A proportional to the input voltage at A to B. Unlike the polarity of $V_{DD}$ to GND, which must be positive, voltage across A to B, W to A, and W to B can be at either polarity.
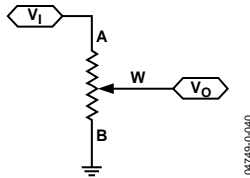
*Figure 38. Potentiometer Mode Configuration*

If ignoring the effect of the wiper resistance for approximation, connecting the A terminal to 5 V and the B terminal to ground produces an output voltage at the wiper-to-B starting at 0 V up to 1 LSB less than 5 V. Each LSB of voltage is equal to the voltage applied across terminals A and B divided by the 256 positions of the potentiometer divider. The general equation defining the output voltage at $V_W$ with respect to ground for any valid input voltage applied to terminals A and B is

$$V_W(D) = \frac{D}{256}V_A + \frac{256 - D}{256}V_B \qquad (3)$$

A more accurate calculation, which includes the effect of wiper resistance, $V_W$, is

$$V_W(D) = \frac{R_{WB}(D)}{R_{AB}}V_A + \frac{R_{WA}(D)}{R_{AB}}V_B \qquad (4)$$

Operation of the digital potentiometer in the divider mode results in a more accurate operation over temperature. Unlike the rheostat mode, the output voltage is dependent mainly on the ratio of the internal resistors $R_{WA}$ and $R_{WB}$ and not the absolute values. Therefore, the temperature drift reduces to 15 ppm/°C.

## 3-WIRE SERIAL BUS DIGITAL INTERFACE

The AD5165 contains a 3-wire digital interface (SDI, CS, and CLK). The 8-bit serial word must be loaded MSB first. The format of the word is shown in Table 5.

The positive-edge sensitive CLK input requires clean transitions to avoid clocking incorrect data into the serial input register. Standard logic families work well. If mechanical switches are used for product evaluation, they should be debounced by a flip-flop or other suitable means. When CS is high, the clock loads data into the serial register on each positive clock edge, as shown in Figure 34.

The data setup and data hold times in the specifications table determine the valid timing requirements. The AD5165 uses an 8-bit serial input data register word that is transferred to the internal RDAC register when the CS line returns to logic low. Extra MSB bits are ignored.

## ESD PROTECTION

All digital inputs are protected with a series of input resistors and parallel Zener ESD structures, shown in Figure 39 and Figure 40. This applies to the digital input pins SDI, CLK, and CS.
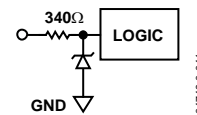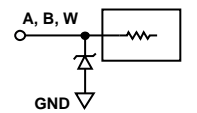
*Figure 39. ESD Protection of Digital Pins*

*Figure 40. ESD Protection of Resistor Terminals*

## TERMINAL VOLTAGE OPERATING RANGE

The AD5165 $V_{DD}$ and GND power supply defines the boundary conditions for proper 3-terminal digital potentiometer operation. Supply signals present on terminals A, B, and W that exceed $V_{DD}$ or GND are clamped by the internal forward-biased diodes, as shown in Figure 41.
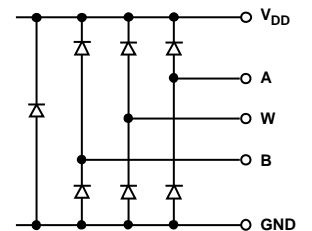
*Figure 41. Maximum Terminal Voltages Set by $V_{DD}$ and GND*

## POWER-UP SEQUENCE

Because the ESD protection diodes limit the voltage compliance at terminals A, B, and W (see Figure 41), it is important to power $V_{DD}$/GND before applying any voltage to terminals A, B, and W; otherwise, the diode is forward biased such that $V_{DD}$ is powered unintentionally and may affect the rest of the user's circuit. The ideal power-up sequence is in the following order: GND, $V_{DD}$, digital inputs, and then $V_A$, $V_B$, and $V_W$. The relative order of powering $V_A$, $V_B$, $V_W$, and the digital inputs is not important as long as they are powered after $V_{DD}$/GND.

## LAYOUT AND POWER SUPPLY BYPASSING

It is good practice to employ compact, minimum lead length layout design. The leads to the inputs should be as direct as possible with a minimum conductor length. Ground paths should have low resistance and low inductance.

Similarly, it is also good practice to bypass the power supplies with quality capacitors for optimum stability. Supply leads to the device should be bypassed with disk or chip ceramic capacitors of 0.01 μF to 0.1 μF. Low ESR 1 μF to 10 μF tantalum or electrolytic capacitors should also be applied at the supplies to minimize any transient disturbance and low frequency ripple (see Figure 42). Note that the digital ground should also be joined remotely to the analog ground at one point to minimize the ground bounce.
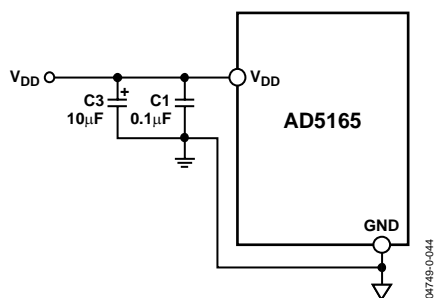
*Figure 42. Power Supply Bypassing*

## EVALUATION BOARD

An evaluation board, along with all necessary software, is available to program the AD5165 from any PC running Windows® 98/2000/XP. The graphical user interface, as shown in Figure 43, is straightforward and easy to use. More detailed information is available in the user manual, which comes with the board.
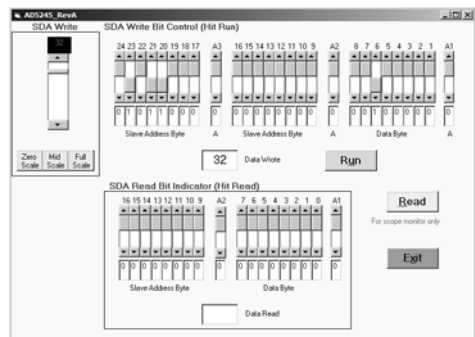
*Figure 43. AD5165 Evaluation Board Software*

The AD5165 starts at midscale upon power-up. To increment or decrement the resistance, the user may move the scroll bars on the left. To write any specific value, the user should use the bit pattern in the upper screen and click the Run button. The format of writing data to the device is shown in Figure 32.
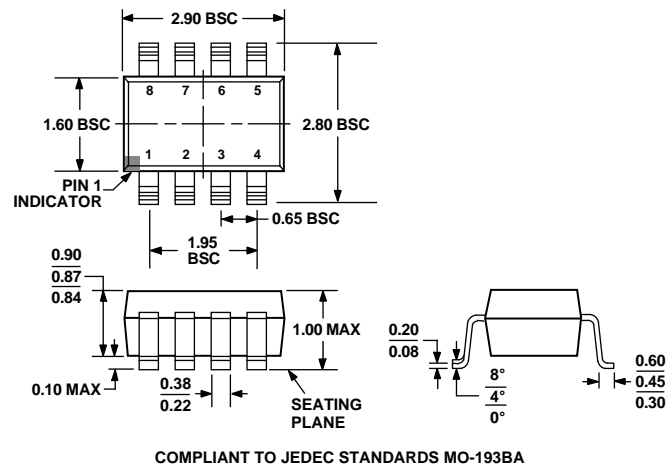
# OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-193BA

*Figure 44. 8-Lead Thin Small Outline Transistor Package [Thin SOT-23]*
*(UJ-8)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model | $R_{AB}$ (Ω) | Temperature | Package Description | Package Option | Quantity on Reel | Branding |
|---|---|---|---|---|---|---|
| AD5165BUJZ100-R2[1] | 100 k | −40°C to +125°C | Thin SOT-23 | UJ-8 | 250 | D3N |
| AD5165BUJZ100-R7[1] | 100 k | −40°C to +125°C | Thin SOT-23 | UJ-8 | 3,000 | D3N |
| AD5165EVAL | | | Evaluation Board | | | |

[1] Z = Pb-free part.

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