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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—SOIC PACKAGE

V_{CB} = 15 V, I_O = 10 μA, T_A = 25°C, unless otherwise specified.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DC AND AC CHARACTERISTICS						
Current Gain[1]	h_{FE}					
		I_C = 1 mA	300	605		
		−40°C ≤ T_A ≤ +85°C	300			
		I_C = 10 μA	200	550		
		−40°C ≤ T_A ≤ +85°C	200			
Current Gain Match[2]	Δh_{FE}	10 μA ≤ I_C ≤ 1 mA		0.5	5	%
Noise Voltage Density[3]	e_N	I_C = 1 mA, V_{CB} = 0 V				
		f_O = 10 Hz		1.6	2	nV/√Hz
		f_O = 100 Hz		0.9	1	nV/√Hz
		f_O = 1 kHz		0.85	1	nV/√Hz
		f_O = 10 kHz		0.85	1	nV/√Hz
Low Frequency Noise (0.1 Hz to 10 Hz)	e_N p-p	I_C = 1 mA		0.4		μV p-p
Offset Voltage	V_{OS}	V_{CB} = 0 V, I_C = 1 mA		10	200	μV
		−40°C ≤ T_A ≤ +85°C			220	μV
Offset Voltage Change vs. V_{CB}	$\Delta V_{OS}/\Delta V_{CB}$	0 V ≤ V_{CB} ≤ V_{MAX}[4], 1 μA ≤ I_C ≤ 1 mA[5]		10	50	μV
Offset Voltage Change vs. I_C	$\Delta V_{OS}/\Delta I_C$	1 μA ≤ I_C ≤ 1 mA[5], V_{CB} = 0 V		5	70	μV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +85°C		0.08	1	μV/°C
		−40°C ≤ T_A ≤ +85°C, V_{OS} trimmed to 0 V		0.03	0.3	μV/°C
Breakdown Voltage	BV_{CEO}		40			V
Gain Bandwidth Product	f_T	I_C = 10 mA, V_{CE} = 10 V		200		MHz
Collector-to-Base Leakage Current	I_{CBO}	V_{CB} = V_{MAX}		25	500	pA
		−40°C ≤ T_A ≤ +85°C		3		nA
Collector-to-Collector Leakage Current	I_{CC}	V_{CC} = V_{MAX}[6, 7]		35	500	pA
		−40°C ≤ T_A ≤ +85°C		4		nA
Collector-to-Emitter Leakage Current	I_{CES}	V_{CE} = V_{MAX}, V_{BE} = 0 V[6, 7]		35	500	pA
		−40°C ≤ T_A ≤ +85°C		4		nA
Input Bias Current	I_B	I_C = 10 μA			50	nA
		−40°C ≤ T_A ≤ +85°C			50	nA
Input Offset Current	I_{OS}	I_C = 10 μA			6.2	nA
		−40°C ≤ T_A ≤ +85°C			13	nA
Input Offset Current Drift	$\Delta I_{OS}/\Delta T$	I_C = 10 μA[6], −40°C ≤ T_A ≤ +85°C		40	150	pA/°C
Collector Saturation Voltage	$V_{CE (SAT)}$	I_C = 1 mA, I_B = 100 μA		0.05	0.2	V
Output Capacitance	C_{OB}	V_{CB} = 15 V, I_E = 0 μA		23		pF
Bulk Resistance	R_{BE}	10 μA ≤ I_C ≤ 10 mA[6]		0.3	1.6	Ω
Collector-to-Collector Capacitance	C_{CC}	V_{CC} = 0 V		35		pF

[1] Current gain is guaranteed with collector-to-base voltage (V_{CB}) swept from 0 V to V_{MAX} at the indicated collector currents.
[2] Current gain match (Δh_{FE}) is defined as follows: $\Delta h_{FE} = (100(\Delta I_B)(h_{FE\ min})/I_C)$.
[3] Noise voltage density is guaranteed, but not 100% tested.
[4] This is the maximum change in V_{OS} as V_{CB} is swept from 0 V to 40 V.
[5] Measured at I_C = 10 μA and guaranteed by design over the specified range of I_C.
[6] Guaranteed by design.
[7] I_{CC} and I_{CES} are verified by measurement of I_{CBO}.

ELECTRICAL CHARACTERISTICS—LFCSP PACKAGE

V_{CB} = 15 V, I_O = 100 μA, T_A = 25°C, unless otherwise specified.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DC AND AC CHARACTERISTICS						
Current Gain[1]	h_{FE}					
		I_C = 1 mA, V_{CB} = 15 V	300	1800	2400	
		I_C = 1 mA, V_{CB} = 0 V	200	1300	2200	
		I_C = 100 μA, V_{CB} = 15 V	350	2100	2500	
		I_C = 100 μA, V_{CB} = 0 V	250	1500	2300	
Current Gain Match[2]	Δh_{FE}	100 μA ≤ I_C ≤ 1 mA		0.5	5	%
Noise Voltage Density[3]	e_N	I_C = 1 mA, V_{CB} = 0 V				
		f_O = 10 Hz		1.6	2	nV/√Hz
		f_O = 100 Hz		0.9	1	nV/√Hz
		f_O = 1 kHz		0.85	1	nV/√Hz
		f_O = 10 kHz		0.85	1	nV/√Hz
Low Frequency Noise (0.1 Hz to 10 Hz)	e_N p-p	I_C = 1 mA		0.4		μV p-p
Offset Voltage	V_{OS}	V_{CB} = 0 V, I_C = 1 mA		25	250	μV
		V_{CB} = 0 V, I_C = 100 μA		10	250	μV
Gain Bandwidth Product	f_T	I_C = 10 mA, V_{CE} = 10 V		200		MHz
Input Bias Current	I_B	I_C = 100 μA			200	nA
Input Offset Current	I_{OS}	I_C = 100 μA			10	nA
Output Capacitance	C_{OB}	V_{CB} = 15 V, I_E = 0 μA		23		pF
Collector-to-Collector Capacitance	C_{CC}	V_{CC} = 0 V		35		pF

[1] Current gain is guaranteed with collector-to-base voltage (V_{CB}) swept from 0 V to V_{MAX} at the indicated collector currents.
[2] Current gain match (Δh_{FE}) is defined as follows: $\Delta h_{FE} = (100(\Delta I_B)(h_{FE\,min})/I_C)$.
[3] Noise voltage density is guaranteed, but not 100% tested.

ABSOLUTE MAXIMUM RATING

Table 3.

Parameter	Rating
Breakdown Voltage of Collector-to-Base Voltage (BV_{CBO})	40 V
Breakdown Voltage of Collector-to-Emitter Voltage (BV_{CEO})	40 V
Breakdown Voltage of Collector-to-Collector Voltage (BV_{CC})	40 V
Breakdown Voltage of Emitter-to-Emitter Voltage (BV_{EE})	40 V
Collector Current (I_C)	20 mA
Emitter Current (I_E)	20 mA
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC (R-8)	120	45	°C/W
16-Lead LFCSP (CP-16-22)	75	4.4	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{CE} = 5 V, unless otherwise specified.

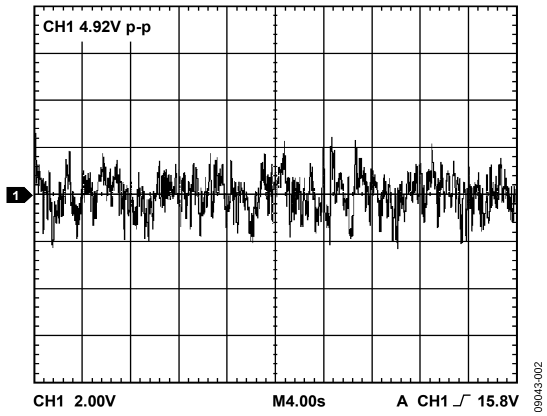

Figure 3. Low Frequency Noise (0.1 Hz to 10 Hz), I_C = 1 mA, Gain = 10,000,000

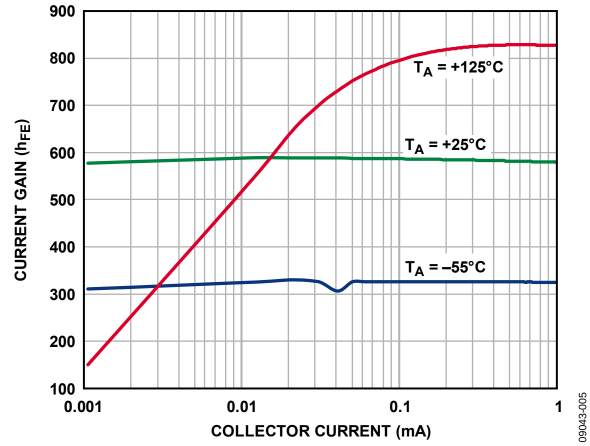

Figure 6. Current Gain vs. Collector Current (V_{CB} = 0 V)

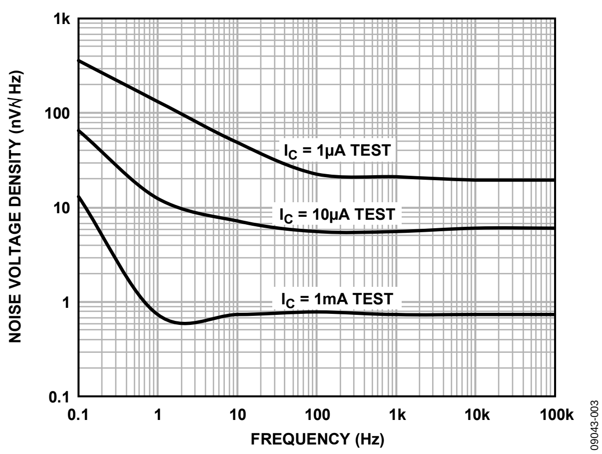

Figure 4. Noise Voltage Density vs. Frequency

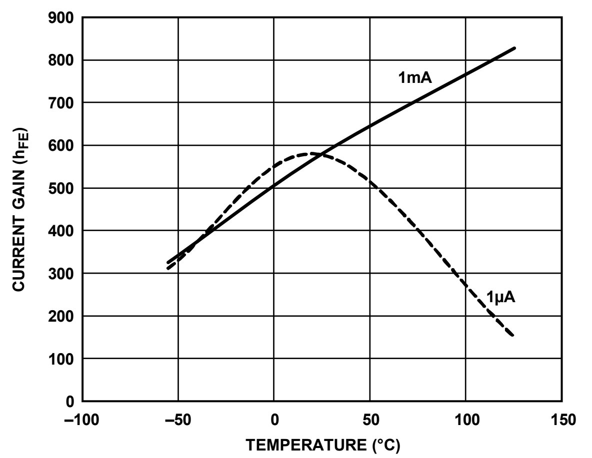

Figure 7. Current Gain vs. Temperature (Excludes I_{CBO})

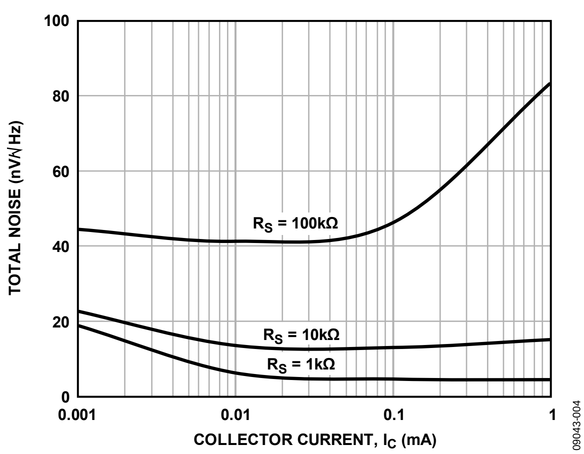

Figure 5. Total Noise vs. Collector Current, f = 1 kHz

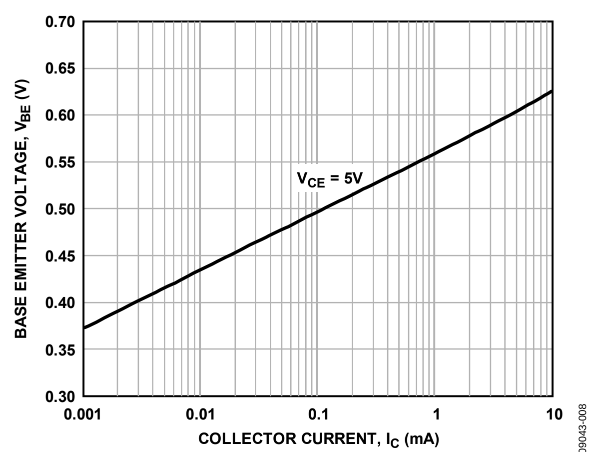

Figure 8. Base Emitter Voltage vs. Collector Current

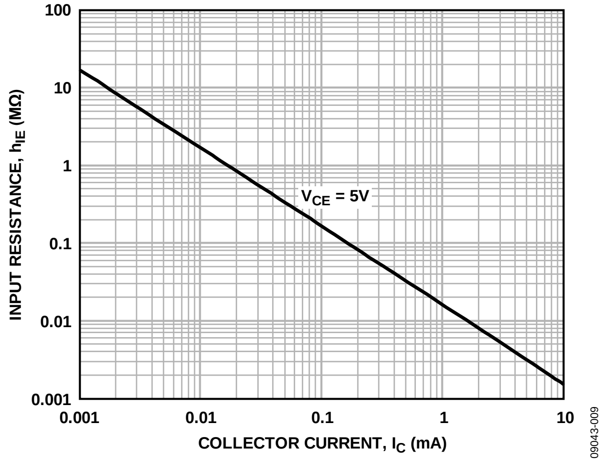

Figure 9. Small Signal Input Resistance vs. Collector Current

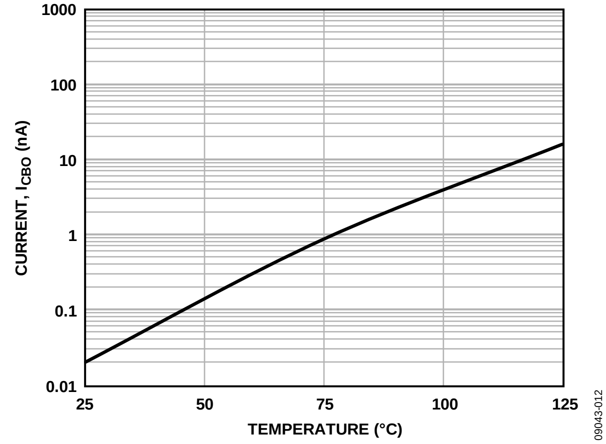

Figure 12. Collector-to-Base Leakage Current vs. Temperature

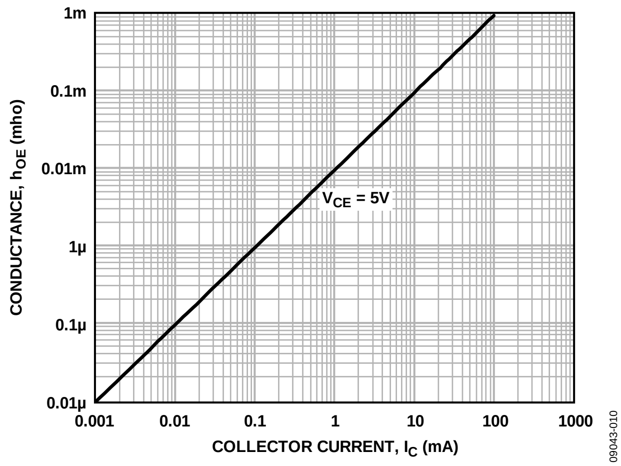

Figure 10. Small Signal Output Conductance vs. Collector Current

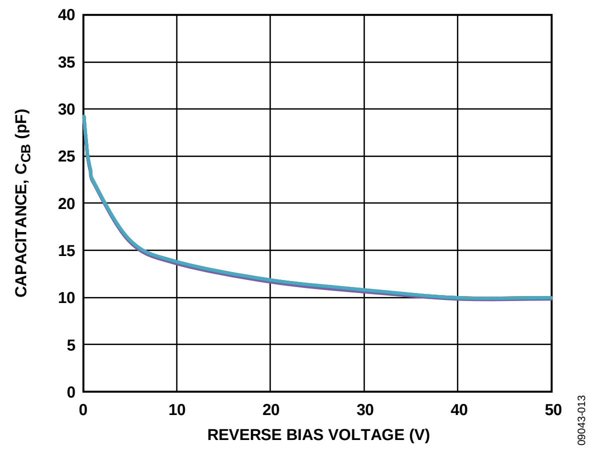

Figure 13. Collector-to-Base Capacitance vs. Reverse Bias Voltage

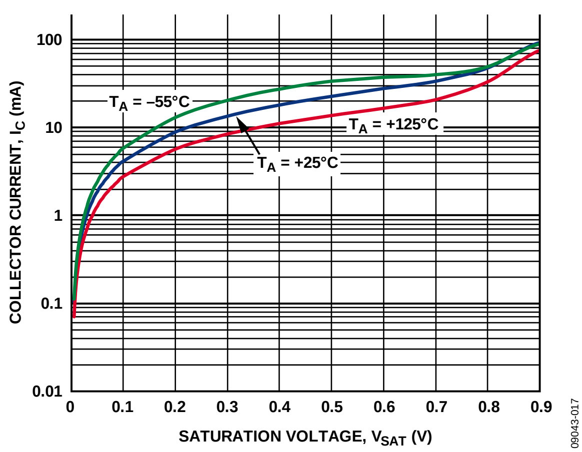

Figure 11. Collector Current vs. Saturation Voltage

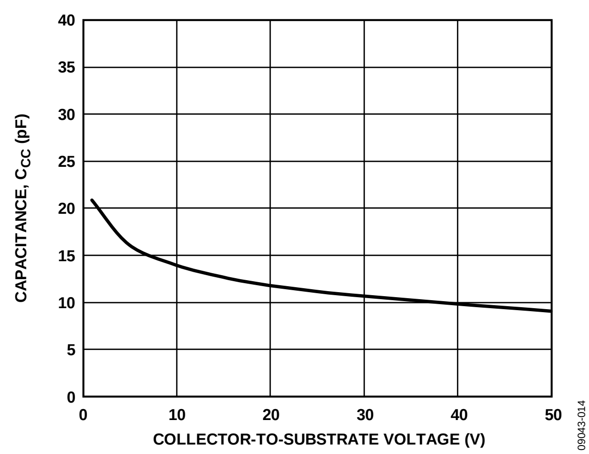

Figure 14. Collector-to-Collector Capacitance vs. Collector-to-Substrate Voltage

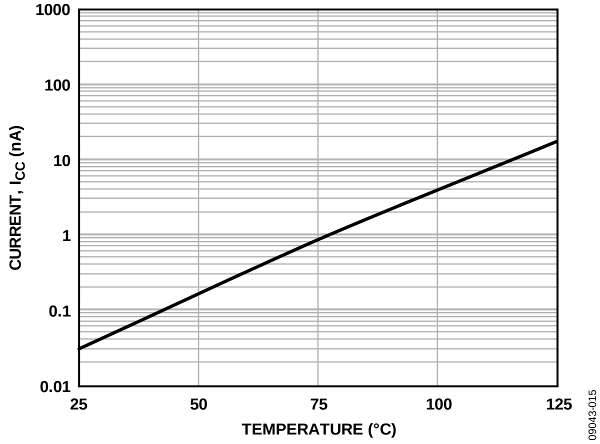

Figure 15. Collector-to-Collector Leakage Current vs. Temperature

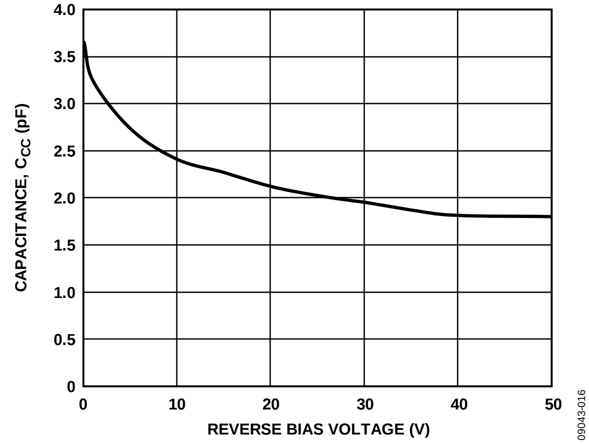

Figure 16. Collector-to-Collector Capacitance vs. Reverse Bias Voltage

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

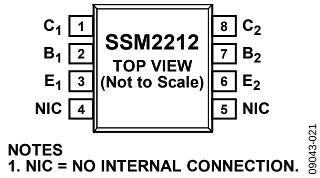

Figure 17. SOIC Pin Configuration

Table 5. SOIC Pin Function Descriptions

Pin No.	Mnemonic	Description
1	C_1	Collector of Channel 1.
2	B_1	Base of Channel 1.
3	E_1	Emitter of Channel 1.
4, 5	NIC	No Internal Connection.
6	E_2	Emitter of Channel 2.
7	B_2	Base of Channel 2.
8	C_2	Collector of Channel 2.

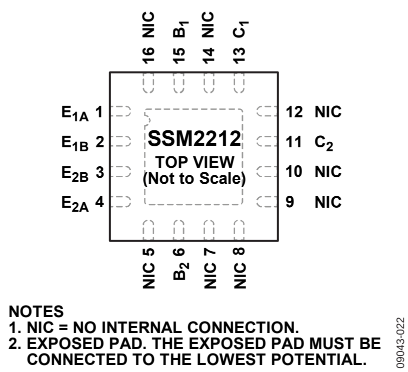

Figure 18. LFCSP Pin Configuration

Table 6. LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	E_{1A}	Emitter of Channel 1. Must be connect to E_{1B}.
2	E_{1B}	Emitter of Channel 1. Must be connect to E_{1A}.
3	E_{2B}	Emitter of Channel 2. Must be connect to E_{2A}.
4	E_{2A}	Emitter of Channel 2. Must be connect to E_{2B}.
5, 7, 8, 9, 10, 12, 14, 16	NIC	No Internal Connection.
6	B_2	Base of Channel 2.
11	C_2	Collector of Channel 2.
13	C_1	Collector of Channel 1.
15	B_1	Base of Channel 1.
	EPAD	Exposed Pad. The exposed pad must be connected to the lowest potential.

APPLICATIONS INFORMATION

FAST LOGARITHMIC AMPLIFIER

The circuit in Figure 19 is a modification of a standard logarithmic amplifier configuration. Running the SSM2212 at 2.5 mA per side (full scale) allows a fast response with a wide dynamic range. The circuit has a 7 decade current range and a 5 decade voltage range, and it is capable of 2.5 µs settling time to 1% with a 1 V to 10 V step. The output follows the equation:

$$V_O = \frac{R3 + R2}{R2} \frac{kT}{q} \ln \frac{V_{REF}}{V_{IN}}$$

To compensate for the temperature dependence of the kT/q term, a resistor with a positive 0.35%/°C temperature coefficient is chosen for R_2. The output is inverted with respect to the input and is nominally −1 V/decade using the component values indicated.

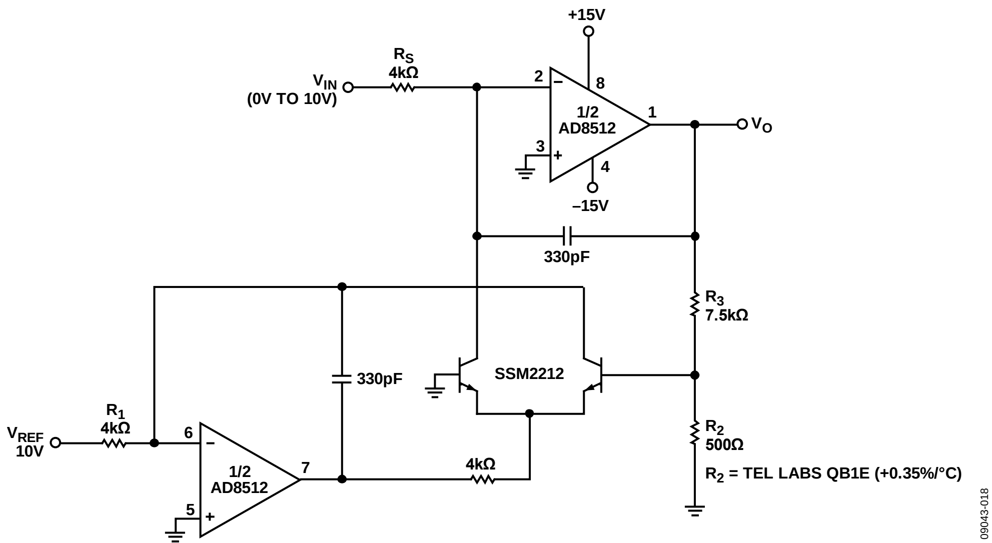

Figure 19. Fast Logarithmic Amplifier

OUTLINE DIMENSIONS

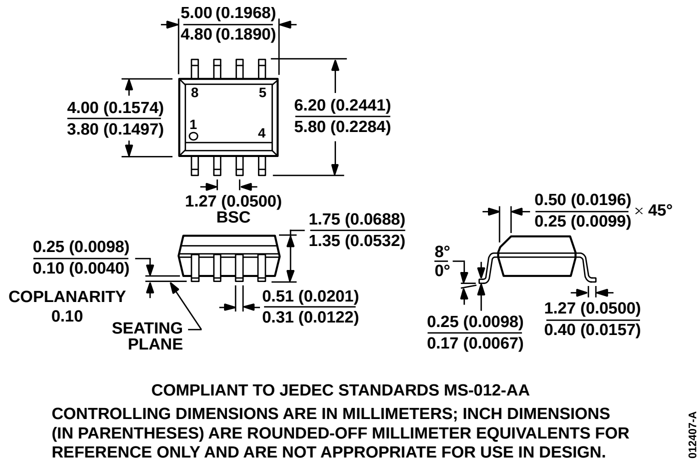

Figure 20. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters (and inches)

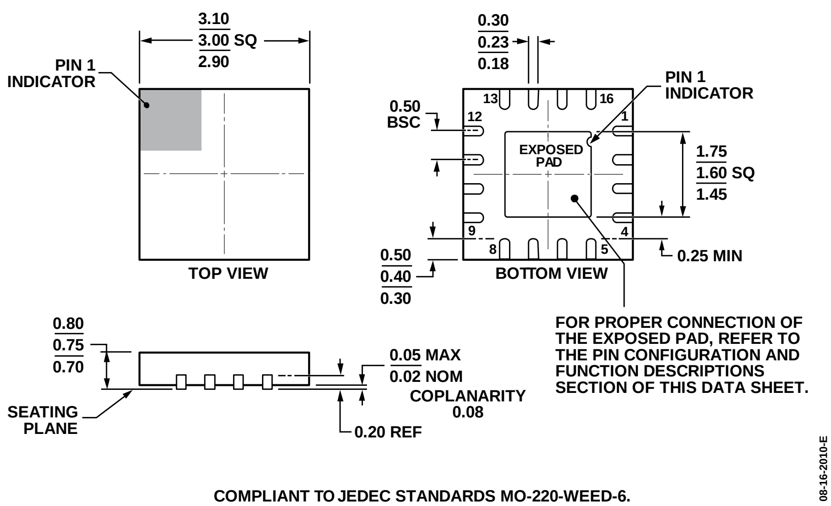

Figure 21. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
3 mm × 3 mm Body, Very Very Thin Quad
(CP-16-22)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
SSM2212RZ	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
SSM2212RZ-R7	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
SSM2212RZ-RL	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
SSM2212CPZ-R7	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-22	A3F
SSM2212CPZ-RL	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-22	A3F

[1] Z = RoHS Compliant Part.

NOTES

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