Complete, 8-Channel, 12-Bit Data-Acquisition Systems

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND ..... -0.3V, +7V
V_{SS} to DGND ..... -0.3V, -17V
AGND to DGND ..... -0.3V, V_{DD} + 0.3V
AIN _, MUXOUT, ADCIN, REFADJ,
OFFADJ to REFIN ..... -0.3V, V_{DD} + 0.3V
REFIN to DGND ..... +0.3V, V_{SS} - 0.3V
CS, WR, RD, CLK, A2-A0,
BIP, DIFF, HBEN to DGND ..... -0.3V, V_{DD} + 0.3V
BUSY, D0-D11 to DGND ..... -0.3V, V_{DD} + 0.3V

Continuous Power Dissipation (any package)
to +70°C 1000mW
derates above +70°C by ..... 10mW/°C
Operating Temperature Ranges:
MAX18 _C _ _ ..... 0°C to +70°C
MAX18 _E _ _ ..... -40°C to +85°C
MAX18 _MJL ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ±5%, V_{SS} = -12V ±5% or -15V ±5%, REFIN = -5V, Internal Reference Mode, Bipolar Mode, Slow-Memory Mode (see text), f_{CLK} = 1.6MHz external, MAX180/MAX181 all grades, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY (Note 2)						
Resolution	N		12			Bits
Integral Nonlinearity Error	INL	MAX18_A			±1/2	LSB
		MAX18_B/C			±1	
Differential Nonlinearity Error	DNL	Guaranteed monotonic over temperature			±1	LSB
Unipolar Offset Error (Note 3)				±1	±4	LSB
Bipolar Offset Error (Note 3)				±1	±6	LSB
Unipolar Gain Error				±2	±10	LSB
Bipolar Gain Errror				±2	±15	LSB
Gain-Error Tempco (Note 4)				±5		ppm/°C
Channel-to-Channel Matching				±1/4		LSB
DYNAMIC PERFORMANCE (Note 2)						
Signal-to-Noise + Distortion Ratio	SINAD	10kHz input signal, 100kHz sampling rate, bipolar mode, T_A = +25°C	70			dB
Total Harmonic Distortion (up to the 5th harmonic)	THD	10kHz input signal, 100kHz sampling rate, bipolar mode, T_A = +25°C			-80	dB
Spurious-Free Dynamic Range	SFDR	10kHz input signal, 100kHz sampling rate, bipolar mode, T_A = +25°C	80			dB
Full-Power Sampling Bandwidth		In track mode, under-sampled waveform		6		MHz
Track-and-Hold Acquisition Time (Note 5)	t_{ACQ}		1.875			µs
Conversion Time	t_{CONV}	Asynchronous hold mode; Note 5	7.500		8.125	µs
		ROM, Slow-Memory, and I/O Port Modes; 15-16 clock cycles	9.375		10.000	
ANALOG INPUT						
Voltage Range		AIN_, MUXOUT, and ADCIN	REFIN		V_{DD}	V
Unipolar, Single-Ended Range		AIN_ to AGND	0		5.0	
Unipolar, Differential Range		AIN_+ to AIN_-	0		5.0	
Bipolar, Single-Ended Range		AIN_ to AGND	-2.5		2.5	
Bipolar, Differential Range		AIN_+ to AIN_-	-2.5		2.5	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±5%, V_{SS} = -12V ±5% or -15V ±5%, REFIN = -5V, Internal Reference Mode, Bipolar Mode, Slow-Memory Mode (see text), f_{CLK} = 1.6MHz external, MAX180/MAX181 all grades, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG INPUT (continued)							
Input Current		AIN_ , MAX180				±1.0	µA
		ADCIN, MAX181				±0.1	
Mux-On Resistance	R_{ON}	AIN_ = 2.5V, I_{MUXOUT} = 1.25mA, MAX181				2	kΩ
Mux-On Leakage Current	I_{ON}	AIN_ = MUXOUT = ±5V, MAX181				±100	nA
Mux-Off Leakage Current	$I_{IN (OFF)}$	AIN_ = ±5V, V_{OUT} = ±5V, MAX181				±100	nA
	$I_{OUT (OFF)}$	AIN_ = ±5V, V_{OUT} = ±5V, MAX181				±100	
Input Capacitance (Note 5)	C_{IN}	AIN_ , ADCIN			25	35	pF
		MUXOUT			35	45	
REFERENCE INPUT							
Input Range (Note 5)				-4.92	-5.00	-5.08	V
Input Current						-2	mA
Input Resistance				2.5			kΩ
REFERENCE OUTPUT							
VREF Output Voltage		T_A = +25°C		-4.98	-5.00	-5.02	V
VREF Output Tempco (Note 6)		MAX18_A/B				25	ppm/°C
		MAX18_C				45	
VREF Load Regulation (Note 7)		I_{OUT} = 0mA to 5mA, T_A = +25°C			0.2	1.0	mV/mA
REFADJ, OFFADJ							
Input Current		V_{REFADJ}, V_{OFFADJ} = V_{DD} to REFIN				±1	µA
Disable Threshold				4.5			V
REFADJ Adjustment Range		REFIN < REFADJ <AGND		±60	±80		mV
OFFADJ Adjustment Range		REFIN < OFFADJ <AGND		±15	±25		LSB
LOGIC INPUTS							
Input Low Voltage	V_{IL}	MODE				0.5	V
		$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, CLK, A2-A0, DIFF, BIP, HBEN				0.8	
Input High Voltage	V_{IH}	MODE		4.5			V
		$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, CLK, A2-A0, DIFF, BIP, HBEN		2.4			
Input Mid-Level Voltage	V_{MID}	MODE		1.5		3.5	V
Input Floating Voltage	V_{FLT}	MODE			2.5		V
Input Current	I_{IN}	MODE	T_A = +25°C		±50	±100	µA
			T_A = T_{MIN} to T_{MAX}		±50	±100	
		$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, CLK, A2-A0, DIFF, BIP, HBEN	T_A = +25°C			±1	
			T_A = T_{MIN} to T_{MAX}			±10	
Input Capacitance (Note 5)	C_{IN}					15	pF
LOGIC OUTPUTS							
Output Low Voltage	V_{OL}	D11-D0, $\overline{BUSY}$, RDY, I_{SINK} = 1.6mA				0.4	V
Output High Voltage	V_{OH}	D11-D0, $\overline{BUSY}$, RDY, I_{SOURCE} = 360µA		4.0			V
Floating State Leakage Current	I_{LKG}	D11-D0, V_{OUT} = 0V to V_{DD}				±10	µA
Floating State Output Capacitance (Note 5)	C_{OUT}					15	pF

Complete, 8-Channel, 12-Bit Data-Acquisition Systems

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±5%, V_{SS} = -12V ±5% or -15V ±5%, REFIN = -5V, Internal Reference Mode, Bipolar Mode, Slow-Memory Mode (see text), f_{CLK} = 1.6MHz external, MAX180/MAX181 all grades, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER REQUIREMENTS						
Supply Voltage (Note 1)	V_{DD}		4.75	5.00	5.25	V
	V_{SS}		-11.40		-15.75	
Supply Current	I_{DD}	V_{DD} = 5V		4.5	7.0	mA
	I_{SS}	V_{SS} = -12V		7.0	10.0	
Power Dissipation	PD	V_{DD} = 5V, VSS = -15V		110	155	mW
Power-Supply Rejection, with Internal Reference	PSR	Input near FS, V_{SS} = -12V, V_{DD} = 4.75V to 5.25V		±1/2	±1	LSB
		Input near FS, V_{DD} = 5V, V_{SS} = -14.25V to -15.75V		±1/8	±1/2	
		Input near FS, V_{DD} = 5V, V_{SS} = -11.4V to = -12.6V		±1/8	±1/2	

TIMING CHARACTERISTICS

(V_{DD} = +5V, V_{SS} = -12V, f_{CLK} = 1.6MHz, Internal Reference Mode, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 8)

PARAMETER	SYMBOL	CONDITIONS		T_A = +25°C			MAX18_C/E			MAX18_M			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$\overline{CS}$ to $\overline{RD}$ Setup time	t_1		Note 5	0			0			0			ns
$\overline{CS}$ to $\overline{RD}$ Hold time	t_2			0			0			0			ns
$\overline{CS}$ to $\overline{WR}$ Setup time	t_3			0			0			0			ns
$\overline{CS}$ to $\overline{WR}$ Hold time	t_4		Note 5	0			0			0			ns
$\overline{WR}$ Low Pulse Width	t_5			120			120			120			ns
$\overline{WR}$ High Pulse Width	t_6	MODE = 0 or 1	Note 5	200			200			200			ns
DATA IN to $\overline{WR}$ Setup Time	t_7			80			100			120			ns
DATA IN to $\overline{WR}$ Hold Time	t_8			0			0			0			ns
$\overline{WR}$ Rising to $\overline{BUSY}$ Delay	t_9	C_L = 50pF, MODE = 1				160			180			200	ns
$\overline{WR}$ Falling to $\overline{BUSY}$ Delay	t_{10}	C_L = 50pF, MODE = open				220			260			280	ns
$\overline{RD}$ Low Pulse Width	t_{11}			100			130			150			ns
$\overline{RD}$ High Pulse Width	t_{12}		Note 5	200			200			200			ns
DATA IN to $\overline{RD}$ Setup Time	t_{13}			80			100			120			ns
DATA IN to $\overline{RD}$ Hold Time	t_{14}			0			0			0			ns
$\overline{RD}$ to $\overline{BUSY}$ Fall Delay	t_{15}	C_L = 50pF				150			170			200	ns
$\overline{RD}$ to Data out Valid	t_{16}	C_L = 100pF	Note 9		50	100			130			150	ns
$\overline{RD}$ to Data out Three-State	t_{17}		Notes 9, 10		30	50			65			75	ns
HBEN to $\overline{RD}$ or $\overline{WR}$ Setup Time	t_{18}			80			100			120			ns
HBEN to $\overline{RD}$ or $\overline{WR}$ Hold Time	t_{19}			0			0			0			ns
$\overline{CS}$ to $\overline{READY}$ Fall Delay	t_{20}	C_L = 50pF				110			130			150	ns

TIMING CHARACTERISTICS (continued)

(V_{DD} = +5V, V_{SS} = -12V, f_{CLK} = 1.6MHz, Internal Reference Mode, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 8)

PARAMETER	SYMBOL	CONDITIONS		T_A = +25°C MIN	T_A = +25°C TYP	T_A = +25°C MAX	MAX18_C/E MIN	MAX18_C/E TYP	MAX18_C/E MAX	MAX18_M MIN	MAX18_M TYP	MAX18_M MAX	UNITS
$\overline{BUSY}$ to Data Out Valid	t_{21}	C_L = 100pF	Note 9		125			150				170	ns
$\overline{CS}$, $\overline{RD}$, or $\overline{WR}$ to CLK Setup time for 15 clock conversion	t_{22}		Note 5	220			220			220			ns
$\overline{CS}$, RD, or $\overline{WR}$ to CLK Setup time for 16 clock conversion	t_{23}		Note 5	0			0			0			ns

Note 1: Performance at power-supply tolerance limits guaranteed by power-supply rejection test.
Note 2: V_{DD} = +5V, V_{SS} = -15V, FS = +5V, REFIN = -5V.
Note 3: Typical change over temperature is ±1LSB.
Note 4: FS Tempco = ΔFS/ΔT, where ΔFS is full-scale change from T_A = +25°C to T_{MIN} or to T_{MAX}.
Note 5: Guaranteed by design.
Note 6: REFIN TC = ΔREFIN/ΔT, where ΔREFIN is reference voltage change from T_A = +25°C to T_{MIN} or to T_{MAX}
Note 7: Load current should remain constant during conversion. This current is in addition to the DAC input current.
Note 8: All inputs are 0V to +5V swing with t_r = t_f = 5ns (10% to 90% of 5V) and timed from a voltage level of +1.6V.
Note 9: t_{16} and t_{21} are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.
Note 10: t_{17} is defined as the time required for the data lines to change 0.5V when the circuit load is as shown in Figure 2.

Pin Description

NAME	MAX180 DIP	MAX180 PLCC	MAX181 DIP	MAX181 PLCC	FUNCTION
AIN0-AIN5	1-6	2-7	1-6	2-7	Analog Inputs to the mux: 0V to +5V unipolar, -2.5V to +2.5V bipolar
AIN6-AIN7	7,8	8,9			Analog Inputs to the mux: 0V to +5V unipolar, -2.5V to +2.5V bipolar
MUXOUT			7	8	Muliplexer Output
ADCIN			8	9	Analog Input to track-and-hold
REFIN	9	10	9	10	Reference Input
AGND	10	11	10	11	Analog Ground
REFOUT	11	13	11	13	-5V Reference Output
REFADJ	12	14	12	14	-5V Reference Adjust. Connect to V_{DD} if not required.
OFFADJ	13	15	13	15	Offset Adjust. Connect to V_{DD} if not required.
MODE	14	16	14	16	Interface Mode Select pin.
V_{SS}	15	17	15	17	Negative Supply: -15V or -12V
D11-D8	16-19	18-21	16-19	18-21	Three-State Data Outputs, MSB = D11
DGND	20	22	20	22	Digital Ground
D7-D0	21-28	24-31	21-28	24-31	Three-State Data Outputs, LSB = D0
CLKIN	29	32	29	32	Clock Input, TTL/CMOS compatible
HBEN	30	33	30	33	High-Byte Enable Input
$\overline{RD}$	31	35	31	35	$\overline{READ}$ Input
$\overline{WR}$	32	36	32	36	$\overline{WRITE}$ Input (MODE = 1 or Open) $\overline{READY}$ Output (MODE = 0)
$\overline{CS}$	33	37	33	37	$\overline{CHIP\text{-}SELECT}$ Input
$\overline{BUSY}$	34	38	34	38	$\overline{BUSY}$ Output
DIFF	35	39	35	39	Single-Ended Mode: DIFF = 0, Differential Mode: DIFF = 1
BIP	36	40	36	40	Unipolar Mode: BIP = 0, Bipolar Mode: BIP = 1
A0-A2	37-39	41-43	37-39	41-43	Multiplexer Channel Address Input: A2 = MSB, A0 = LSB
V_{DD}	40	44	40	44	Positive Supply: +5V Input (substrate connected to V_{DD})
N.C.		1,12, 23,34		1,12, 23,34	No Connect. No internal connection. Leave pin open or connect to AGND.

Complete, 8-Channel, 12-Bit Data-Acquisition Systems

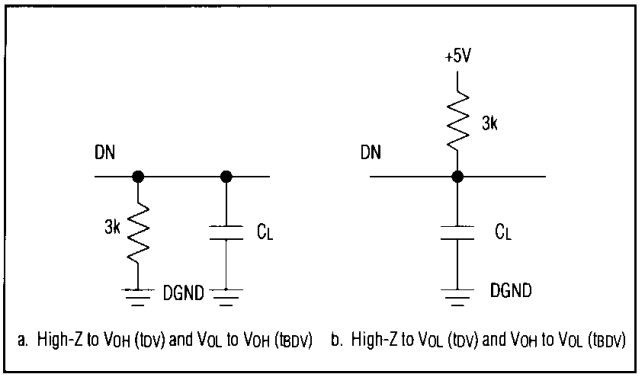

Figure 1. Load Circuits for Access Time

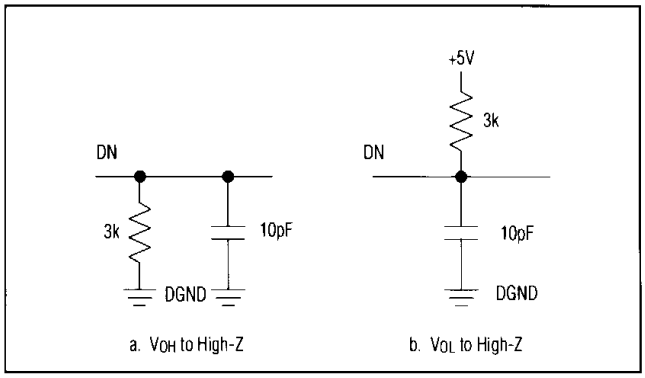

Figure 2. Load Circuits for Bus-Relinquish Time

A/D Converter Operation

The MAX180/MAX181 use successive approximation and input track-and-hold (T/H) circuitry to convert an analog signal to a series of 12-bit digital output codes. The control logic interfaces easily to uPs, requiring only a few passive components for most applications. The T/H does not require an external capacitor. Figure 3 shows the MAX180 typical operating circuit.

Starting a Conversion

Regardless of the mode or interface selected, the following sequence occurs once conversion is started:

1. The data inputs that configure the data-acquisition system (DAS) latch, and the interface signals the µP that a conversion has started.
2. The mux directs the selected input signal to the T/H input.
3. A fixed time delay allows the T/H to acquire the signal. In all modes except asynchronous hold, this delay is 3 clock cycles. In asynchronous hold, the µP controls this delay.
4. The T/H switches to hold mode. The T/H output delivers a stable, single-ended sample of the input signal to the A/D input.
5. The successive approximation cycle begins. The ADC tests and sets each of the 12 bits in turn, from most to least significant. Bit decisions occur on the CLKIN falling edges, for a total of 12 clock cycles.
6. Output data is latched by the output registers, and the interface signals the µP that conversion is complete and data is available.

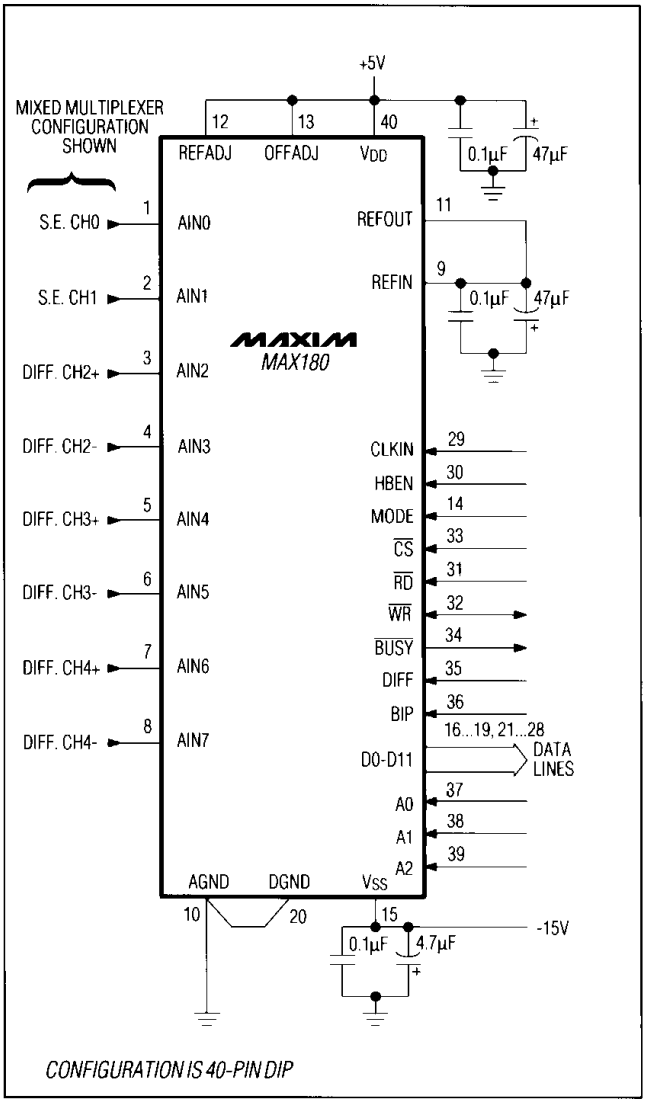

Figure 3. MAX180 Typical Operating Circuit

Analog Input - Track-and-Hold

Figure 4 shows the equivalent input circuit, illustrating the sampling architecture of the ADC's analog comparator. The input capacitance acts as the hold capacitor and is charged by the input signal with every A/D conversion. The capacitance is charged through an internal 1kΩ resistor in series with the input. Note: Figure 4's switches represents both the mux and hold switches.

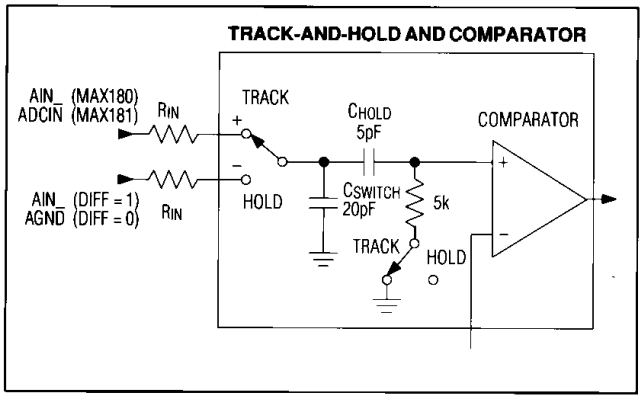

Figure 4. Equivalent Input Circuit

When in single-ended input mode and between conversions ($\overline{BUSY}$ = High), the selected analog input is connected to the hold capacitor (track mode). When a conversion starts, CHOLD disconnects from the + T/H input, thus sampling the input (see "Digital Interface" section for percise T/H timing). When the switch closes at conversion end, CHOLD reconnects to the input and charges to the input signal. The loading effect of the analog inputs on the signal is such that a high-speed input buffer is usually NOT needed because the ADC disconnects from the input during the actual conversion.

The previous explanation applies for the differential input mode if "input" is replaced by AIN+ and "analog ground" is replaced by AIN-. In the differential input mode, A0-A2 select the input channel pairs (Table 1). Only the signal side of the input channel is held by the T/H; the return side must remain stable within ±0.5LSB (±0.1LSB for best results) during the conversion. For example, a common-mode signal of 0.33Vp-p at 60Hz results in a maximum error of 0.5LSB.

The T/H starts tracking when the ADC is deselected ($\overline{BUSY}$ = High). Hold mode begins 3 clock cycles after a conversion is initiated in all but the Asynchronous Hold Mode. Variation in hold-mode delay from one conversion to the next (aperture jitter) is less than 100ps. Figures 7-11 detail the T/H and interface timing for the various interface modes.

The time required for the T/H to acquire an input signal is a function of how quickly the input capacitance is charged. If the input source impedance is high, the acquisition time lengthens and more time must be allowed between conversions. Acquisition time is calculated by:

$$t_{ACQ} = 10(R_S + R_{IN})20pF \text{ (but never less than } 1.875\mu s)$$

where R_{IN} = 1kΩ, and R_S = source impedance of the input signal.

Input Bandwidth

The A/D's input tracking circuitry is excellent for tracking large signals and wide bandwidths and does not exhibit the slew-rate limitations of many other ADC T/Hs. The MAX180/MAX181 T/H's full-power bandwidth is typically 6MHz; this allows the measurement of periodic signals with bandwidths exceeding the ADC's sample rate (100kHz) using under-sampling techniques. Important note: If under-sampling is used to measure high-frequency signals, take special care to avoid aliasing errors. Without adequate input filtering, high-frequency noise could be aliased into the measurement band.

Reference

The MAX180/MAX181 operate with either the internal reference or an external -5V reference. In both cases, REFIN must be bypassed to AGND with a 47µF electrolytic capacitor in parallel with a 0.1µF ceramic capacitor to minimize noise and maintain a low impedance at high frequencies. REFIN is connected directly to the internal DAC, and the current load varies between 0mA and 1mA during conversion.

Internal Reference

The internal reference is buffered through an amplifier whose output connects to REFOUT. To operate the MAX180/MAX181 with the internal reference, connect REFIN to REFOUT. Do not connect a resistor between the bypass capacitors and REFIN. The reference buffer amplifier can sink 5mA for external loads. Adjust the reference output at REFADJ (Figure 14).

External Reference

With a -5V external reference, bypass REFIN to AGND with a 47µF electrolytic capacitor in parallel with a 0.1µF ceramic capacitor. The reference source impedance must be less than 0.2Ω and must be able to sink the internal DAC load of 1mA. Connect REFOUT to V_{SS} and REFADJ to V_{DD} to prevent noise. If REFIN is driven above AGND during power sequencing, latchup can occur. Connect a Schottky clamp diode (IN5817) to prevent REFIN from substantially exceeding AGND.

Complete, 8-Channel, 12-Bit Data-Acquisition Systems

Table 1. Address vs. Channel Selection (see Figure 4)

	A2	A1	A0	$\overline{SE}$/DIFF	AIN0	AIN1	AIN2	AIN3	AIN4	AIN5	AIN6	AIN7	COM
MAX180/MAX181	0	0	0	0	+								–
MAX180/MAX181	0	0	1	0		+							–
MAX180/MAX181	0	1	0	0			+						–
MAX180/MAX181	0	1	1	0				+					–
MAX180/MAX181	1	0	0	0					+				–
MAX180/MAX181	1	0	1	0						+			–
MAX180	1	1	0	0							+		–
MAX181	1	1	0	0		MUXOUT CONNECTED TO AGND							+, –
MAX180	1	1	1	0								+	–
MAX181	1	1	1	0		CH 0-5, AND MUXOUT ARE OPEN							–
MAX180/MAX181	0	0	0	1	+	–							
MAX180/MAX181	0	0	1	1	–	+							
MAX180/MAX181	0	1	0	1			+	–					
MAX180/MAX181	0	1	1	1			–	+					
MAX180/MAX181	1	0	0	1					+	–			
MAX180/MAX181	1	0	1	1					–	+			
MAX180	1	1	0	1							+	–	
MAX180	1	1	1	1							–	+	
MAX181	1	1	0	1		MUXOUT CONNECTED TO AGND							+, –
MAX181	1	1	1	1		CH 0-5, AND MUXOUT ARE OPEN							–

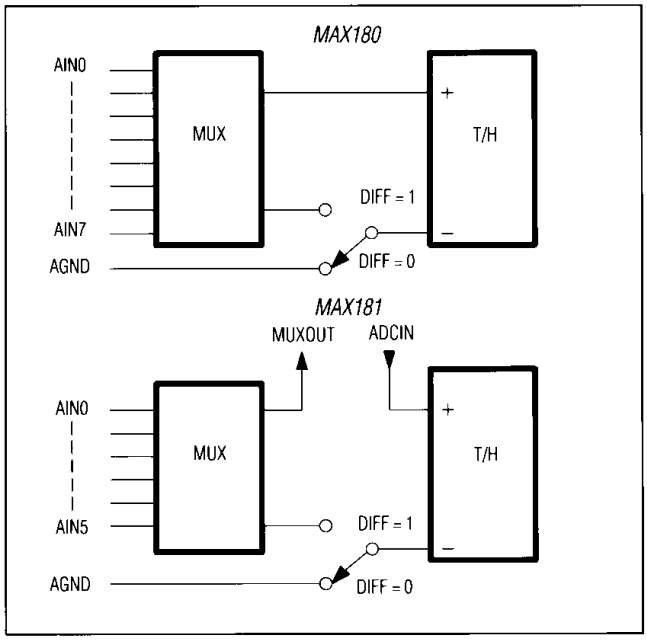

Figure 5. Multiplexer channel configuration

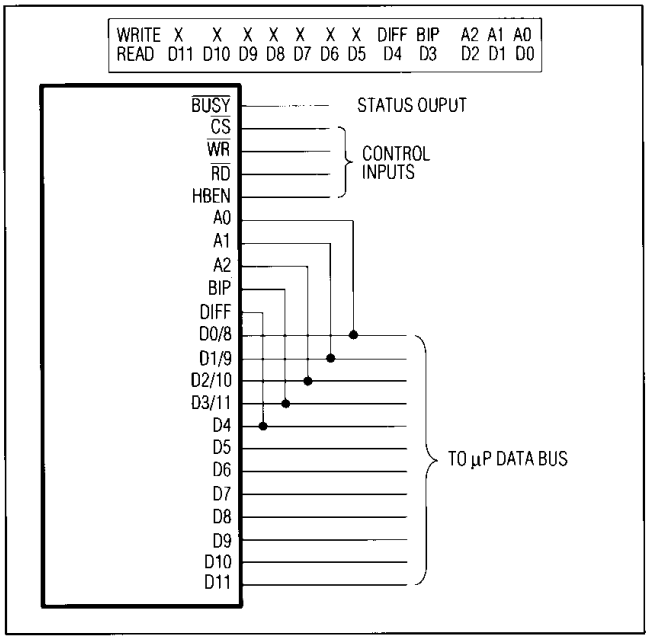

Figure 6. Input/Output Port Mode (12-Bit-Wide Data Bus Shown)

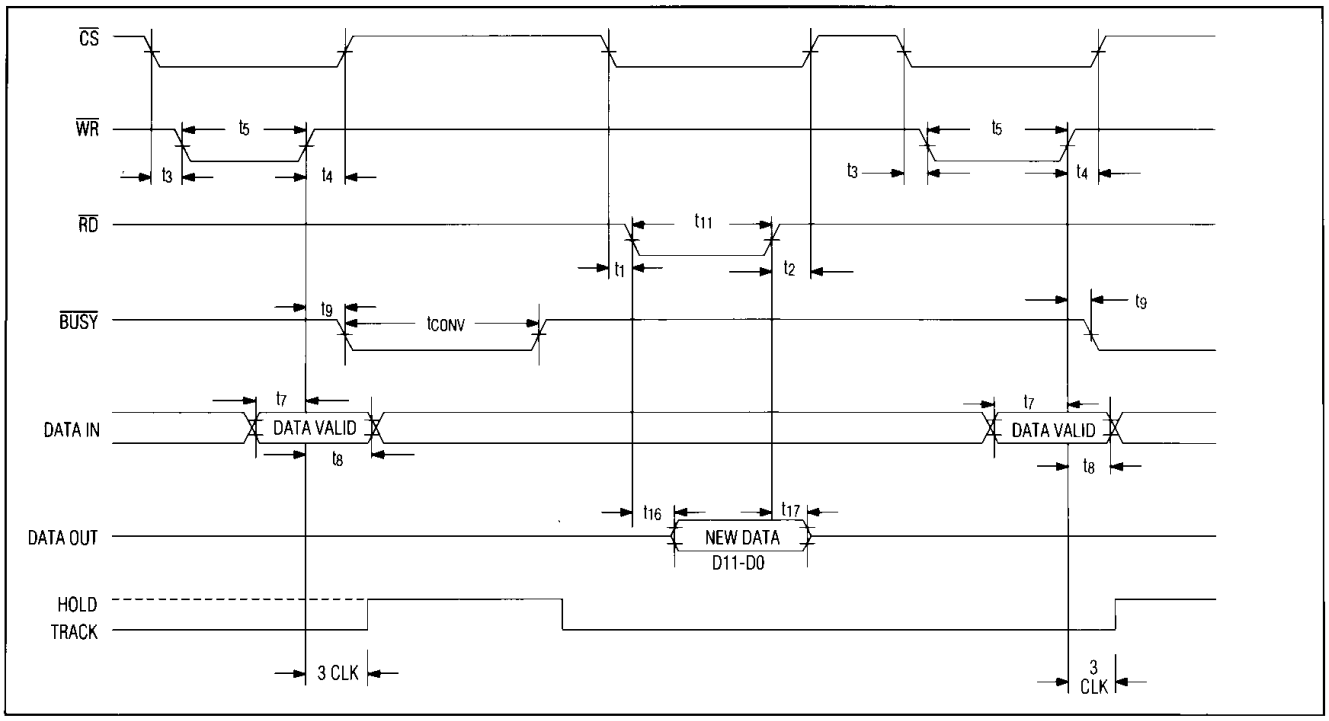

Figure 7a. Input/Output Port-Mode timing, parallel read (MODE = 1, HBEN = 0).

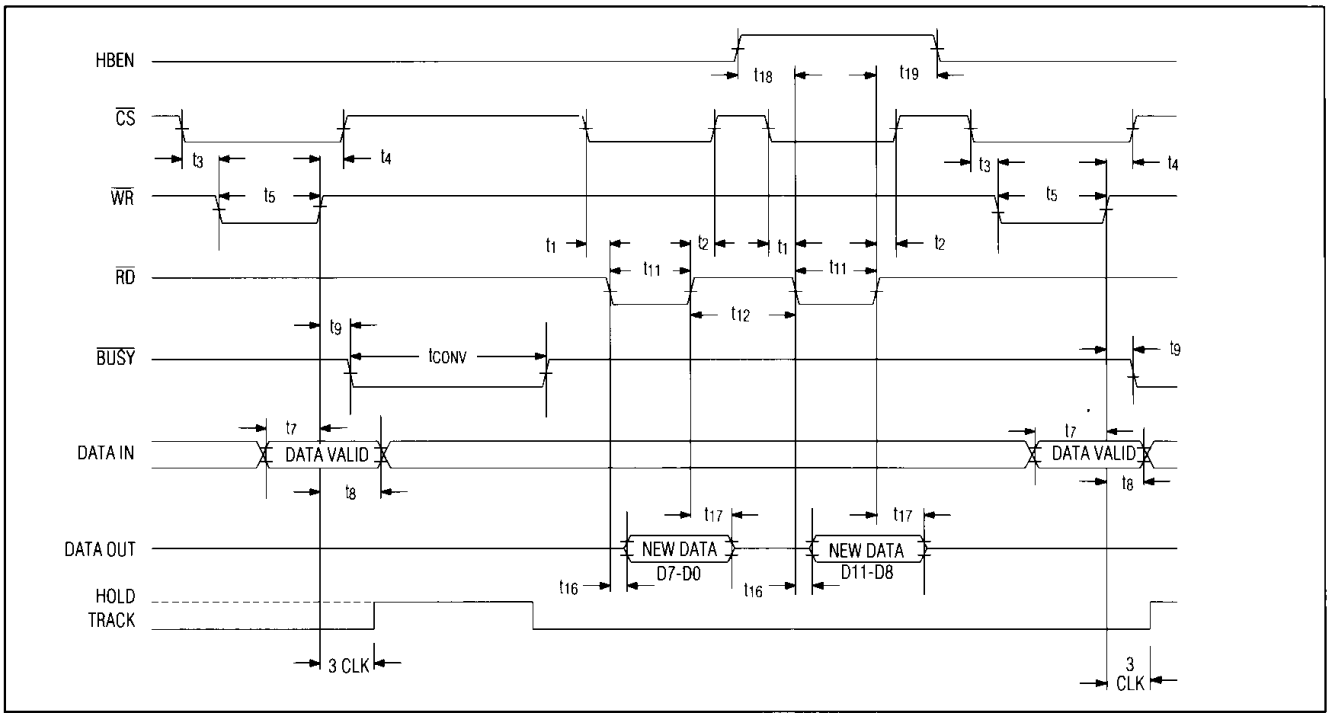

Figure 7b. Input/Output Port-Mode timing, two-byte read (MODE = 1).

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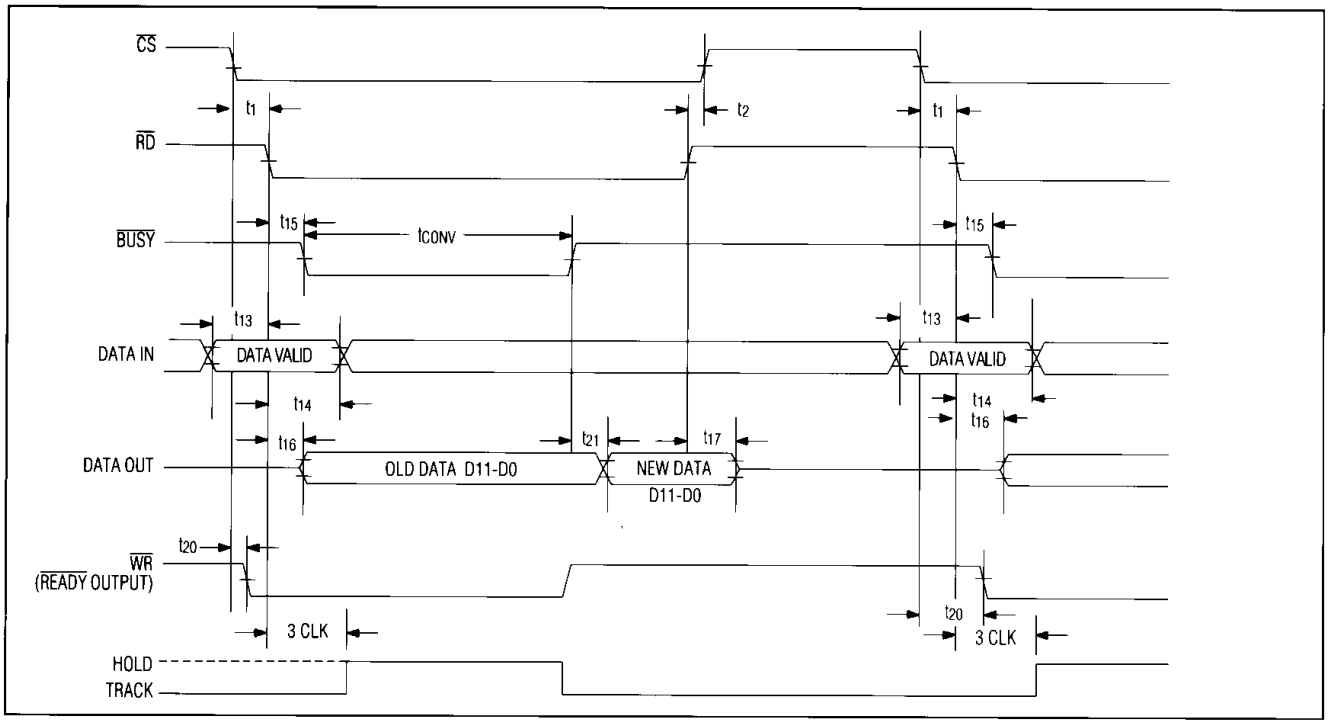

Figure 8a. Slow Memory Mode timing, parallel read (MODE = 0, HBEN = 0).

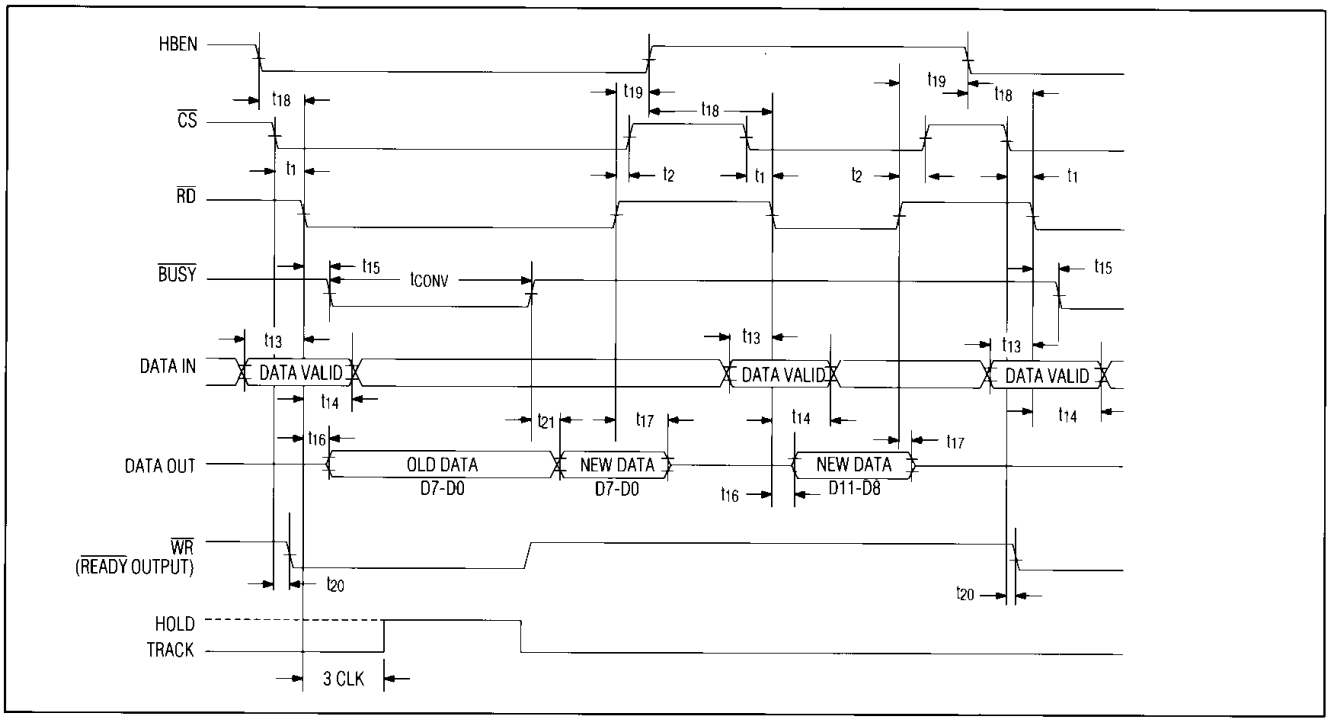

Figure 8b. Slow Memory Mode timing, two-byte read (MODE = 0).

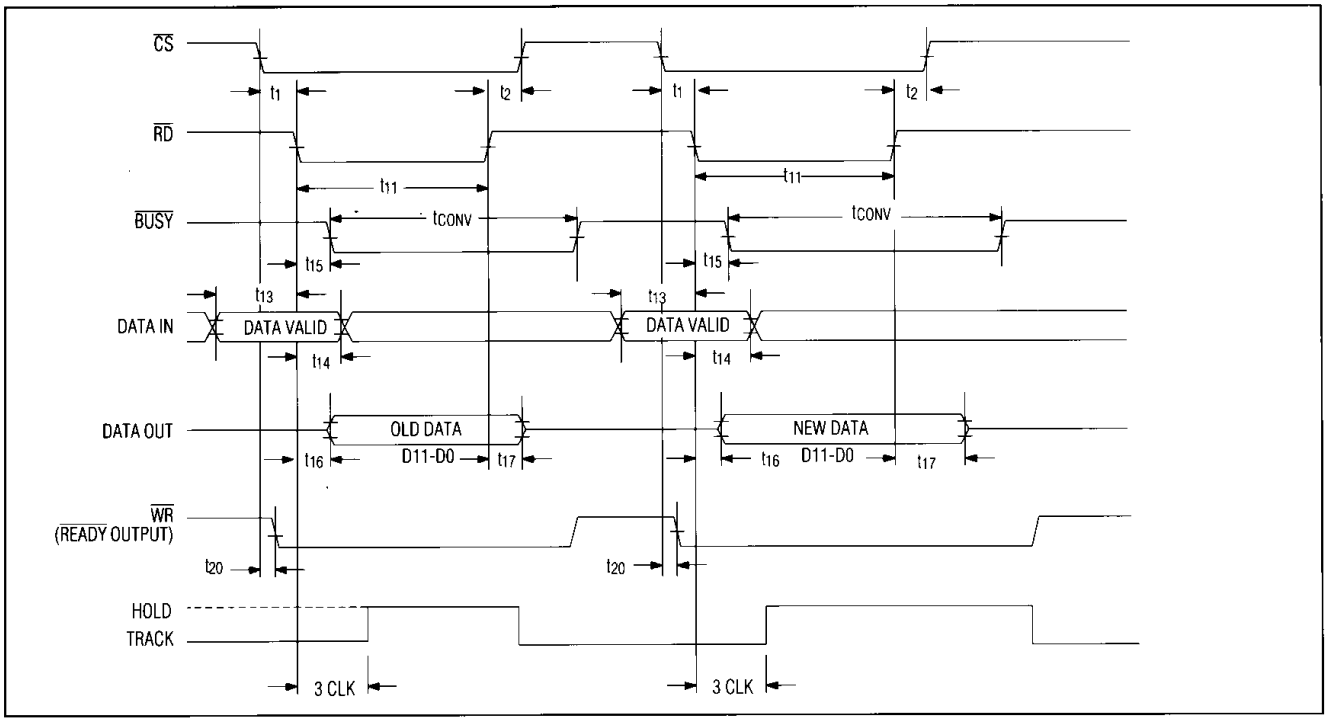

Figure 9a. ROM Mode timing, parallel read (MODE = 0, HBEN = 0).

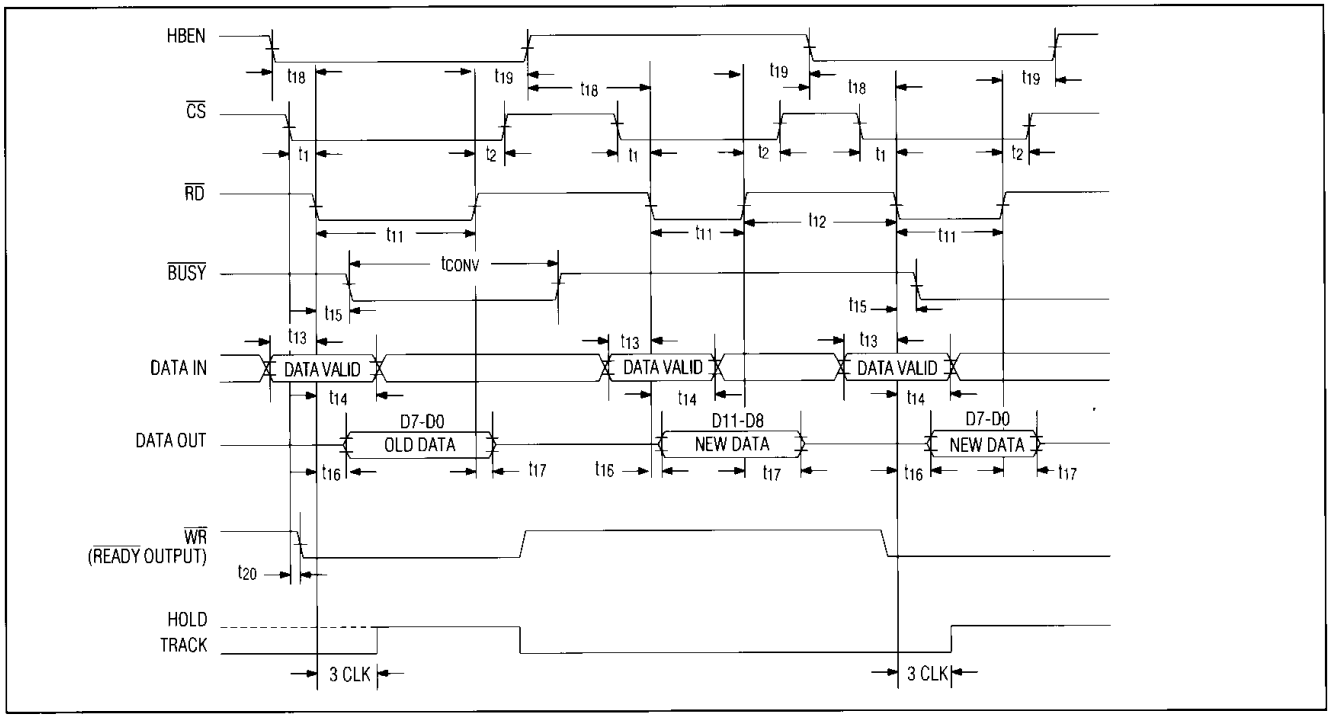

Figure 9b. ROM Mode timing, two-byte read (MODE = 0).

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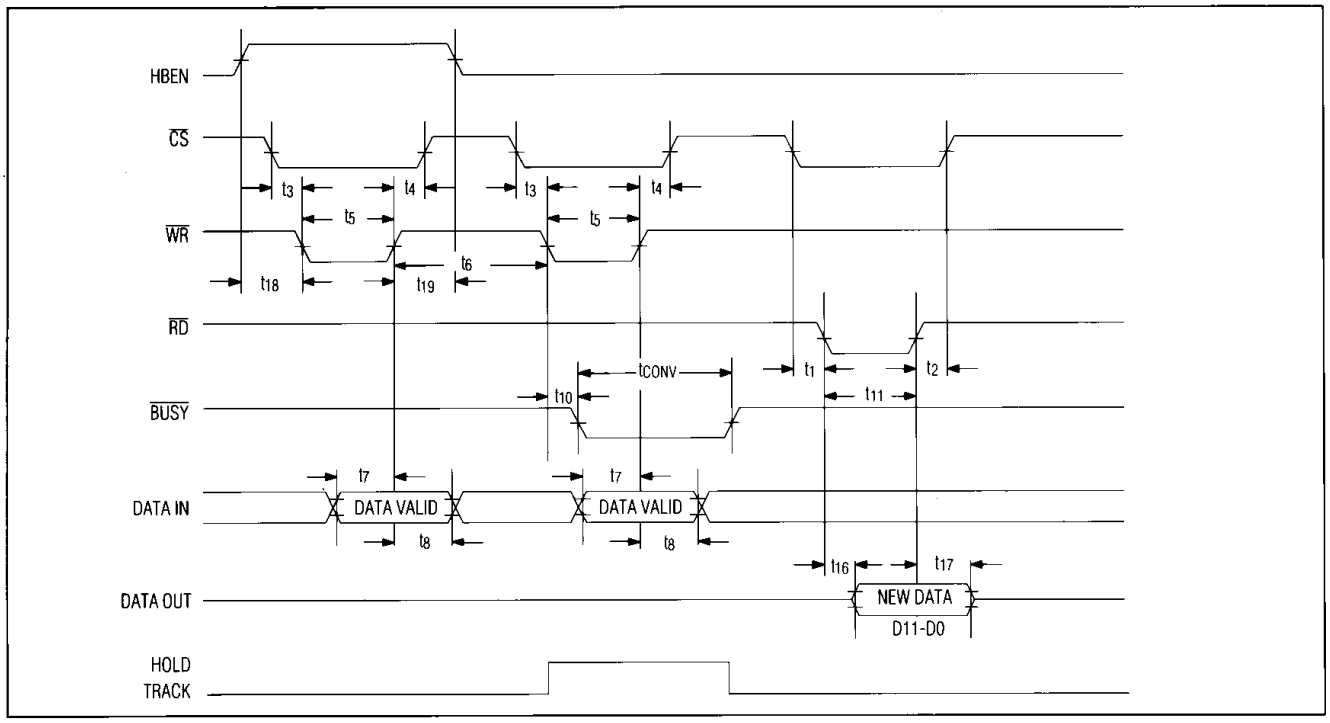

Figure 10a. Asynchronous Hold Mode timing, parallel read (MODE = open circuit)

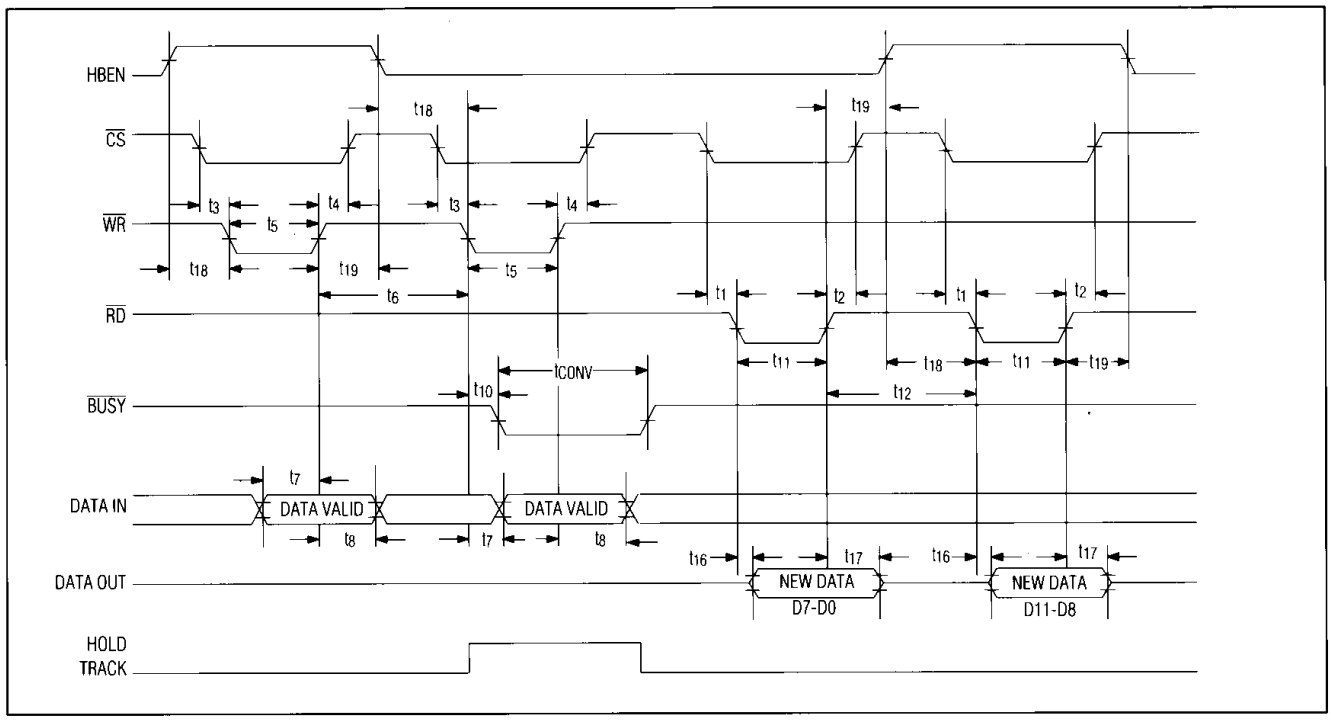

Figure 10b. Asynchronous Hold Mode timing, two-byte read (MODE = open circuit)

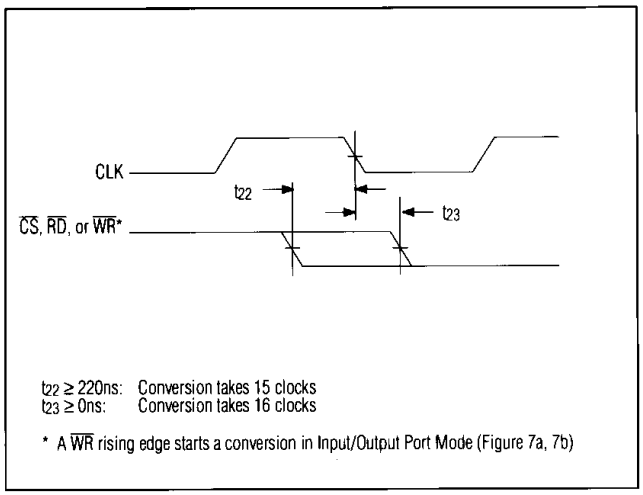

Figure 11. CS, RD, or WR to CLK Setup and Hold Time for Synchronous Operation

Digital Interface

Input/Output Port Mode (MODE = 1)

In this mode, data inputs and outputs are usually connected together (Figure 6), and the µP writes the configuration data to the DAS internal register with a write instruction (Figure 7). This starts a conversion, as indicated by the high-to-low transition of BUSY. The mux connects the selected input channel to the T/H, which acquires the signal during the first 3 clock cycles. On the falling edge of the 3rd clock, the T/H switches to hold mode, and the A/D conversion starts. 15 clock cycles after WR goes high, BUSY goes high, and the conversion result latches into three-state output buffers. The µP can then access the conversion result with a read instruction. For 16-bit bus operation, HBEN = 0, and the 12-bit result is read directly. For 8-bit bus operation, HBEN = 0 during the conversion, and the read instruction returns the 8 LSBs. A second read with HBEN = 1 returns the 4 MSBs in the low nibble. Note: In any mode, HBEN = 1 disables conversion start.

The DAS internal register is 5 bits wide: 3 bits for the analog-channel address, 1 bit for single-ended/differential mux operation, and 1 bit for unipolar/bipolar A/D operation.

Slow Memory Mode (MODE = 0)

The DAS appears to the µP as memory or as a slow peripheral in memory mode. The 5 configuration bits can be preset by an external data latch, a decoded device address, or any external selection logic. A read instruction initiates a conversion as shown in Figure 8. In this mode, the WR input functions as the RDY output and goes low when CS goes low. BUSY goes low after RD goes low, indicating the beginning of a signal acquisition cycle, and can be used to place the µP into a wait state. When the conversion is complete, BUSY releases the µP from its wait state. The µP can then access the conversion result with a read instruction. For 16-bit bus operation, HBEN = 0, and the 12-bit result is read directly. For 8-bit bus operation, HBEN = 0 during the conversion, and the read instruction returns the 8 LSBs. A second read with HBEN = 1 returns the 4 MSBs in the low nibble. Note: In any mode, HBEN = 1 disables conversion start.

ROM Mode, Parallel Read (MODE = 0)

ROM mode avoids using µP wait states. A conversion starts with a read instruction, and the 12 data bits from the previous conversion appear at D11-D0. The data from the first read in a sequence is often disregarded when ROM mode is used. A second read accesses the results of the first conversion and starts a new conversion. The time between successive reads must be longer than the conversion time of the MAX180/MAX181 (Figure 9a, 16-bit bus).

ROM Mode, 2-Byte Read (MODE = 0)

As in memory mode, only D7-D0 are used for a 2-byte read. A conversion starts with a read instruction when HBEN is low. At this point, the data outputs contain the 8 LSBs from the previous conversion. Two more read operations are needed to access the conversion result. The first, with HBEN high, accesses the 4 MSBs with 4 leading zeros. The second read, with HBEN low, outputs the 8 LSBs and starts a new conversion. Figure 9b (8-bit bus) details this mode.

Asynchronous Hold Mode (MODE = Open)

Asynchronous hold mode is helpful when a precise or repeatable sample timing is required. Asynchronous hold is very similar to the I/O port mode, except two write instructions are required. The first write, with HBEN = 1, configures the MAX180/MAX181 and connects the selected channel to the T/H input; the second write, with HBEN = 0, places the T/H into hold and starts the conversion. In other words, the three-clock cycle delay for T/H acquisition can be changed by controlling when the second write instruction occurs. The falling edge of the second WR pulse places the T/H into hold (Figure 10).

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External Clock

The range for the external clock duty cycle is between 20% and 80%. A precise square wave is not required.

Clock and Control Synchronization

For best analog performance, the MAX180/MAX181 clock should be synchronized to the $\overline{RD}$, $\overline{WR}$, and $\overline{CS}$ inputs (Figure 11) with at least 100ns separating convert start from the nearest clock edge. This synchronization ensures that transitions at CLKIN are not coupled to the analog input and sampled by the T/H. The magnitude of this feedthrough is only a few millivolts. If CLKIN and convert start ($\overline{CS}$, $\overline{WR}$ and $\overline{RD}$) are asynchronous, frequency components caused by mixing of the clock and convert signals can increase the apparent input noise.

When the clock and convert signals are synchronized, small end-point errors (offset and full-scale) are the most that can be generated by clock feedthrough, but even these errors are eliminated by ensuring that the start of a conversion ($\overline{RD}$ or $\overline{WR}$ and $\overline{CS}$ falling edge) does not occur within 100ns of a clock transition (Figure 11).

Output Data Format

The 12 data bits can be output either in full parallel or as two 8-bit bytes. Table 2 shows the data-bus output format. To obtain parallel output for 16-bit µPs, HBEN is tied low. Note: The output data, D11-D0, is right-justified (i.e. D0, the LSB, is the right-most bit in the 16-bit word).

A two-byte read makes use of outputs D7-D0. Byte selection is controlled by HBEN, which multiplexes the data outputs. When HBEN is low, the lower 8 bits appear at the data outputs. When HBEN is high, the upper 4 bits appear at D0-D3 with the leading 4 bits low in locations D4-D7. Note: The 4 MSBs always appear at D11-D8 when the outputs are enabled, regardless of the state of HBEN.

Application Hints

Initialization After Power-Up

In some applications, power is removed from the ADC during periods of inactivity to conserve power. This is increasingly common in battery-powered systems. To initialize the MAX180/MAX181 at power-up, execute a read operation with HBEN low, ignoring the data outputs.

Minimizing System-Induced Noise

The MAX180/MAX181 are insensitive to most noise sources, especially when the layout, bypass, and grounding recommendations are followed . The following practices should also be considered:

1. Minimize digital activity during conversion, especially activity that is asynchronous with the MAX180/MAX181 clock.
2. Avoid data-bus activity within ±20ns of the CLKIN falling edge.

If the data bus connected to the ADC is active during a conversion, coupling from the data pins to the ADC comparator can cause errors. Using slow-memory mode avoids this problem by placing the µP in a wait state during the conversion. In ROM mode, the bus should be isolated from the ADC using three-state drivers if the data bus is active during the conversion.

In ROM mode, the ADC generates considerable digital noise when $\overline{RD}$ or $\overline{CS}$ go high and the output data drivers are disabled after conversion start. This noise can affect the ADC comparator and cause large errors if it coincides with the SAR latching a comparator decision. To prevent this, $\overline{RD}$ and $\overline{CS}$ should be active for less than one clock cycle. If this is not possible, $\overline{RD}$ or $\overline{CS}$ should go high on a rising edge of CLKIN because the comparator output is latched on the falling edge of CLKIN.

Table 2. Data-Bus Output, $\overline{CS}$ & $\overline{RD}$ = LOW

DIP Pin #	Pin 16	Pin 17	Pin 18	Pin 19	Pin 21	Pin 22	Pin 23	Pin 24	Pin 25	Pin 26	Pin 27	Pin 28
Pin Label*	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
HBEN = LOW**	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
HBEN = HIGH**	D11	D10	D9	D8	LOW	LOW	LOW	LOW	D11	D10	D9	D8

Note: * D11–D0 are the ADC data output pin names.
** D11–D0 are the 12-bit conversion results. D11 is the MSB.

Layout, Grounding, Bypassing

Use printed circuit boards for best system performance; wire-wrap boards are not recommended. The board layout should ensure that digital- and analog-signal lines are separated as much as possible. Do not run analog and digital (especially clock) lines parallel to one another or digital lines underneath the ADC package.

Figure 12a shows the recommended system-ground connections. A single-point analog STAR ground should be established at AGND, separate from the logic ground. All other analog grounds and DGND should be connected to this STAR ground, and no other digital system grounds should be connected here. For noise-free operation, the ground return to the power supply from this STAR ground should be low impedance and as short as possible.

The ADC's high-speed comparator is sensitive to high-frequency noise in the V_{DD} and V_{SS} power supplies. These supplies should be bypassed to the analog STAR ground with 0.1µF and 47µF bypass capacitors. Minimize capacitor lead length for best supply noise rejection. If the 5V power supply is very noisy, connect a small (10Ω) resistor to filter the noise (Figure 12b).

Gain and Offset Adjustment

Figure 13 plots the nominal unipolar I/O transfer function of the MAX180/MAX181. Code transitions occur halfway between successive integer LSB values. Output coding for unipolar operation is natural binary with 1LSB = 1.22mV (5V/4096). Figure 14 shows the bipolar-input transfer function, where output coding is twos-complement.

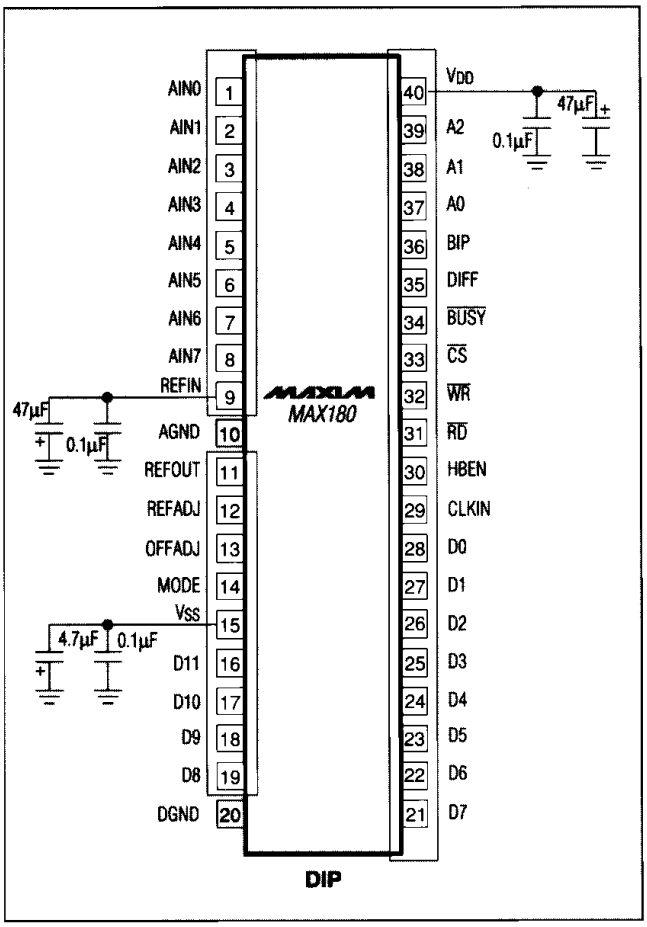

Figure 12a. Recommended Grounding and Ground Plane

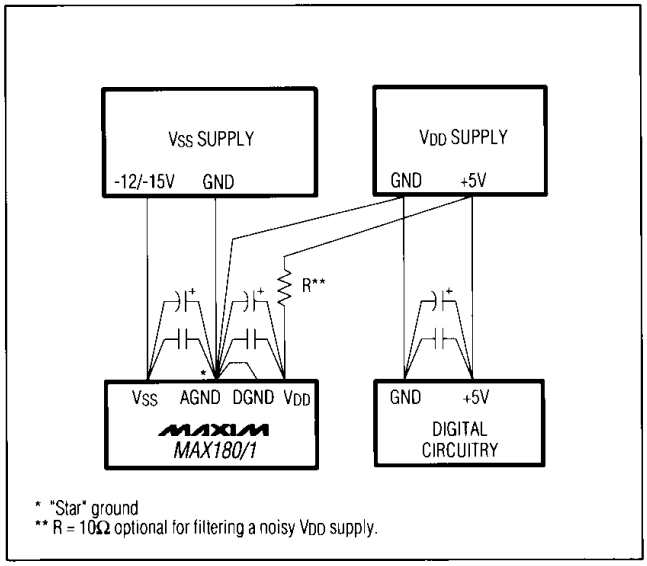

Figure 12b. Power-Supply Grounding

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If offset and gain adjustments are not desired, connect OFFADJ and REFADJ to V_{DD}. Figure 15's circuit provides ±1.2% (±50 LSBs) of adjustment range for gain and ±0.44% (±18LSBs) of adjustment range for offset. This is ideal for applications that require gain (full-scale range) or offset adjustment. If the adjustment inputs are used, bypass to AGND with a 0.1µF capacitor. Offset should be adjusted before gain. For the 0V to 5V input range, apply LSB (0.61mV) to the analog input, and adjust R1 so the digital output code changes between 0000 0000 0000 and 0000 0000 0001. To adjust full scale, apply FS - 1LSB (4.99817V), and adjust R2 until the output code changes between 1111 1111 1110 and 1111 1111 1111. There may be a slight interaction between the adjustments.

To adjust bipolar (±2.5V) offset, apply LSB (0.61mV) to the analog input, and adjust R1 until the output code switches between 0000 0000 0000 and 0000 0000 0001. For full scale, apply FS - 1LSB (2.49817V) to the input, and adjust R2 so the output code switches between 0111 1111 1110 and 0111 1111 1111 (Figure 15). There may be some interaction between these adjustments. If an external reference is used, adjust gain by varying the value of the reference instead of R2.

Dynamic Performance

Wide-bandwidth analog input and 100kHz throughput make the MAX180/MAX181 ideal for wideband-signal processing. To support these and other related applications, fast Fourier transform (FFT) test techniques guarantee the ADC's dynamic frequency response, distortion, and noise at the rated throughput. Specifically, this involves applying a low-distortion sine wave to the ADC input and recording the digital conversion results for a specified time. The data is then analyzed using an FFT algorithm that determines its spectral content. Conversion errors are seen as spectral elements outside of the fundamental input frequency.

ADCs have traditionally been evaluated by specifications such as zero and full-scale error and integral (INL) and differential (DNL) nonlinearity. Such parameters are widely accepted for specifying performance with DC and slowly varying signals, but less useful in signal-processing applications where the ADC's impact on the system transfer function is the main concern. The significance of the various DC parameters does not translate well to the dynamic case, so different tests are required.

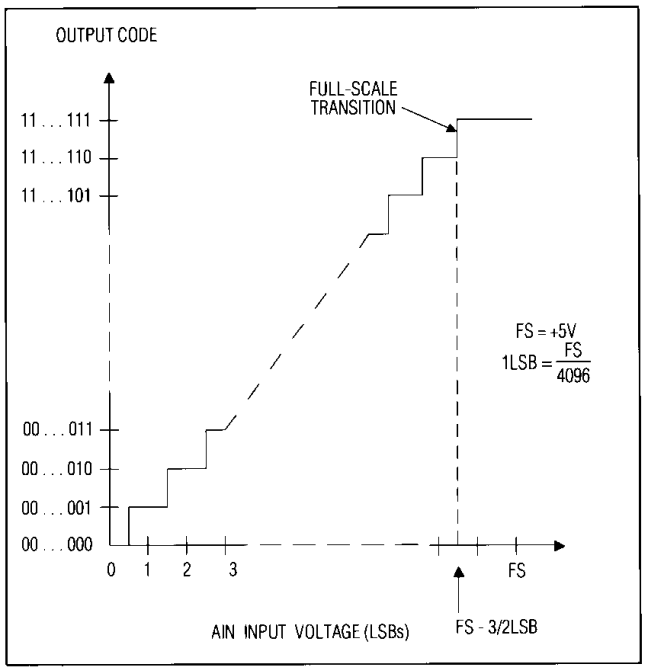

Figure 13. MAX180/MAX181 Unipolar Transfer Function

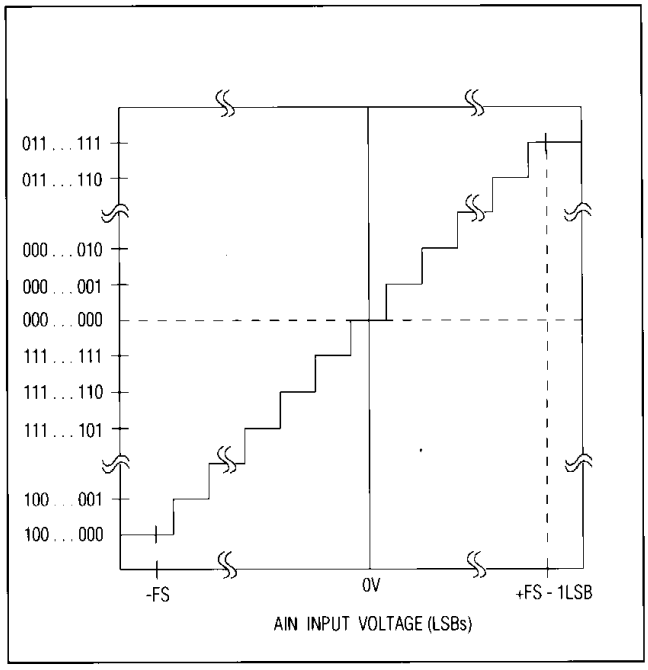

Figure 14. MAX180/MAX181 Bipolar Transfer Function

Signal-to-Noise Ratio and Effective Number of Bits

Signal-to-noise ratio (SNR) is the ratio between the RMS amplitude of the fundamental frequency to the RMS amplitude of all other ADC spectral components, excluding harmonics. The output band is limited to frequencies above DC and below one-half the ADC sample (conversion) rate. This band includes both distortion and noise components. For this reason, the signal-to-noise and distortion ratio (SINAD) is a better measure of the ADC's performance.

The theoretical minimum ADC noise is caused by quantization error and is a direct result of the ADC's resolution:

SNR = (6.02N + 1.76)dB

where N is the number of bits of resolution. A perfect 12-bit ADC can therefore do no better than 74dB. Figure 16 shows the result of sampling a pure 10kHz sinusoid at a 100kHz rate with the MAX180/MAX181. An output FFT plot shows the relative output amplitude at discrete spectral frequencies (Figure 16).

By transposing the equation that converts resolution to SNR, we can determine the effective resolution (effective number of bits) the ADC provides from the measured SNR: N = (SNR - 1.76)/6.02. Figure 17 shows the effective number of bits as a function of the input frequency for the MAX180/MAX181.

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of all the harmonics (in the frequency band above DC and below one-half the sample rate) to the RMS amplitude of the fundamental frequency. This is expressed as:

$$THD = 20Log\left[\frac{\sqrt{(V_2^2 + V_3^2 + \ldots + V_N^2)}}{V_1}\right]$$

where V_1 is the fundamental RMS amplitude, and V_2 to V_N are the amplitudes of the 2nd through Nth harmonics.

Spurious-Free Dynamic Range

Spurious-free dynamic range is the ratio of the fundamental RMS amplitude to the amplitude of the next largest spectral component (in the frequency band above DC and below one-half the sample rate). Usually this peak occurs at some harmonic of the input frequency. But if

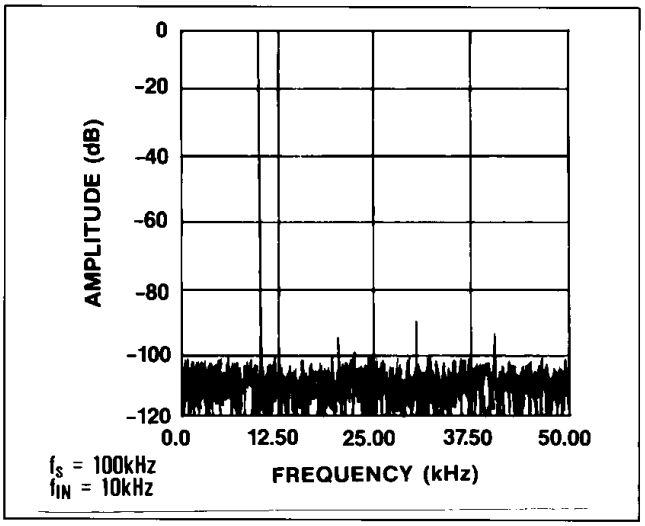

Figure 16. FFT Plot for the MAX180/MAX181

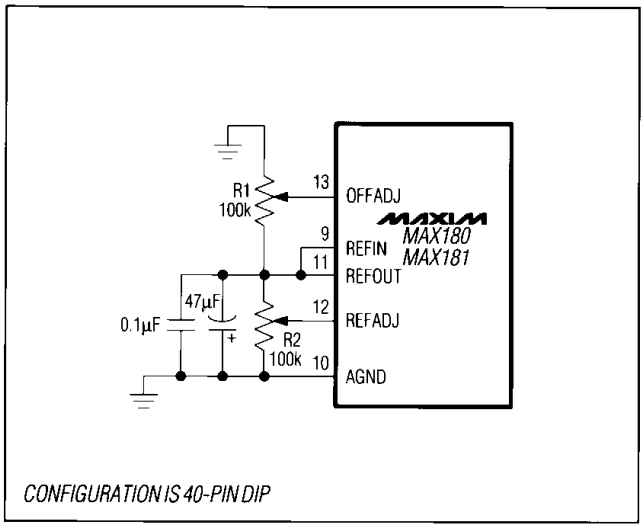

Figure 15. Offset and Gain Adjustment

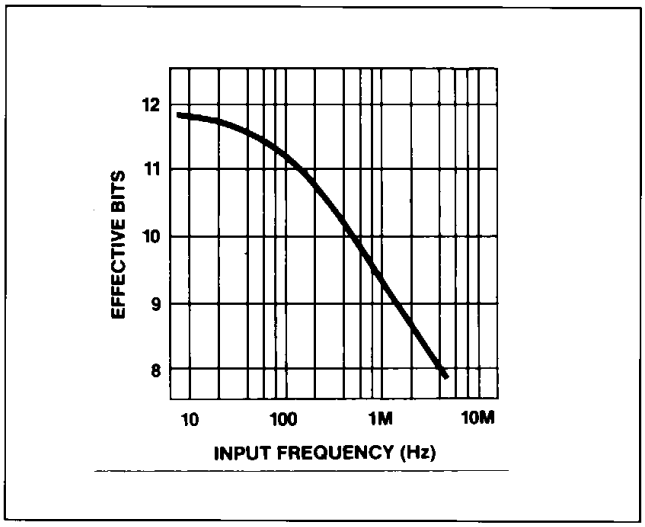

Figure 17. MAX180/MAX181 Effective Bits vs. Input Frequency

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Typical Applications

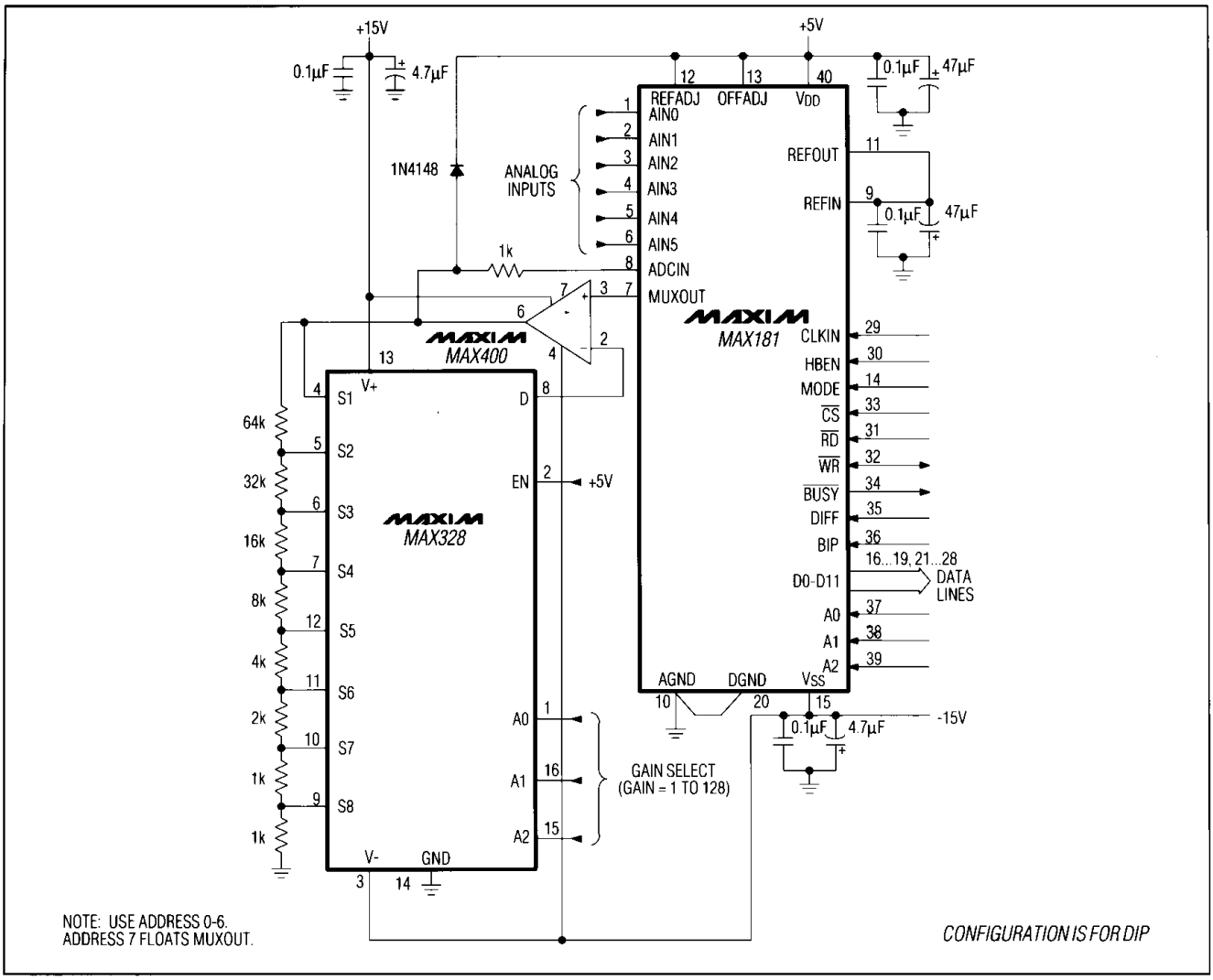


Figure 18a. MAX181 operating as a 6-channel programmable gain ADC. Gains are 1, 2, 4, 8, 16, 32, 64, and 128.

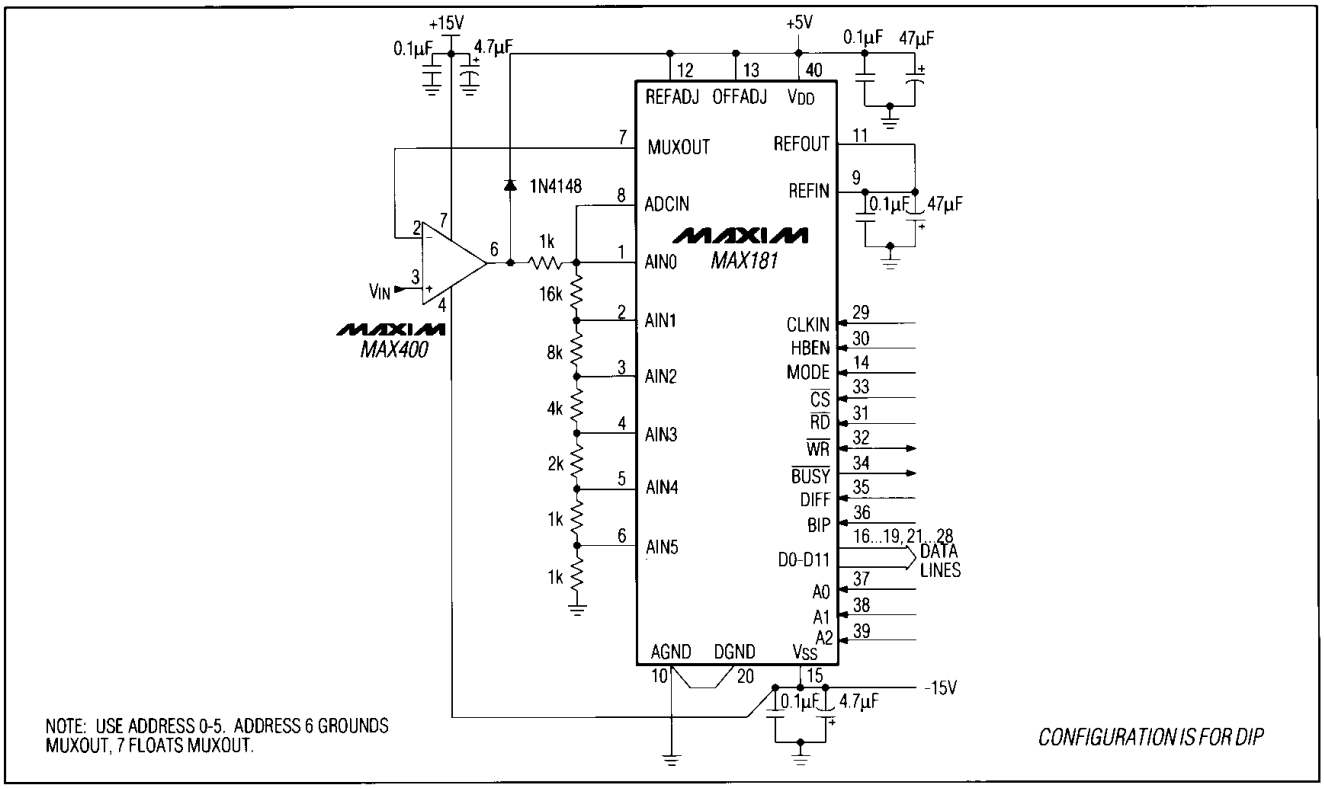
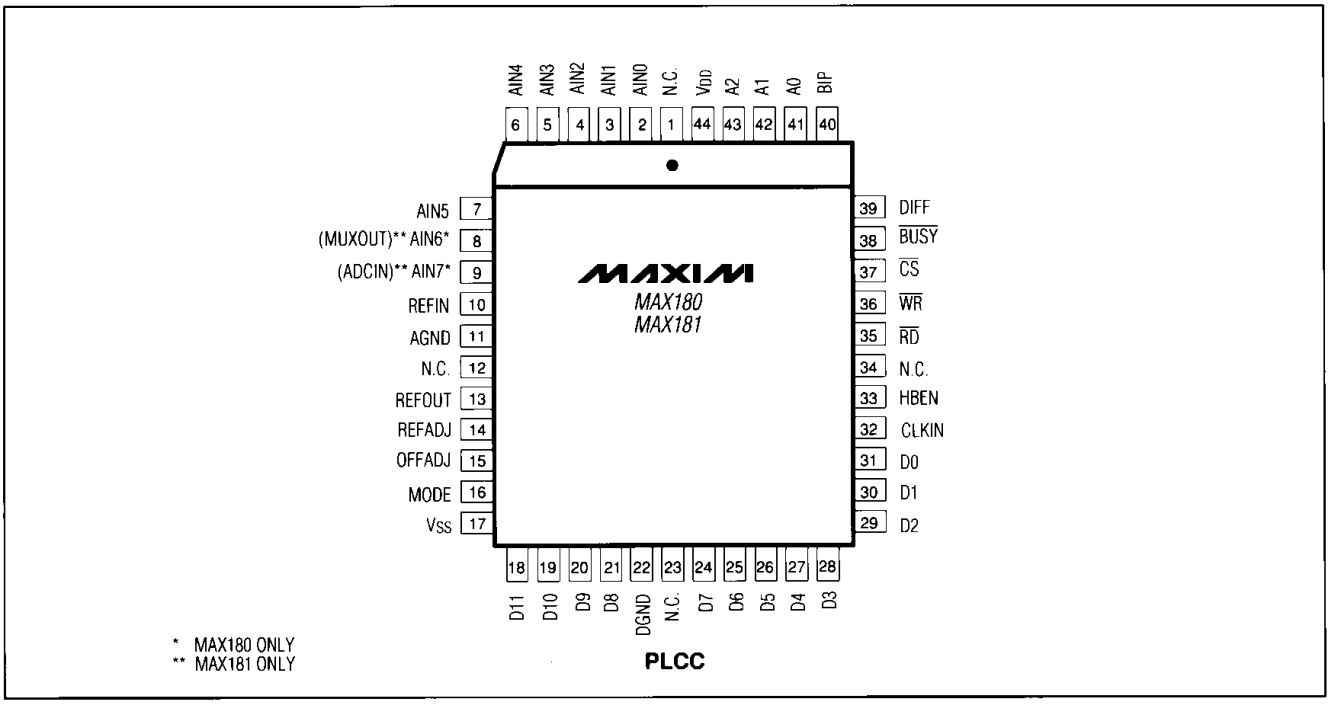


Figure 18b. MAX181 operating as a single-channel programmable gain ADC. Gains are 1, 2, 4, 16, and 32.

Pin Configurations (continued)



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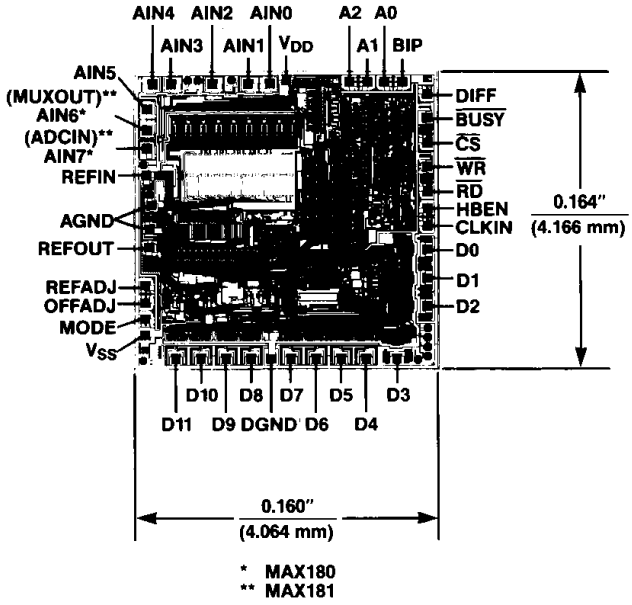
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSBs)
MAX180CCQH	0°C to +70°C	44 PLCC	±1
MAX180CC/D	0°C to +70°C	Dice*	±1
MAX180AEPL	-40°C to +85°C	40 Plastic DIP	±1/2
MAX180BEPL	-40°C to +85°C	40 Plastic DIP	±1
MAX180CEPL	-40°C to +85°C	40 Plastic DIP	±1
MAX180AEQH	-40°C to +85°C	44 PLCC	±1/2
MAX180BEQH	-40°C to +85°C	44 PLCC	±1
MAX180CEQH	-40°C to +85°C	44 PLCC	±1
MAX180AMJL	-55°C to +125°C	40 CERDIP**	±1/2
MAX180BMJL	-55°C to +125°C	40 CERDIP**	±1
MAX180CMJL	-55°C to +125°C	40 CERDIP**	±1
MAX181ACPL	0°C to +70°C	40 Plastic DIP	±1/2
MAX181BCPL	0°C to +70°C	40 Plastic DIP	±1
MAX181CCPL	0°C to +70°C	40 Plastic DIP	±1
MAX181ACQH	0°C to +70°C	44 PLCC	±1/2
MAX181BCQH	0°C to +70°C	44 PLCC	±1
MAX181CCQH	0°C to +70°C	44 PLCC	±1
MAX181CC/D	0°C to +70°C	Dice*	±1
MAX181AEPL	-40°C to +85°C	40 Plastic DIP	±1/2
MAX181BEPL	-40°C to +85°C	40 Plastic DIP	±1
MAX181CEPL	-40°C to +85°C	40 Plastic DIP	±1
MAX181AEQH	-40°C to +85°C	44 PLCC	±1/2
MAX181BEQH	-40°C to +85°C	44 PLCC	±1
MAX181CEQH	-40°C to +85°C	44 PLCC	±1
MAX181AMJL	-55°C to +125°C	40 CERDIP**	±1/2
MAX181BMJL	-55°C to +125°C	40 CERDIP**	±1
MAX181CMJL	-55°C to +125°C	40 CERDIP**	±1

* *Contact factory for dice specifications.*
** *Contact factory for availability and processing to MIL-STD-883.*

Chip Topography



* MAX180
** MAX181

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