Full-Featured µP Supervisory Circuit with ±1.5% Reset Accuracy

ABSOLUTE MAXIMUM RATINGS

Input Voltages (with respect to GND)
- V_{CC} .....-0.3V to 6V
- V_{BATT} .....-0.3V to 6V
- All Other Inputs.....-0.3V to (V_{OUT} + 0.3V)

Input Current
- V_{CC} Peak 1.0A
- V_{CC} Continuous 500mA
- I_{BATT} Peak.....250mA
- I_{BATT} Continuous 50mA
- GND 50mA
- All Other Inputs 50mA

Continuous Power Dissipation (T_A = +70°C)
- Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
- Wide SO (derate 9.52mW/°C above +70°C).....762mW
- CERDIP (derate 10.00mW/°C above +70°C).....800mW
- TSSOP (derate 6.70 mW/°C above +70°C) 533mW

Operating Temperature Ranges
- MAX807_C_E .....0°C to +70°C
- MAX807_E_E .....-40°C to +85°C
- MAX807_MJE .....-55°C to +125°C

Storage Temperature Range .....-65°C to +160°C

Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.60V to 5.5V for the MAX807L, V_{CC} = 4.50V to 5.5V for the MAX807N, V_{CC} = 4.35V to 5.5V for the MAX807M, V_{BATT} = 2.8V, V_{PFI} = 0V, T_A = T_{MIN} to T_{MAX}. Typical values are tested with V_{CC} = 5V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range V_{BATT}, V_{CC} (Note 1)				0		5.5	V
V_{OUT} in Normal Operating Mode		V_{CC} = 4.5V	I_{OUT} = 25mA		V_{CC} - 0.02		V
			I_{OUT} = 250mA, MAX807C/E	V_{CC} - 0.35	V_{CC} - 0.22		
			I_{OUT} = 250mA, MAX807M	V_{CC} - 0.45			
		V_{CC} = 3V, V_{BATT} = 2.8V, I_{OUT} = 100mA		V_{CC} - 0.25	V_{CC} - 0.12		
V_{CC} to OUT On-Resistance		V_{CC} = 4.5V, I_{OUT} = 250mA	MAX807C/E		1.0	1.4	Ω
			MAX807M			1.8	
		V_{CC} = 3V, I_{OUT} = 100mA			1.2	2.5	
V_{OUT} in Battery-Backup Mode		V_{BATT} = 4.5V, I_{OUT} = 20mA, V_{CC} = 0V			V_{BATT} - 0.17		V
		V_{BATT} = 2.8V, I_{OUT} = 10mA, V_{CC} = 0V		V_{BATT} - 0.25	V_{BATT} - 0.12		
		V_{BATT} = 2.0V, I_{OUT} = 5mA, V_{CC} = 0V		V_{BATT} - 0.20	V_{BATT} - 0.08		
BATT to OUT On-Resistance		V_{BATT} = 4.5V, I_{OUT} = 20mA			8.5		Ω
		V_{BATT} = 2.8V, I_{OUT} = 10mA			12	25	
		V_{BATT} = 2.0V, I_{OUT} = 5mA			16	40	
Supply Current in Normal Operating Mode (excludes I_{OUT})					70	110	µA
Supply Current in Battery-Backup Mode (excludes I_{OUT}) (Note 2)		V_{CC} = 0V, V_{BATT} = 2.8V	T_A = +25°C		0.4	1	µA
			MAX807C/E			5	
			MAX807M			50	
BATT Standby Current (Note 3)		V_{BATT} = 2.8V, V_{CC} = 3.0V	T_A = +25°C	-0.1		0.1	µA
			T_A = T_{MIN} to T_{MAX}	-1.0		1.0	
Battery-Switchover Threshold		V_{BATT} = 2.8V	Power up		V_{BATT} + 0.05		V
			Power down		V_{BATT}		
Battery-Switchover Hysteresis					50		mV
BATT ON Output, Low Voltage		$V_{RST\ (max)}$, I_{SINK} = 3.2mA			0.1	0.4	V
BATT ON Output, High Voltage		V_{CC} = 0V, I_{SOURCE} = 0.1mA, V_{BATT} = 2.8V		2	2.7		V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 4.60V to 5.5V for the MAX807L, V_{CC} = 4.50V to 5.5V for the MAX807N, V_{CC} = 4.35V to 5.5V for the MAX807M, V_{BATT} = 2.8V, V_{PFI} = 0V, T_A = T_{MIN} to T_{MAX}. Typical values are tested with V_{CC} = 5V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
BATT ON Output Short-Circuit Current		Sink current			70		mA
		Source current, V_{CC} = 0V, V_{BATT} = 2.8V			5		
RESET, LOW LINE, AND WATCHDOG TIMER							
Reset Threshold	V_{RST}	V_{CC} rising and falling	MAX807L	4.600	4.675	4.750	V
			MAX807N	4.500	4.575	4.650	
			MAX807M	4.350	4.425	4.500	
Reset Threshold Hysteresis					13		mV
LOW LINE to RESET Threshold Voltage	V_{LR}	V_{CC} falling		30	52	70	mV
LOW LINE Threshold, V_{CC} Rising	V_{LL}	MAX807L			4.73	4.81	V
		MAX807N			4.63	4.71	
		MAX807M			4.48	4.56	
V_{CC} to RESET Delay		V_{CC} falling at 1mV/µs			26		µs
V_{CC} to LOW LINE Delay		V_{CC} falling at 1mV/µs			24		µs
RESET Active-Timeout Period	t_{RP}	V_{CC} rising		140	200	280	ms
Watchdog-Timeout Period	t_{WD}			1.12	1.6	2.24	s
Minimum Watchdog Input Pulse Width		V_{IL} = 0.8V, V_{IH} = 0.75 x V_{CC}		100			ns
RESET Output Voltage		I_{SINK} = 50µA, V_{BATT} = 0V, V_{CC} falling	V_{CC} = 1V, MAX807_C			0.3	V
			V_{CC} = 1.2V, MAX807_E/M			0.3	
		I_{SINK} = 3.2mA, V_{CC} = 4.25V			0.1	0.4	
		I_{SOURCE} = 0.1mA		V_{CC} - 1.5	V_{CC} - 0.1		
RESET Output Short-Circuit Current	I_{SC}	Output sink current, V_{CC} = 4.25V			60		mA
		Output source current			1.6		
RESET Output Voltage		I_{SINK} = 3.2mA				0.4	V
		I_{SOURCE} = 5mA		V_{CC} - 1.5			
RESET Output Short-Circuit Current	I_{SC}	Output sink current			60		mA
		Output source current, V_{CC} = 4.25V			15		
LOW LINE Output Voltage		I_{SINK} = 3.2mA, V_{CC} = 4.25V				0.4	V
		I_{SOURCE} = 5mA		V_{CC} - 1.5			
LOW LINE Output Short-Circuit Current	I_{SC}	Output sink current, V_{CC} = 4.25V			28		mA
		Output source current			20		
WDO Output Voltage		I_{SINK} = 3.2mA				0.4	V
		I_{SOURCE} = 5mA		V_{CC} - 1.5			
WDO Output Short-Circuit Current	I_{SC}	Output sink current			35		mA
		Output source current			20		
WDI Threshold Voltage (Note 4)	V_{IH}			0.75 x V_{CC}			V
	V_{IL}					0.8	
WDI Input Current		Reset deasserted, WDI = 0V		-50	-10		µA
		Reset deasserted, WDI = V_{CC}			16	50	

Full-Featured µP Supervisory Circuit with ±1.5% Reset Accuracy

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 4.60V to 5.5V for the MAX807L, V_{CC} = 4.50V to 5.5V for the MAX807N, V_{CC} = 4.35V to 5.5V for the MAX807M, V_{BATT} = 2.8V, V_{PFI} = 0V, T_A = T_{MIN} to T_{MAX}. Typical values are tested with V_{CC} = 5V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PFI Input Threshold	V_{PFT}	V_{PFI} falling		2.20	2.265	2.33	V
		V_{PFI} rising		2.22	2.285	2.35	
PFI Hysteresis					20		mV
PFI Leakage Current					±0.005	±40	nA
PFI to PFO Delay (Note 5)		V_{OD} = 30mV, V_{PFI} falling			14		µs
CHIP-ENABLE GATING							
CE IN Leakage Current		Disabled mode, MR = 0V			±0.00002	±1	µA
CE IN to CE OUT Resistance (Note 6)		Enabled mode, V_{CC} = V_{RST} (max)			75	150	Ω
CE OUT Short-Circuit Current (RESET Active)		V_{CC} = 5V, disabled mode, CE OUT = 0, MR = 0V			17		mA
CE IN to CE OUT Propagation Delay (Note 7)		V_{CC} = 5V, C_{LOAD} = 50pF, 50Ω source impedance driver			2	8	ns
CE OUT Output Voltage High (RESET Active)		Disabled mode, MR = 0V	V_{CC} = 5V, I_{OUT} = 2mA	3.5			V
			V_{CC} = 0V, I_{OUT} = 10µA	V_{BATT} - 0.1	V_{BATT}		
RESET to CE OUT Delay		V_{CC} falling			28		µs
MANUAL RESET INPUT							
MR Minimum Pulse Input				1			µs
MR-to-RESET Propagation Delay					170		ns
MR Threshold	V_{IH}			2.4			V
	V_{IL}					0.8	
MR Pullup Current		MR = 0V		50	100	200	µA
BATT OK COMPARATOR							
BATT OK Threshold	V_{BOK}			2.200	2.265	2.350	V
BATT OK Hysteresis					20		mV
LOGIC OUTPUTS							
Output Voltage (PFO, BATT OK)	V_{OL}	I_{SINK} = 3.2mA				0.4	V
	V_{OH}	I_{SOURCE} = 5mA		V_{CC} - 1.5			
Output Short-Circuit Current	I_{SC}	Output sink current			35		mA
		Output source current			20		

Note 1: Either V_{CC} or V_{BATT} can go to 0 if the other is greater than 2.0V.

Note 2: The supply current drawn by the MAX807 from the battery (excluding I_{OUT}) typically goes to 15µA when (V_{BATT} - 0.1V) < V_{CC} < V_{BATT}. In most applications, this is a brief period as V_{CC} falls through this region (see *Typical Operating Characteristics*).

Note 3: "+"= battery discharging current, "-"= battery charging current.

Note 4: WDI is internally connected to a voltage-divider between V_{CC} and GND. If unconnected, WDI is driven to 1.8V (typical), disabling the watchdog function.

Note 5: Overdrive (V_{OD}) is measured from center of hysteresis band.

Note 6: The chip-enable resistance is tested with $V_{CE\ IN}$ = V_{CC}/2, and $I_{CE\ IN}$ = 1mA.

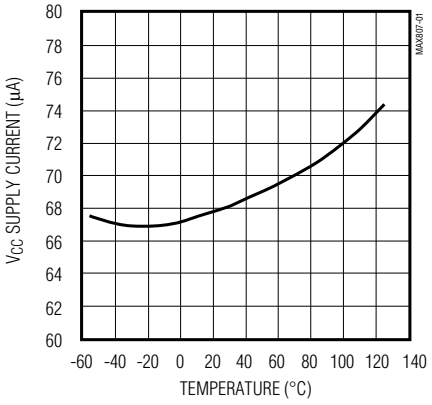
Note 7: The chip-enable propagation delay is measured from the 50% point at CE IN to the 50% point at CE OUT.

Full-Featured µP Supervisory Circuit with ±1.5% Reset Accuracy

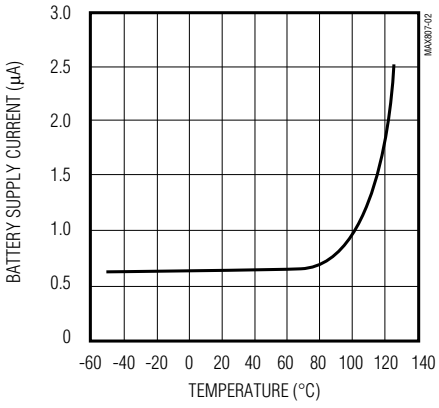
Typical Operating Characteristics

(V_{CC} = 5V, V_{BATT} = 2.8V, PFI = 0, no load, T_A = +25°C, unless otherwise noted.)

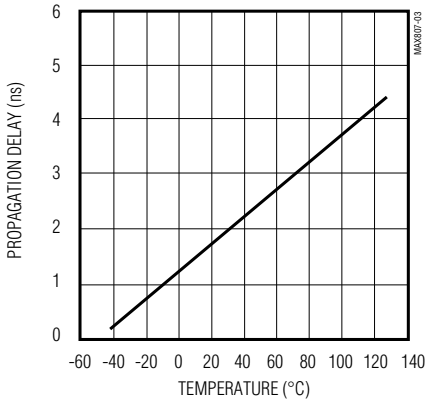
V_{CC} SUPPLY CURRENT vs. TEMPERATURE (NORMAL OPERATING MODE)



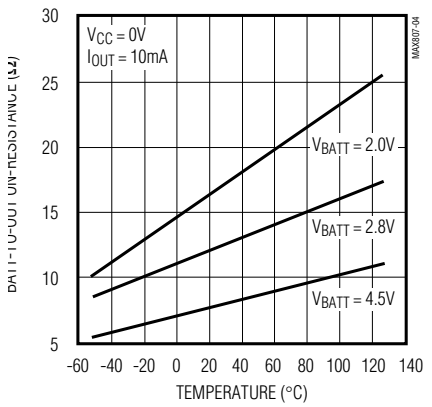
BATTERY SUPPLY CURRENT vs. TEMPERATURE (BATTERY-BACKUP MODE)



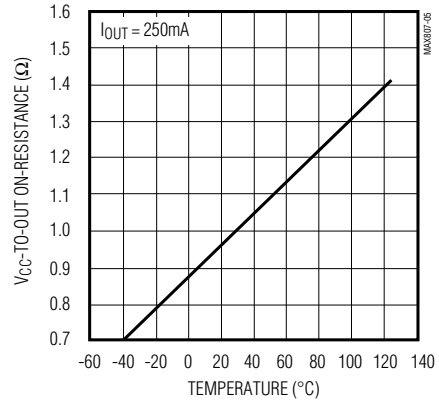
CHIP-ENABLE PROPAGATION DELAY vs. TEMPERATURE



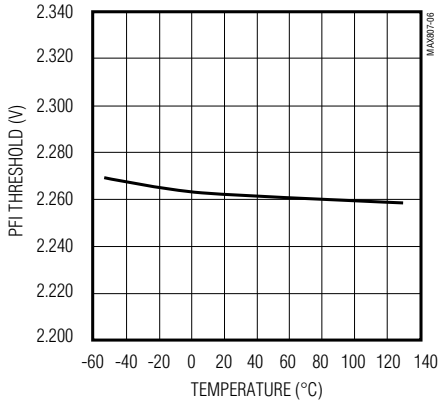
BATT-TO-OUT ON-RESISTANCE vs. TEMPERATURE



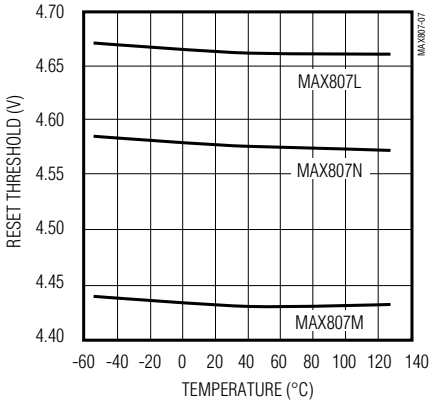
V_{CC}-TO-OUT ON-RESISTANCE vs. TEMPERATURE



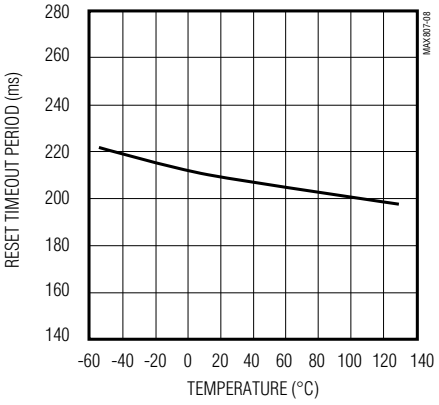
PFI THRESHOLD vs. TEMPERATURE (V_{PFI} FALLING)



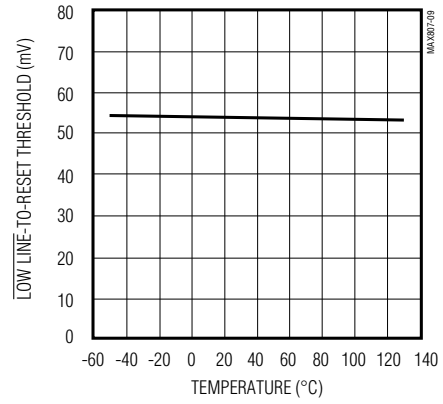
RESET THRESHOLD vs. TEMPERATURE



RESET TIMEOUT PERIOD vs. TEMPERATURE (V_{CC} RISING)



$\overline{\text{LOW LINE}}$ -TO-RESET THRESHOLD vs. TEMPERATURE (V_{CC} FALLING)

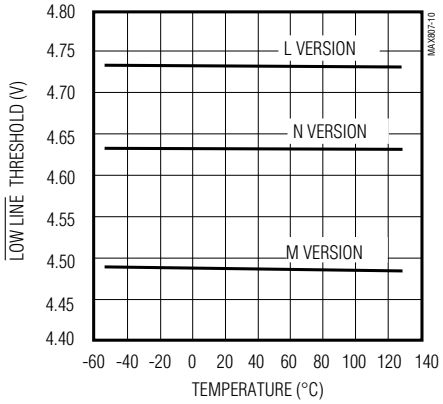


Full-Featured µP Supervisory Circuit with ±1.5% Reset Accuracy

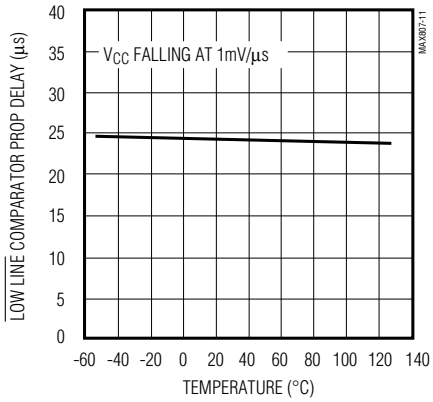
Typical Operating Characteristics (contiued)

(V_{CC} = 5V, V_{BATT} = 2.8V, PFI = 0, no load, T_A = +25°C, unless otherwise noted.)

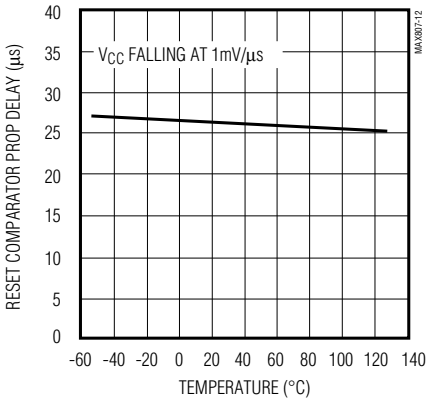
$\overline{\text{LOW LINE}}$ THRESHOLD vs. TEMPERATURE (V_{CC} RISING)



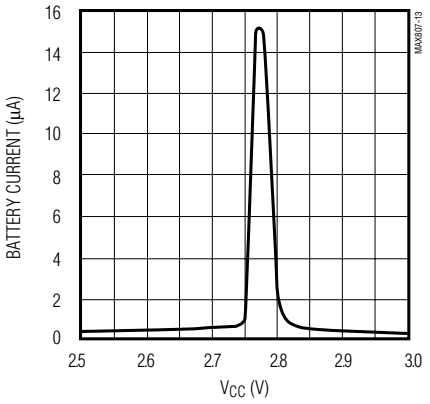
$\overline{\text{LOW LINE}}$ COMPARATOR PROPAGATION DELAY vs. TEMPERATURE (V_{CC} FALLING)



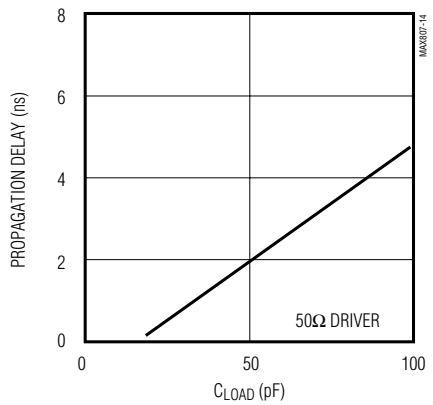
RESET COMPARATOR PROPAGATION DELAY vs. TEMPERATURE (V_{CC} FALLING)



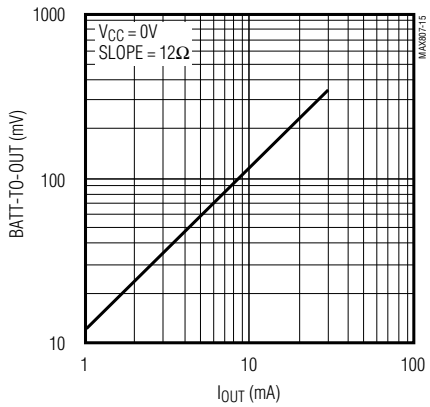
BATTERY CURRENT vs. INPUT SUPPLY VOLTAGE



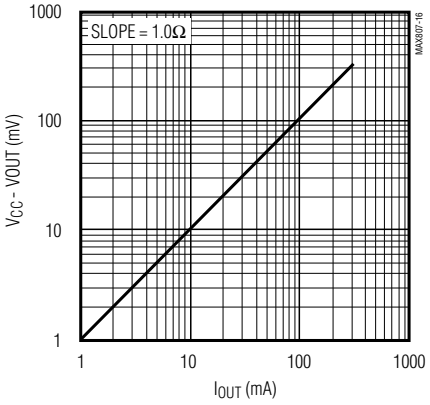
CHIP-ENABLE PROPAGATION DELAY vs. $\overline{\text{CE}}$ OUT LOAD CAPACITANCE



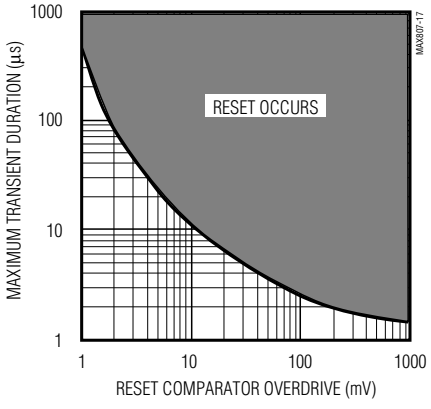
BATT-TO-OUT vs. OUTPUT CURRENT



V_{CC}-TO-OUT vs. OUTPUT CURRENT



MAXIMUM TRANSIENT DURATION vs. RESET COMPARATOR OVERDRIVE



Pin Description

PIN	NAME	FUNCTION
1	PFI	Power-Fail Input. When PFI is less than V_{PFT} (2.265V), PFO goes low. Connect to ground when unused.
2	PFO	Power-Fail Output. This CMOS-logic output goes low when PFI is less than V_{PFT} (2.265V). Valid for $V_{CC} \geq 4V$. PFO swings between V_{CC} and GND.
3	V_{CC}	Input Supply Voltage, nominally +5V. Bypass with a 0.1µF capacitor to GND.
4	WDI	Watchdog Input. If WDI remains high or low longer than the watchdog-timeout period (1.6s, typ), WDO goes low. Leave unconnected to disable the watchdog function.
5	GND	Ground
6	MR	Manual-Reset Input. A logic low on MR asserts reset. Reset remains asserted as long as MR remains low and for 200ms after MR returns high. MR is an active-low input with an internal pullup to V_{CC}. It can be driven using TTL or CMOS logic, or shorted to ground with a switch. Connect to V_{CC}, or leave unconnected if not used.
7	LOW LINE	Low-Line Comparator Output. This CMOS-logic output goes low when V_{CC} falls to 52mV above the reset threshold. Use this output to generate an NMI to initiate an orderly shutdown routine when V_{CC} is falling. LOW LINE swings between V_{CC} and GND.
8	RESET	Active-High Reset Output. RESET is the inverse of RESET. It is a CMOS output that sources and sinks current. RESET swings between V_{CC} and GND.
9	RESET	Active-Low Reset Output. RESET is triggered and stays low when V_{CC} is below the reset threshold or when MR is low. It remains low 200ms after V_{CC} rises above the reset threshold or MR returns high. RESET has a strong pulldown but a relatively weak pullup, and can be wire-OR connected to logic gates. Valid for $V_{CC} \geq 1V$. RESET swings between V_{CC} and GND.
10	WDO	Watchdog Output. This CMOS-logic output goes low if WDI remains high or low longer than the watchdog-timeout period (t_{WD}), and remains low until the next transition of WDI. WDO remains high if WDI is unconnected. WDO is high during reset. WDO swings between V_{CC} and GND. Connect WDO to MR to generate resets during watchdog faults.
11	CE OUT	Chip-Enable Output. Output to the chip-enable gating circuit. CE OUT is pulled up to the higher of V_{CC} or V_{BATT}, when the chip-enable gate is disabled.
12	CE IN	Chip-Enable Input
13	BATT ON	Battery-On Output. CMOS-logic output/external bypass switch driver. High when OUT is connected to BATT and low when OUT is connected to V_{CC}. Connect the base of a PNP transistor or gate of a PMOS transistor to BATT ON for I_{OUT} requirements exceeding 250mA. BATT ON swings between the higher of V_{CC} and V_{BATT} and GND.
14	BATT	Backup-Battery Input. When V_{CC} falls below the reset threshold and V_{BATT}, OUT switches from V_{CC} to BATT. V_{BATT} may exceed V_{CC}. The battery can be removed while the MAX807 is powered-up, provided BATT is bypassed with a 0.1µF capacitor to GND. If no battery is used, connect BATT to ground, and connect V_{CC} and OUT together.
15	BATT OK	Battery-OK Signal Output. High in normal operating mode when V_{BATT} exceeds V_{BOK} (2.265V). Valid for $V_{CC} \geq 4V$.
16	OUT	Output Supply Voltage to CMOS RAM. When V_{CC} exceeds the reset threshold or $V_{CC} > V_{BATT}$, OUT is connected to V_{CC}. When V_{CC} falls below the reset threshold and V_{BATT}, OUT connects to BATT. Bypass OUT with a 0.1µF capacitor to GND.

Full-Featured µP Supervisory Circuit with ±1.5% Reset Accuracy

Detailed Description

The MAX807 µP supervisory circuit provides power-supply monitoring, backup-battery switchover, and program execution watchdog functions in µP systems (Figure 1). Use of BiCMOS technology results in an improved 1.5% reset-threshold precision, while keeping supply currents typically below 70µA. The MAX807 is intended for battery-powered applications that require high reset-threshold precision, allowing a wide power-supply operating range while preventing the system from operating below its specified voltage range.

RESET and RESET Outputs

The MAX807's RESET output ensures that the µP powers up in a known state, and prevents code execution errors during power-down and brownout conditions. It accomplishes this by resetting the µP, terminating program execution when V_{CC} dips below the reset threshold or MR is pulled low. Each time RESET is asserted it stays low for the 200ms reset timeout period, which is set by an internal timer to ensure the µP has adequate time to return to an initial state. Any time V_{CC} goes below the reset threshold before the reset-timeout period is completed, the internal timer restarts. The watchdog timer can also initiate a reset if WDO is connected to MR (see the *Watchdog Input* section).

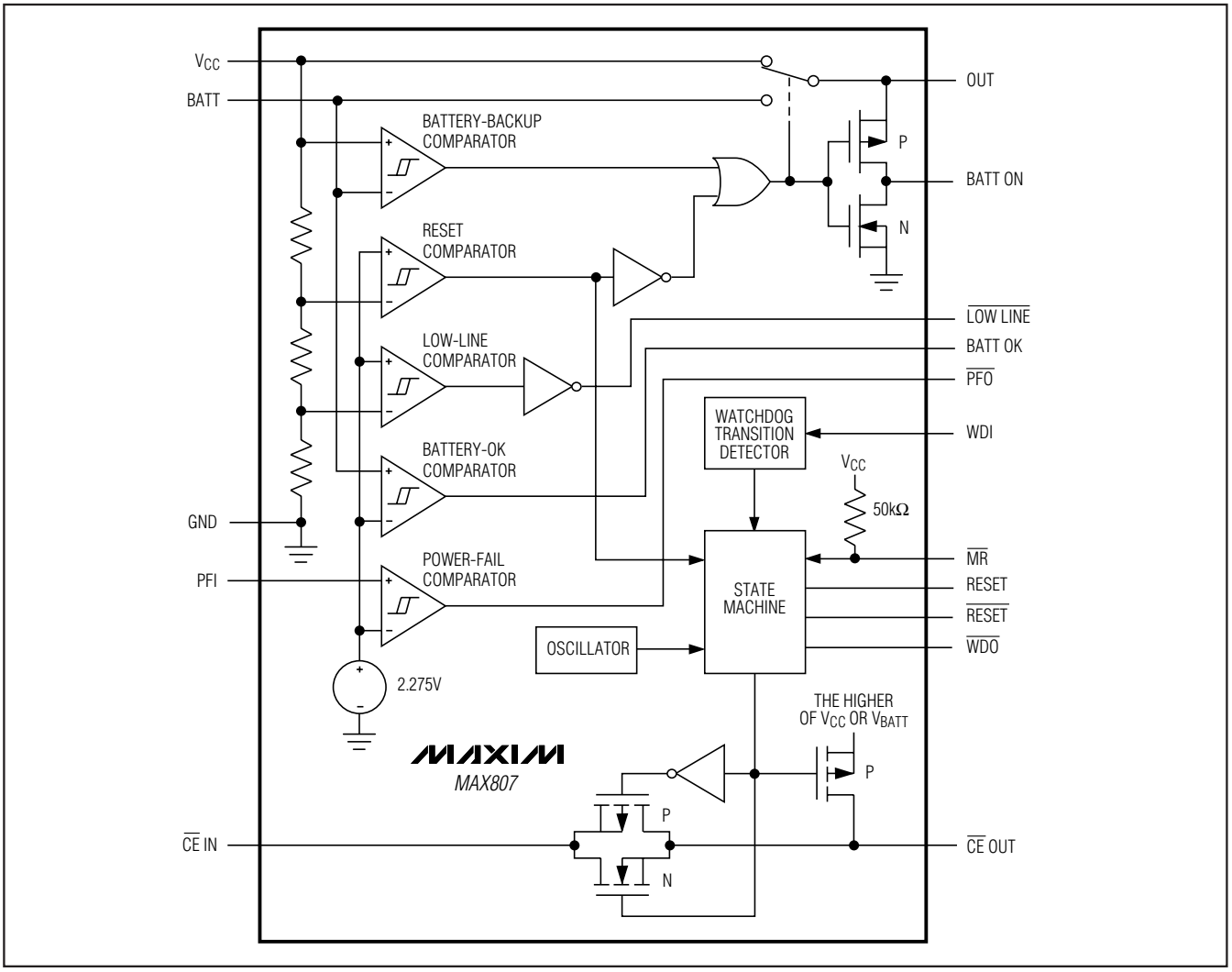


Figure 1. Block Diagram

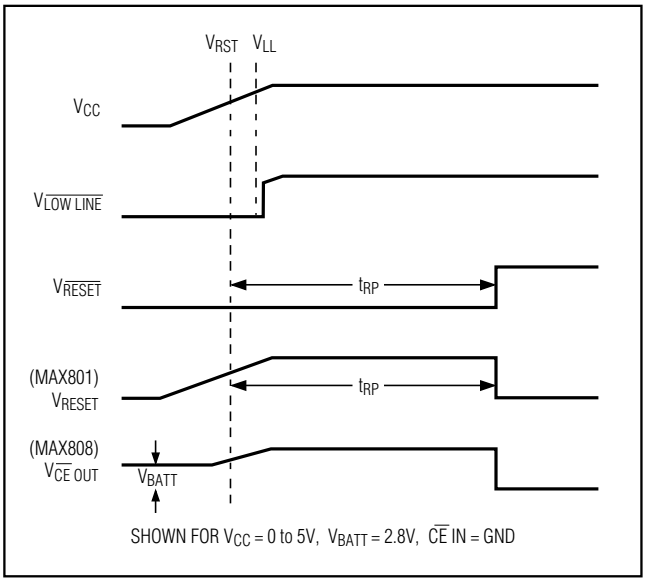


Figure 2a. Timing Diagram, V_{CC} Rising

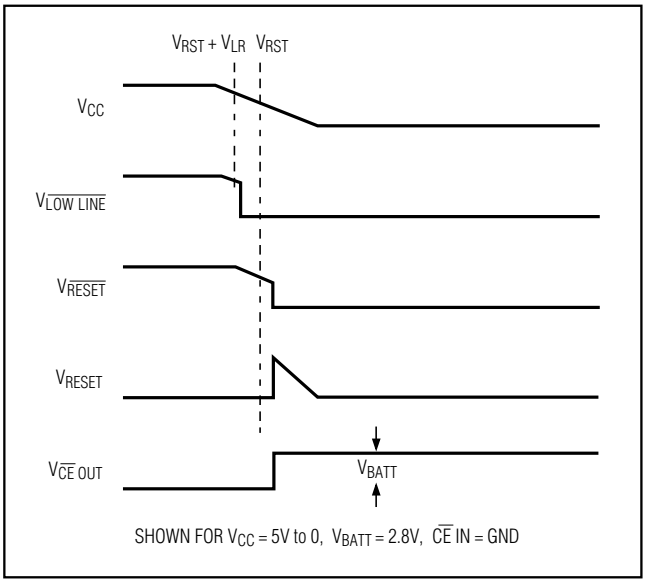


Figure 2b. Timing Diagram, V_{CC} Falling

The RESET output is active low and implemented with a strong pulldown/relatively weak pullup structure. It is guaranteed to be a logic low for $0 < V_{CC} < V_{RST}$, provided V_{BATT} is greater than 2V. Without a backup battery, RESET is guaranteed valid for $V_{CC} \geq 1$. It typically sinks 3.2mA at 0.1V saturation voltage in its active state.

The RESET output is the inverse of the RESET output; it both sources and sinks current and cannot be wire-OR connected. Figure 2a shows a timing diagram with V_{CC} rising and Figure 2b shows V_{CC} falling.

Manual Reset Input

Many µP-based products require manual-reset capability to allow an operator or test technician to initiate a reset. The Manual Reset (MR) input permits the generation of a reset in response to a logic low from a switch, WDO, or external circuitry. Reset remains asserted while MR is low, and for 200ms after MR returns high.

MR has an internal 50µA to 200µA pullup current, so it can be left open if it is not used. MR can be driven with TTL or CMOS-logic levels, or with open-drain/collector outputs. Connect a normally open momentary switch from MR to GND to create a manual-reset function; external debounce circuitry is not required. If MR is driven from long cables or if the device is used in a noisy environment, connect a 0.1µF capacitor from MR to ground to provide additional noise immunity. As shown in Figure 3, diode-ORed connections can be used to allow manual resets from multiple sources. Figure 4 shows the reset timing.

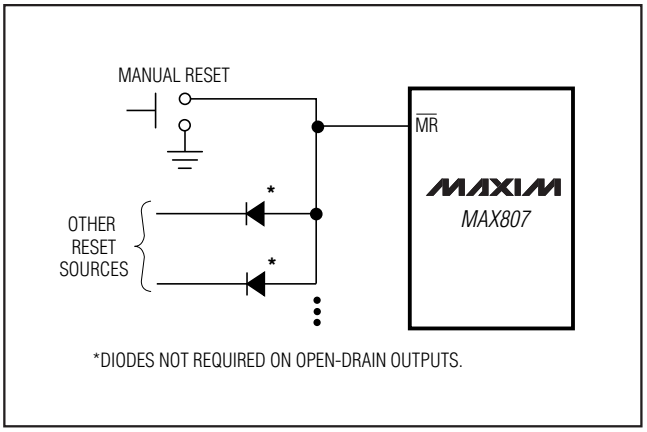


Figure 3. Diode "OR" Connections Allow Multiple Reset Sources to Connect to MR

Watchdog Timer

Watchdog Input

The watchdog circuit monitors the µP's activity. If the µP does not toggle the watchdog input (WDI) within 1.6s, WDO goes low. The internal 1.6s timer is cleared and WDO returns high when reset is asserted or when a transition (low-to-high or high-to-low) occurs at WDI while RESET is high. As long as reset is asserted, the timer remains cleared and does not count. As soon as reset is released, the timer starts counting (Figure 5). Supply current is typically reduced by 10µA when WDI is at a valid logic level.

Full-Featured µP Supervisory Circuit with ±1.5% Reset Accuracy

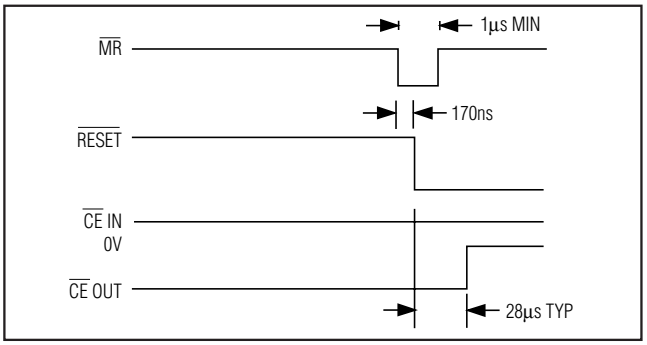


Figure 4. Manual-Reset Timing Diagram

Watchdog Output

WDO remains high if there is a transition or pulse at WDI during the watchdog-timeout period. WDO goes low if no transition occurs at WDI during the watchdog-timeout period. The watchdog function is disabled and WDO is a logic high when V_{CC} is below the reset threshold or WDI is an open circuit. To generate a system reset on every watchdog fault, diode-OR connect WDO to MR (Figure 6). When a watchdog fault occurs in this mode, WDO goes low, which pulls MR low, causing a reset pulse to be issued. As soon as reset is asserted, the watchdog timer clears and WDO returns high. With WDO connected to MR, a continuous high or low on WDI will cause 200ms reset pulses to be issued every 1.6s.

Chip-Enable Signal Gating

The MAX807 provides internal gating of chip-enable (CE) signals to prevent erroneous data from corrupting the CMOS RAM in the event of a power failure. During normal operation, the CE gate is enabled and passes all CE transitions. When reset is asserted, this path becomes disabled, preventing erroneous data from corrupting the CMOS RAM. The MAX807 uses a series transmission gate from the Chip-Enable Input (CE IN) to the Chip-Enable Output (CE OUT) (Figure 1).

The 8ns (max) chip-enable propagation from CE IN to CE OUT enables the MAX807 to be used with most µPs.

Chip-Enable Input

CE IN is high impedance (disabled mode) while RESET is asserted. During a power-down sequence when V_{CC} passes the reset threshold, the CE transmission gate disables and CE IN becomes high impedance 28µs after reset is asserted (Figure 7). During a power-up sequence, CE IN remains high impedance (regardless of $\overline{CE}$ IN activity) until reset is deasserted following the reset-timeout period.

In the high-impedance mode, the leakage currents into this input are ±1µA (max) over temperature. In the low-impedance mode, the impedance of CE IN appears as a 75Ω resistor in series with the load at CE OUT.

The propagation delay through the CE transmission gate depends on both the source impedance of the drive to CE IN and the capacitive loading on CE OUT

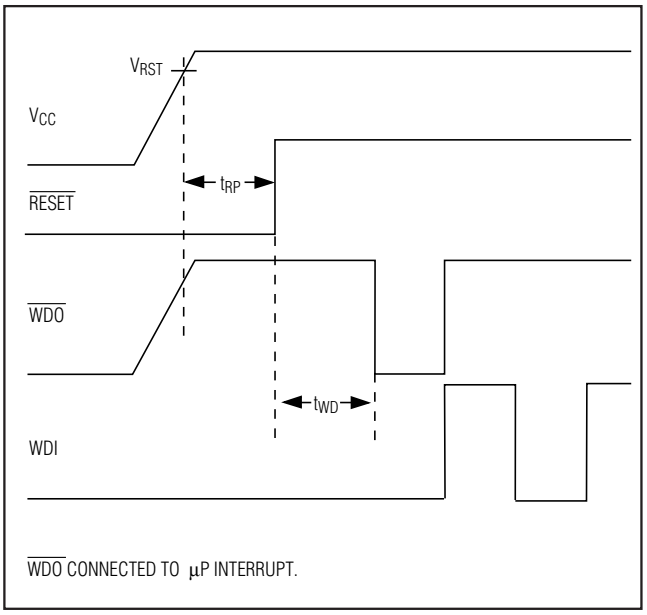


Figure 5. Watchdog Timing Relationship

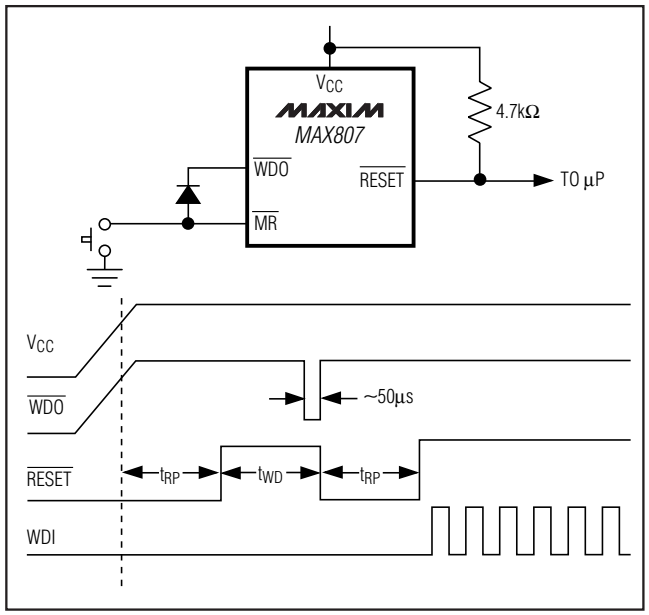


Figure 6. Generating a Reset on Each Watchdog Fault

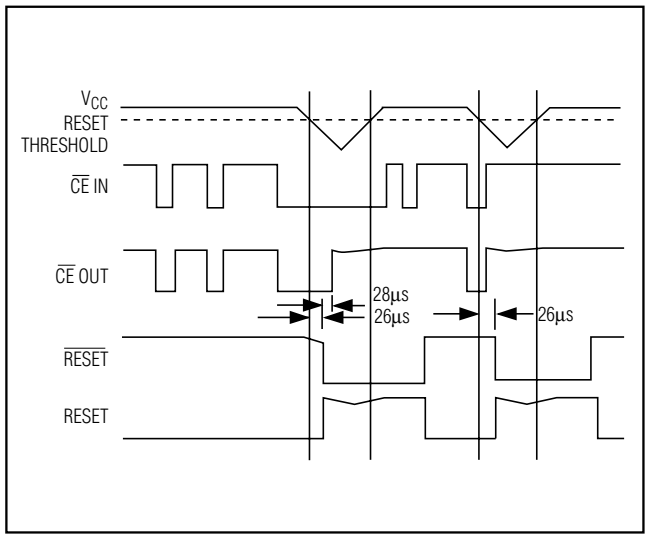


Figure 7. Reset and Chip-Enable Timing

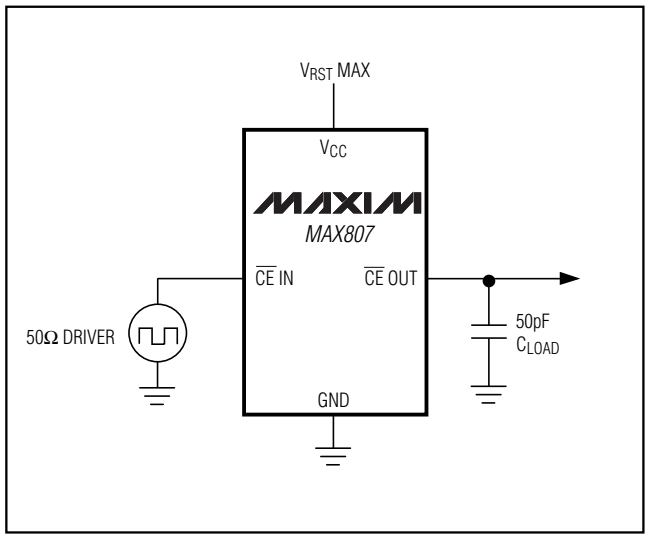


Figure 8. CE Propagation Delay Test Circuit

(see the Chip-Enable Propagation Delay vs. CE OUT Load Capacitance graph in the *Typical Operating Characteristics*). The CE propagation delay is production tested from the 50% point on CE IN to the 50% point on CE OUT using a 50Ω driver and 50pF of load capacitance (Figure 8). For minimum propagation delay, minimize the capacitive load at CE OUT and use a low output-impedance driver.

Chip-Enable Output

In the enabled mode, the impedance of CE OUT is equivalent to 75Ω in series with the source driving CE IN. In the disabled mode, the 75Ω transmission gate is off and CE OUT is actively pulled to the higher of V_{CC} or V_{BATT}. This source turns off when the transmission gate is enabled.

Low-Line Comparator

The low-line comparator monitors V_{CC} with a threshold voltage typically 52mV above the reset threshold, with 13mV of hysteresis. Use LOW LINE to provide a nonmaskable interrupt (NMI) to the µP when power begins to fall to initiate an orderly software shutdown routine.

In most battery-operated portable systems, reserve energy in the battery provides ample time to complete the shutdown routine once the low-line warning is encountered, and before reset asserts. If the system must contend with a more rapid V_{CC} fall time—such as when the main battery is disconnected, a DC-DC converter shuts down, or a high-side switch is opened during normal operation—use capacitance on the V_{CC} line to provide time to execute the shutdown routine (Figure 9). First calculate the worst-case time required for the system to perform its shutdown routine. Then, with the worst-case shutdown time, the worst-case load current, and the minimum low-line to reset threshold ($V_{LR(min)}$), calculate the amount of capacitance required to allow the shutdown routine to complete before reset is asserted:

$$C_{HOLD} = (I_{LOAD} \times t_{SHDN}) / V_{LR}\ (min)$$

where t_{SHDN} is the time required for the system to complete the shutdown routine, and includes the V_{CC} to low-line propagation delay; and where I_{LOAD} is the current being drained from the capacitor, V_{LR} is the low-line to reset threshold.

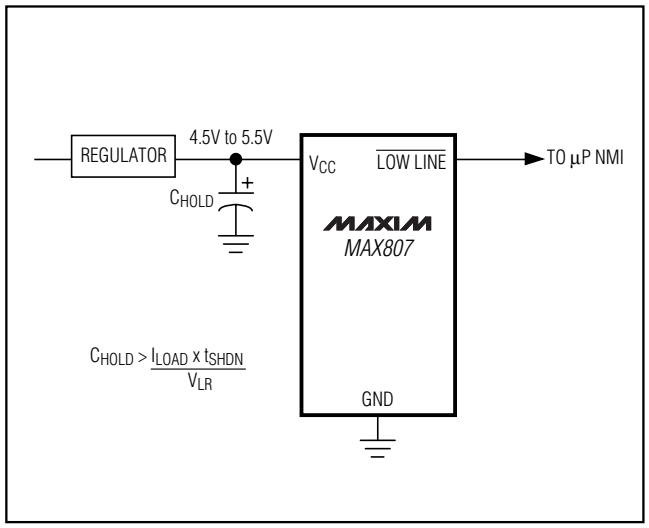


Figure 9. Using LOW LINE to Provide a Power-Fail Warning to the µP

Full-Featured µP Supervisory Circuit with ±1.5% Reset Accuracy

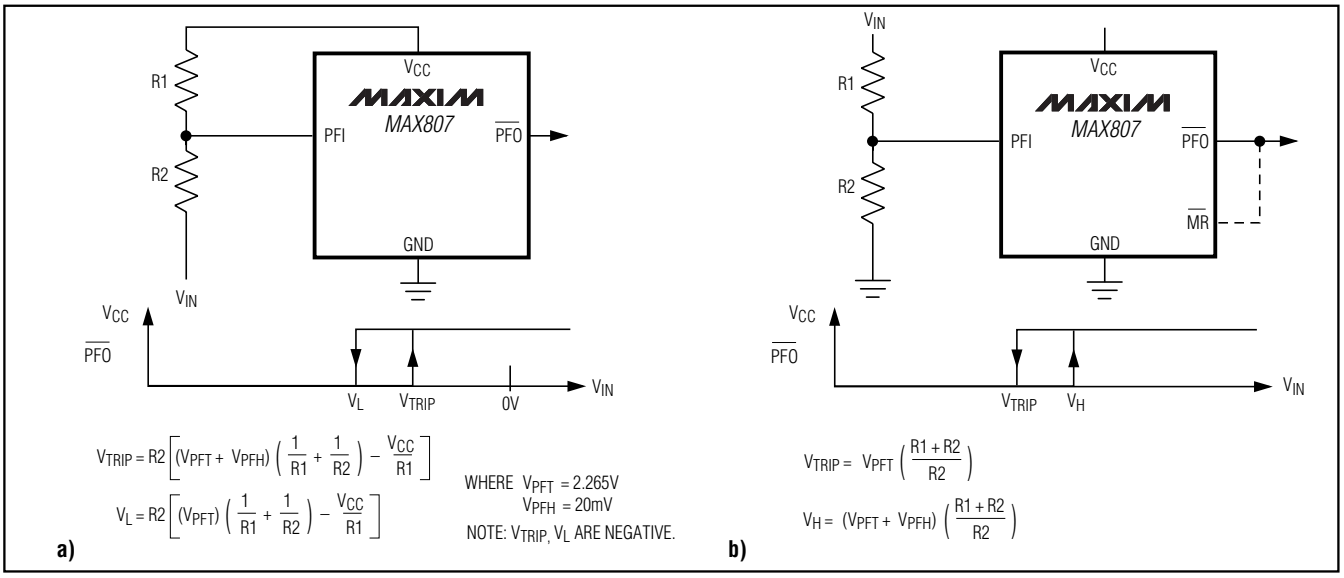


Figure 10. Using the Power-Fail Comparator to Monitor an Additional Power Supply: a) V_{IN} is Negative, b) V_{IN} is Positive

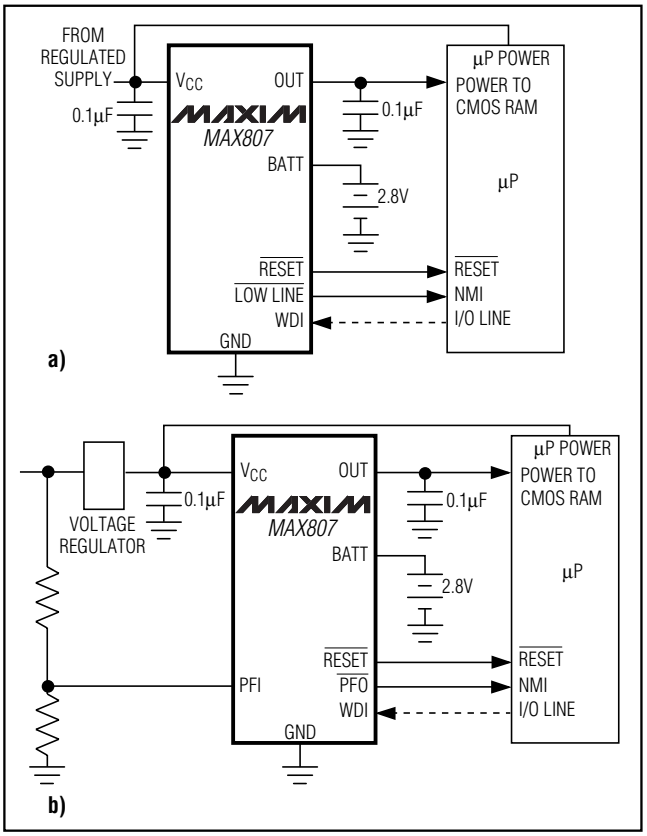


Figure 11. a) If the preregulated supply is inaccessible, LOW LINE generates the NMI for the µP. b) Use PFO to generate the µP NMI if the preregulated supply is accessible.

Power-Fail Comparator

PFI is the noninverting input to an uncommitted comparator. If PFI is less than V_{PFT} (2.265V), PFO goes low. The power-fail comparator is intended to monitor the preregulated input of the power supply, providing an early power-fail warning so software can conduct an orderly shutdown. It can also be used to monitor supplies other than 5V. Set the power-fail threshold with a resistor-divider, as shown in Figure 10.

Power-Fail Input

PFI is the input to the power-fail comparator. The typical comparator delay is 14µs from V_{IL} to V_{OL} (power failing), and 32µs from V_{IH} to V_{OH} (power being restored). If unused, connect this input to ground.

Power-Fail Output

The Power-Fail Output (PFO) goes low when PFI goes below V_{PFT}. It typically sinks 3.2mA with a saturation voltage of 0.1V. With PFI above V_{PFT}, PFO is actively pulled to V_{CC}. Connecting PFI through a voltage-divider to a preregulated supply allows PFO to generate an NMI as the preregulated power begins to fall (Figure 11b). If the preregulated supply is inaccessible, use LOW LINE to generate the NMI (Figure 11a). The LOW LINE threshold is typically 52mV above the reset threshold (see the *Low-Line Comparator* section).

Table 1. Input and Output Status in Battery-Backup Mode

PIN	NAME	FUNCTION
1	PFI	The power-fail comparator remains active in battery-backup mode for $V_{CC} \geq 4V$.
2	PFO	The power-fail comparator remains active in battery-backup mode for $V_{CC} \geq 4V$. Below 4V, PFO is forced low.
3	V_{CC}	Battery switchover comparator monitors V_{CC} for active switchover.
4	WDI	WDI is ignored and goes high impedance
5	GND	Ground—0V reference for all signals
6	MR	MR is ignored
7	LOW LINE	Logic low
8	RESET	Logic high; the open-circuit output voltage is equal to V_{CC}.
9	RESET	Logic low
10	WDO	Logic high. The open-circuit output voltage is equal to V_{CC}.
11	CE OUT	Logic high. The open-circuit output voltage is equal to V_{BATT}.
12	CE IN	High impedance
13	BATT ON	Logic high. The open-circuit output voltage is equal to V_{BATT}.
14	BATT	Supply current is 1µA maximum for $V_{BATT} \leq 2.8V$.
15	BATT OK	Logic high when V_{BATT} exceeds 2.285V. Valid for $V_{CC} \geq 4V$. Below 4V, BATT OK is forced low.
16	OUT	OUT is connected to BATT through two internal PMOS switches in series.

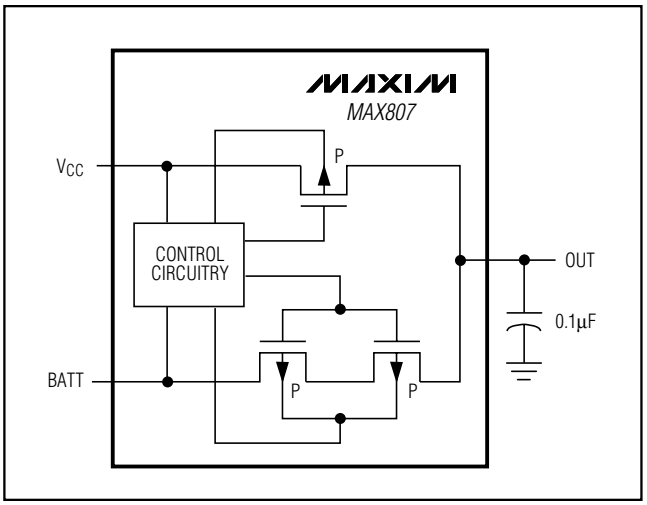


Figure 12. V_{CC} and BATT-to-OUT Switch

Battery-Backup Mode

Battery backup preserves the contents of RAM in the event of a brownout or power failure. With a backup battery installed at BATT, the MAX807 automatically switches RAM to backup power when V_{CC} falls. Two conditions are required for switchover to battery-backup mode: 1) V_{CC} must be below the reset threshold; 2) V_{CC} must be below V_{BATT}. Table 1 lists the status of inputs and outputs during battery-backup mode.

Backup-Battery Input

The BATT input is similar to V_{CC}, except the PMOS switch is much smaller. This input is designed to conduct up to 20mA to OUT during battery backup. The on-resistance of the PMOS switch is approximately 13Ω. Figure 12 shows the two series pass elements between the BATT input and OUT that facilitate UL approval. V_{BATT} can exceed V_{CC} during normal operation without causing a reset.

Output Supply Voltage

The output supply (OUT) transfers power from V_{CC} or BATT to the µP, RAM, and other external circuitry. At the maximum source current of 250mA, V_{OUT} will typically be 260mV below V_{CC}. Decouple this terminal with a 0.1µF capacitor.

BATT ON Output

The battery on (BATT ON) output indicates the status of the internal battery switchover comparator, which controls the internal V_{CC} and BATT switches. For V_{CC} greater than V_{BATT} (ignoring the small hysteresis effect), BATT ON typically sinks 3.2mA at 0.4V. In battery-backup mode, this output sources approximately 5mA. Use BATT ON to indicate battery switchover status, or to supply gate or base drive for an external pass transistor for higher current applications (see the *Typical Operating Circuit*).

Full-Featured µP Supervisory Circuit with ±1.5% Reset Accuracy

BATT OK Output

The BATT OK comparator monitors the backup battery voltage, comparing it with a 2.265V reference (V_{CC} ≥ 4V). BATT OK remains high as long as the backup battery voltage remains above 2.265V, signaling that the backup battery has sufficient voltage to maintain the memory of static RAM. When the battery voltage drops below 2.265V, the BATT OK output drops low, signaling that the backup battery needs to be changed.

Applications Information

The MAX807 is not short-circuit protected. Shorting OUT to ground, other than power-up transients such as charging a decoupling capacitor, may destroy the device. If long leads connect to the IC's inputs, ensure that these lines are free from ringing and other conditions that would forward bias the IC's protection diodes.

There are two distinct modes of operation:

1) Normal Operating Mode, with all circuitry powered up. Typical supply current from V_{CC} is 70µA, while only leakage currents flow from the battery.
2) Battery-Backup Mode, where V_{CC} is below V_{BATT} and V_{RST}. The supply current from the battery is typically less than 1µA.

Using SuperCaps or MaxCaps with the MAX807

BATT has the same operating voltage range as V_{CC}, and the battery-switchover threshold voltage is typically V_{BATT} when V_{CC} is decreasing or V_{BATT} + 0.06V when V_{CC} is increasing. This hysteresis allows use of a SuperCap (e.g., order of 0.47F) and a simple charging circuit as a backup source (Figure 13). Since V_{BATT} can exceed V_{CC} while V_{CC} is above the reset threshold, there are no special precautions when using these µP supervisors with a SuperCap.

Alternative Chip-Enable Gating

Using memory devices with CE and $\overline{CE}$ inputs allows the MAX807 CE loop to be bypassed. To do this, connect CE IN to ground, pull up $\overline{CE}$ OUT to OUT, and connect $\overline{CE}$ OUT to the CE input of each memory device (Figure 14). The CE input of each part then connects directly to the chip-select logic, which does not have to be gated by the MAX807.

Adding Hysteresis to the Power-Fail Comparator

The power-fail comparator has a typical input hysteresis of 20mV. This is sufficient for most applications where a power-supply line is being monitored through an external voltage-divider (Figure 10).

Figure 15 shows how to add hysteresis to the power-fail comparator. Select the ratio of R1 and R2 such that PFI sees 2.265V when V_{IN} falls to the desired trip point (V_{TRIP}). Resistor R3 adds hysteresis. It will typically be an order of magnitude greater than R1 or R2. The current through R1 and R2 should be at least 1µA to ensure that the 25nA (max) PFI input current does not shift the trip point. R3 should be larger than 10kΩ to prevent it from loading down the PFO pin. Capacitor C1 adds additional noise rejection.

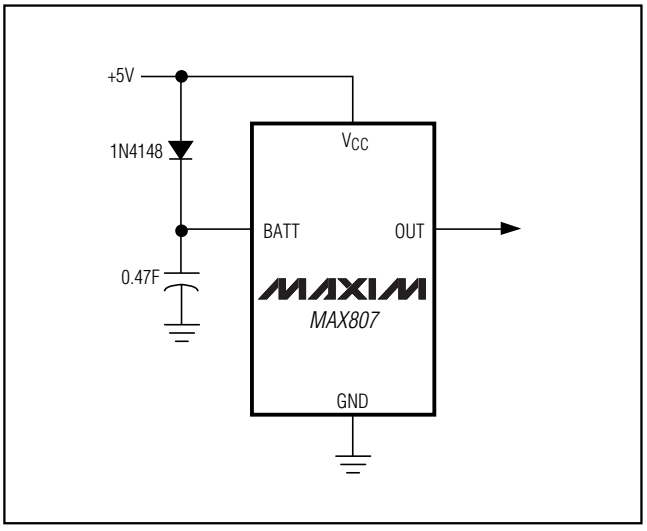


Figure 13. SuperCap or MaxCap on BATT

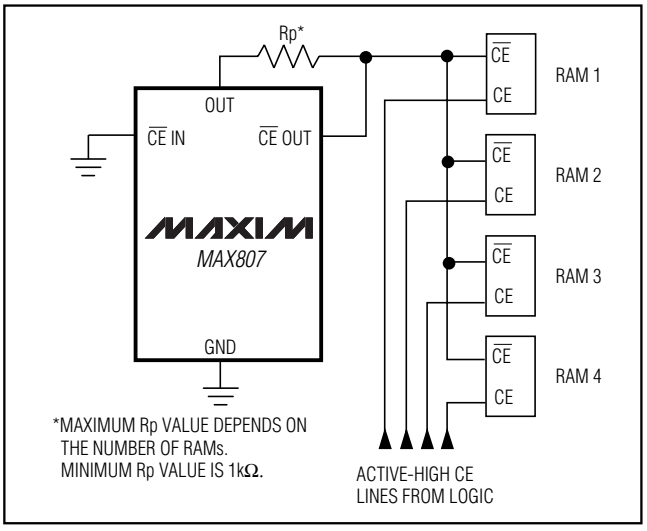


Figure 14. Alternate CE Gating

Backup-Battery Replacement

The backup battery may be disconnected while V_{CC} is above the reset threshold, provided BATT is bypassed with a 0.1µF capacitor to ground. No precautions are necessary to avoid spurious reset pulses.

Negative-Going Vcc Transients

While issuing resets to the µP during power-up, power-down, and brownout conditions, these supervisors are relatively immune to short-duration negative-going V_{CC} transients (glitches). It is usually undesirable to reset the µP when V_{CC} experiences only small glitches.

The *Typical Operating Characteristics* show Maximum Transient Duration vs. Reset Comparator Overdrive, for which reset pulses are not generated. The graph was produced using negative-going V_{CC} pulses, starting at 5V and ending below the reset threshold by the magnitude indicated (reset comparator overdrive). The graph shows the maximum pulse width that a negative-going V_{CC} transient may typically have without causing a reset pulse to be issued. As the amplitude of the transient increases (i.e., goes farther below the reset threshold), the maximum allowable pulse width decreases.

Typically, a V_{CC} transient that goes 40mV below the reset threshold and lasts for 3µs or less will not cause a reset pulse to be issued.

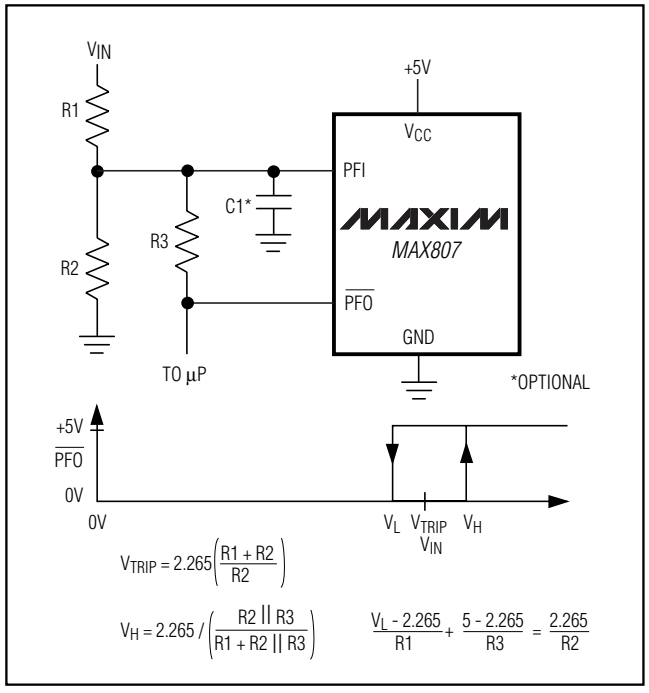


Figure 15. Adding Hysteresis to the Power-Fail Comparator

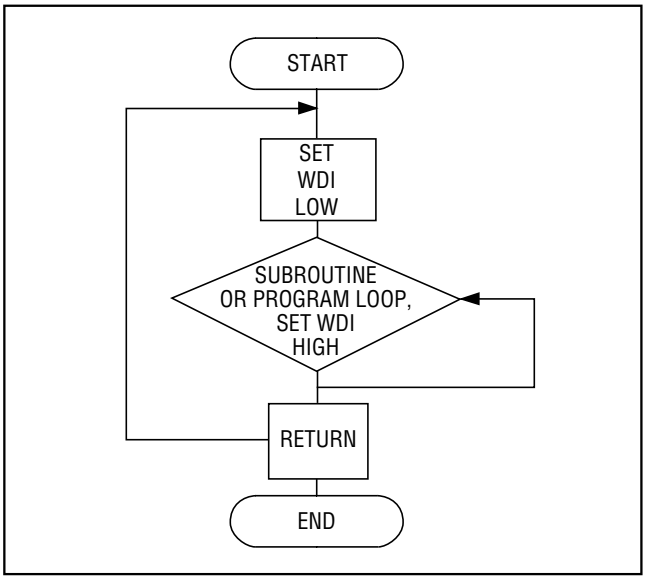


Figure 16. Watchdog Flow Diagram

A 0.1µF bypass capacitor mounted close to the V_{CC} pin provides additional transient immunity.

Watchdog Software Considerations

To help the watchdog timer keep a closer watch on software execution, you can use the method of setting and resetting the watchdog input at different points in the program, rather than "pulsing" the watchdog input high-low-high or low-high-low. This technique avoids a "stuck" loop where the watchdog timer continues to be reset within the loop, keeping the watchdog from timing out.

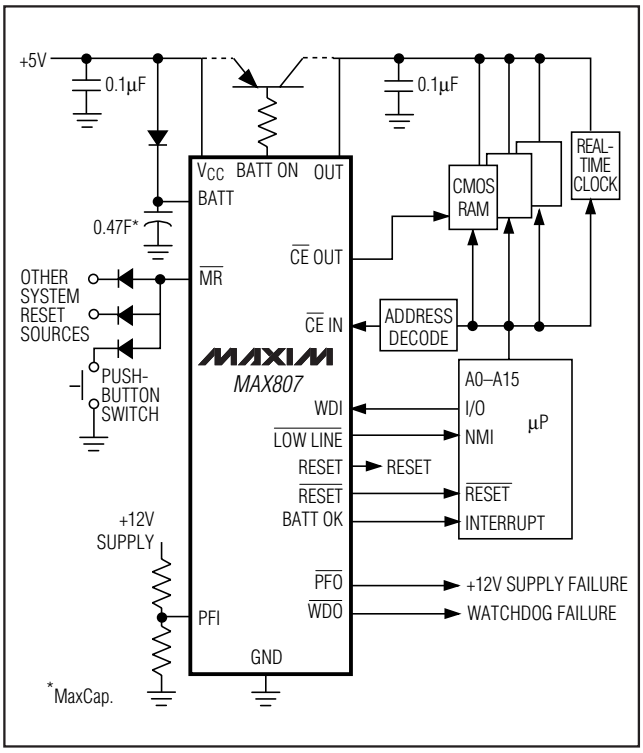
Figure 16 shows an example flow diagram where the I/O driving the watchdog input is set high at the beginning of the program, set low at the beginning of every subroutine or loop, then set high again when the program returns to the beginning. If the program should "hang" in any subroutine, the I/O is continually set low and the watchdog timer is allowed to time out, causing a reset or interrupt to be issued.

Maximum Vcc Fall Time

The V_{CC} fall time is limited by the propagation delay of the battery switchover comparator and should not exceed 0.03V/µs. A standard rule for filter capacitance on most regulators is on the order of 100µF per amp of current. When the power supply is shut off or the main battery is disconnected, the associated initial V_{CC} fall rate is just the inverse or 1A / 100µF = 0.01V/µs. The V_{CC} fall rate decreases with time as V_{CC} falls exponentially, which more than satisfies the maximum fall-time requirement.

Full-Featured µP Supervisory Circuit with ±1.5% Reset Accuracy

Typical Operating Circuit



Ordering Information

PART†	TEMP RANGE	PIN-PACKAGE
MAX807_CPE	0°C to +70°C	16 Plastic DIP
MAX807_CUE	0°C to +70°C	16 TSSOP
MAX807_CWE	0°C to +70°C	16 Wide SO
MAX807_EPE	-40°C to +85°C	16 Plastic DIP
MAX807_EUE	-40°C to +85°C	16 TSSOP
MAX807_EWE	-40°C to +85°C	16 Wide SO
MAX807_MJE	-55°C to +125°C	16 CERDIP

† This part offers a choice of reset threshold voltage. From the table below, select the suffix corresponding to the desired threshold and insert it into the blank to complete the part number.

Devices in PDIP, SO and TSSOP packages are available in both leaded and lead-free packaging. Specify lead free by adding the + symbol at the end of the part number when ordering. Lead free not available for CERDIP package.

SUFFIX	RESET THRESHOLD (V)		
	MIN	TYP	MAX
L	4.60	4.675	4.75
N	4.50	4.575	4.65
M	4.35	4.425	4.50

Chip Information

TRANSISTOR COUNT: 984

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Maxim Integrated:

MAX807LCWE+ MAX807NCWE+ MAX807NEWE+ MAX807LCPE+ MAX807LCUE+ MAX807LCUE+T MAX807LCWE+T MAX807LEPE+ MAX807LEUE+ MAX807LEUE+T MAX807LEWE+ MAX807LEWE+T MAX807MCPE+ MAX807MCUE+ MAX807MCUE+T MAX807MCWE+ MAX807MCWE+T MAX807MEPE+ MAX807MEUE+ MAX807MEUE+T MAX807MEWE+ MAX807MEWE+T MAX807NCPE+ MAX807NCUE+ MAX807NCUE+T MAX807NCWE+T MAX807NEPE+ MAX807NEUE+ MAX807NEUE+T MAX807NEWE+T