ABSOLUTE MAXIMUM RATINGS

V_{DD} to V_{SS} .....-0.3V to +100V
DET, RTN, WAD, PG, $\overline{2EC}$ to V_{SS} .....-0.3V to +100V
CLS to V_{SS} .....-0.3V to +6V
Maximum Current on CLS (100ms maximum).....100mA
Continuous Power Dissipation (T_A = +70°C) (Note 1)
10-Pin TDFN (derate 24.4mW/°C above +70°C)
Multilayer Board 1951mW

Operating Temperature Range ..... -40°C to +85°C
Maximum Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 2)

Junction-to-Ambient Thermal Resistance (θ_{JA})..... 4°C/W
Junction-to-Case Thermal Resistance (θ_{JC})..... 9°C/W

Note 1: Maximum power dissipation is obtained using JEDEC JESD51-5 and JESD51-7 specifications.
Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{IN} = (V_{DD} - V_{SS}) = 48V, R_{DET} = 24.9kΩ, R_{CLS} = 619Ω. RTN, WAD, PG, and $\overline{2EC}$ unconnected, all voltages are referenced to V_{SS}, unless otherwise noted. T_A = T_J = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DETECTION MODE							
Input Offset Current	I_{OFFSET}	V_{IN} = 1.4V to 10.1V (Note 4)				10	µA
Effective Differential Input Resistance	dR	V_{IN} = 1.4V up to 10.1V with 1V step, V_{DD} = RTN = WAD = PG = $\overline{2EC}$ (Note 5)		23.95	25.00	25.5	kΩ
CLASSIFICATION MODE							
Classification Disable Threshold	$V_{TH,CLS}$	V_{IN} rising (Note 6)		22.0	22.8	23.6	V
Classification Stability Time					0.2		ms
Classification Current	I_{CLASS}	V_{IN} = 12.5V to 20.5V, V_{DD} = RTN = WAD = PG = $\overline{2EC}$	Class 0, R_{CLS} = 619Ω	0		3.96	mA
			Class 1, R_{CLS} = 117Ω	9.12		11.88	
			Class 2, R_{CLS} = 66.5Ω	17.2		19.8	
			Class 3, R_{CLS} = 43.7Ω	26.3		29.7	
			Class 4, R_{CLS} = 30.9Ω	36.4		43.6	
			Class 5, R_{CLS} = 21.3Ω	52.7		63.3	
TYPE 2 (802.3at) CLASSIFICATION MODE							
Mark Event Threshold	V_{THM}	V_{IN} falling		10.1	10.7	11.6	V
Hysteresis on Mark Event Threshold					0.84		V
Mark Event Current	I_{MARK}	V_{IN} falling to enter mark event, 5.2V ≤ V_{IN} ≤ 10.1V		0.25		0.85	mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = (V_{DD} - V_{SS}) = 48V, R_{DET} = 24.9kΩ, R_{CLS} = 619Ω. RTN, WAD, PG, and $\overline{2EC}$ unconnected, all voltages are referenced to V_{SS}, unless otherwise noted. T_A = T_J = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Reset Event Threshold	V_{THR}	V_{IN} falling		2.8	4	5.2	V
POWER MODE							
V_{IN} Supply Voltage Range						60	V
V_{IN} Supply Current	I_Q	Measured at V_{DD}			0.27	0.55	mA
V_{IN} Turn-On Voltage	V_{ON}	V_{IN} rising	MAX5969A	34.3	35.4	36.6	V
			MAX5969B	37.2	38.6	40	
V_{IN} Turn-Off Voltage	V_{OFF}	V_{IN} falling		30			V
V_{IN} Turn-On/-Off Hysteresis (Note 7)	V_{HYST_UVLO}	MAX5969A		4.2			V
		MAX5969B		7.3			
V_{IN} Deglitch Time	t_{OFF_DLY}	V_{IN} falling from 40V to 20V (Note 8)		30	120		µs
Inrush to Operating Mode Delay	t_{DELAY}	t_{DELAY} = minimum PG current pulse width after entering into power mode		80	96	112	ms
Isolation Power MOSFET On-Resistance	R_{ON_ISO}	I_{RTN} = 600mA	T_J = +25°C		0.5	0.7	Ω
			T_J = +85°C		0.65	1	
			T_J = +125°C		0.8		
RTN Leakage Current	I_{RTN_LKG}	V_{RTN} = 12.5V to 30V				10	µA
CURRENT LIMIT							
Inrush Current Limit	I_{INRUSH}	During initial turn-on period, V_{RTN} = 1.5V		90	135	180	mA
Current Limit During Normal Operation	I_{LIM}	After inrush completed, V_{RTN} = 1V		720	800	880	mA
Foldback Threshold		V_{RTN} (Note 9)		13		16.5	V
LOGIC							
WAD Detection Threshold	$V_{WAD-REF}$	V_{WAD} rising, V_{IN} = 14V to 48V (referenced to RTN)		8	9	10	V
WAD Detection Threshold Hysteresis		V_{WAD} falling, V_{RTN} = 0V, V_{SS} unconnected			0.725		
WAD Input Current	$I_{WAD-LKG}$	V_{WAD} = 10V (referenced to RTN)				3.5	µA
$\overline{2EC}$ Sink Current		$V_{\overline{2EC}}$ = 3.5V (referenced to RTN), V_{SS} unconnected		1	1.5	2.25	mA
$\overline{2EC}$ Off-Leakage Current		$V_{\overline{2EC}}$ = 48V				1	µA
PG Sink Current		V_{RTN} = 1.5V, V_{PG} = 0.8V, during inrush period		125	230	375	µA
PG Off-Leakage Current		V_{PG} = 48V				1	µA
THERMAL SHUTDOWN							
Thermal-Shutdown Threshold	T_{SD}	T_J rising			+140		°C
Thermal-Shutdown Hysteresis		T_J falling			28		°C

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = (V_{DD} - V_{SS}) = 48V, R_{DET} = 24.9kΩ, R_{CLS} = 619Ω. RTN, WAD, PG, and $\overline{2EC}$ unconnected, all voltages are referenced to V_{SS}, unless otherwise noted. T_A = T_J = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

Note 3: All devices are 100% production tested at T_A = +25°C. Limits over temperature are guaranteed by design.

Note 4: The input offset current is illustrated in Figure 1.

Note 5: Effective differential input resistance is defined as the differential resistance between V_{DD} and V_{SS}. See Figure 1.

Note 6: Classification current is turned off whenever the device is in power mode.

Note 7: UVLO hysteresis is guaranteed by design, not production tested.

Note 8: A 20V glitch on input voltage that takes V_{DD} below V_{ON} shorter than or equal to t_{OFF_DLY} does not cause the MAX5969A/MAX5969B to exit power-on mode.

Note 9: In power mode, current-limit foldback is used to reduce the power dissipation in the isolation MOSFET during an overload condition across V_{DD} and RTN.

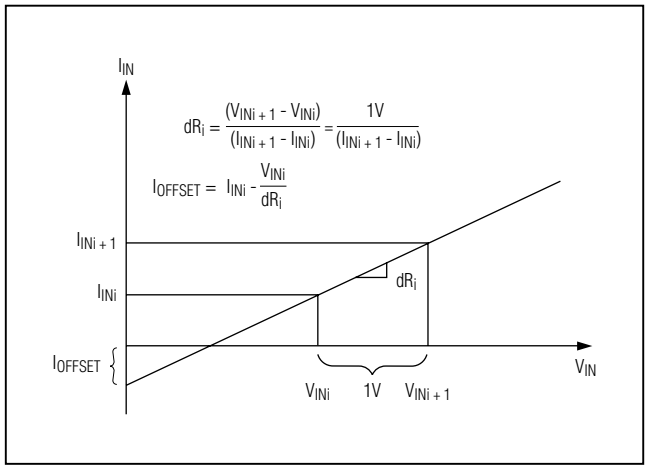
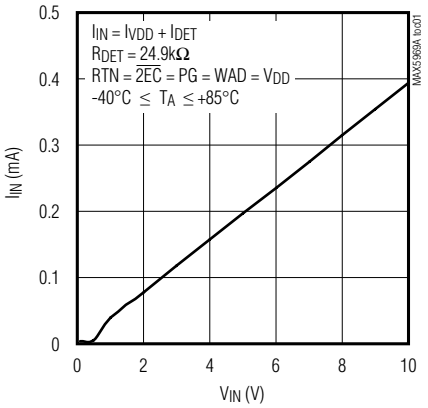


Figure 1. Effective Differential Input Resistance/Offset Current

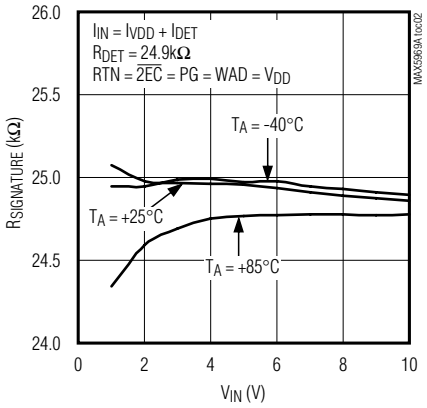
Typical Operating Characteristics

(V_{IN} = (V_{DD} - V_{SS}) = 54V, R_{DET} = 24.9kΩ, R_{CLS} = 615Ω. RTN, WAD, PG, and $\overline{2EC}$ unconnected; all voltages are referenced to V_{SS}.)

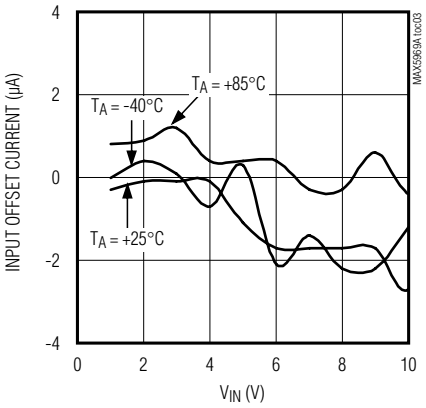
INPUT CURRENT (DETECTION) vs. INPUT VOLTAGE



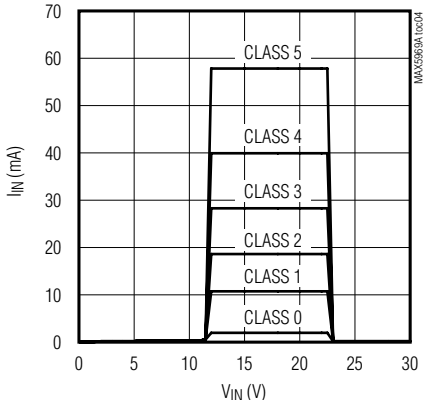
SIGNATURE RESISTANCE vs. INPUT VOLTAGE



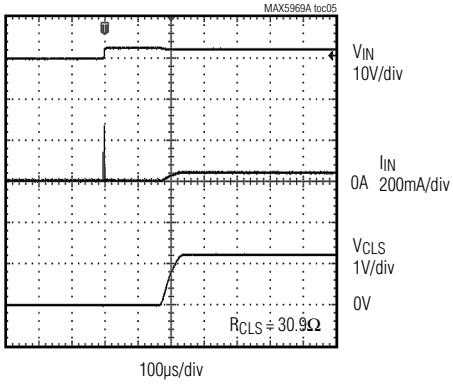
INPUT OFFSET CURRENT vs. INPUT VOLTAGE



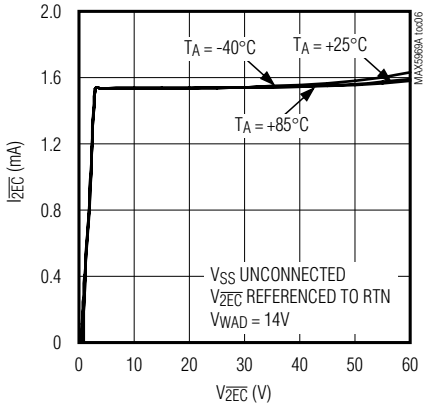
INPUT CURRENT (CLASSIFICATION) vs. INPUT VOLTAGE



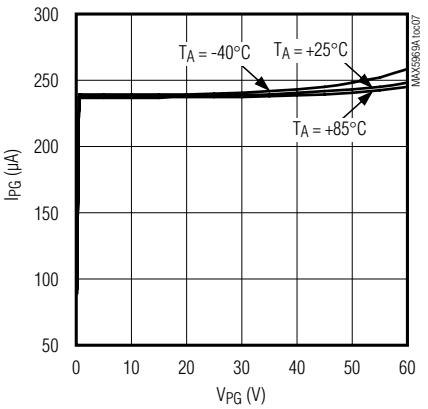
CLASSIFICATION SETTLING TIME



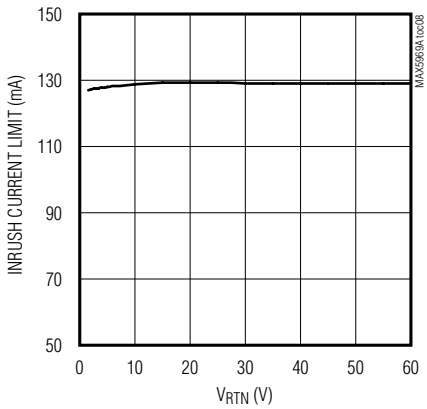
2EC SINK CURRENT vs. 2EC VOLTAGE



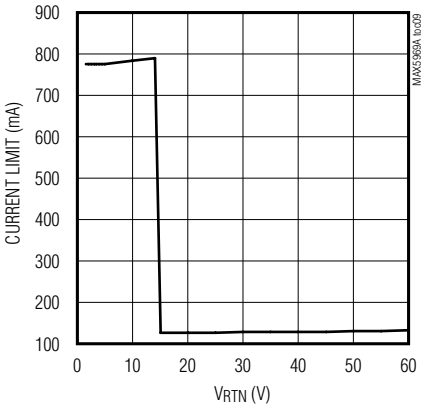
PG SINK CURRENT vs. PG VOLTAGE



INRUSH CURRENT LIMIT vs. RTN VOLTAGE



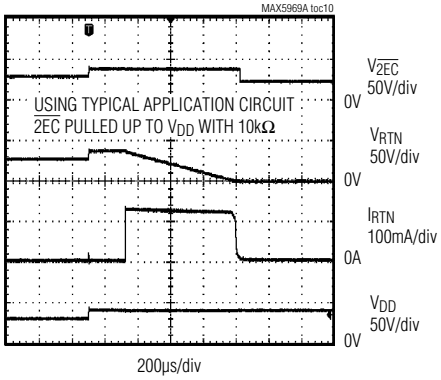
NORMAL OPERATION CURRENT LIMIT vs. RTN VOLTAGE



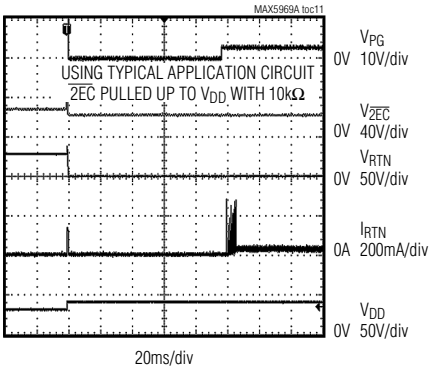
Typical Operating Characteristics (continued)

(V_{IN} = (V_{DD} - V_{SS}) = 54V, R_{DET} = 24.9kΩ, R_{CLS} = 615Ω. RTN, WAD, PG, and $\overline{2EC}$ unconnected; all voltages are referenced to V_{SS}.)

INRUSH CONTROL WAVEFORM WITH TYPE 2 CLASSIFICATION



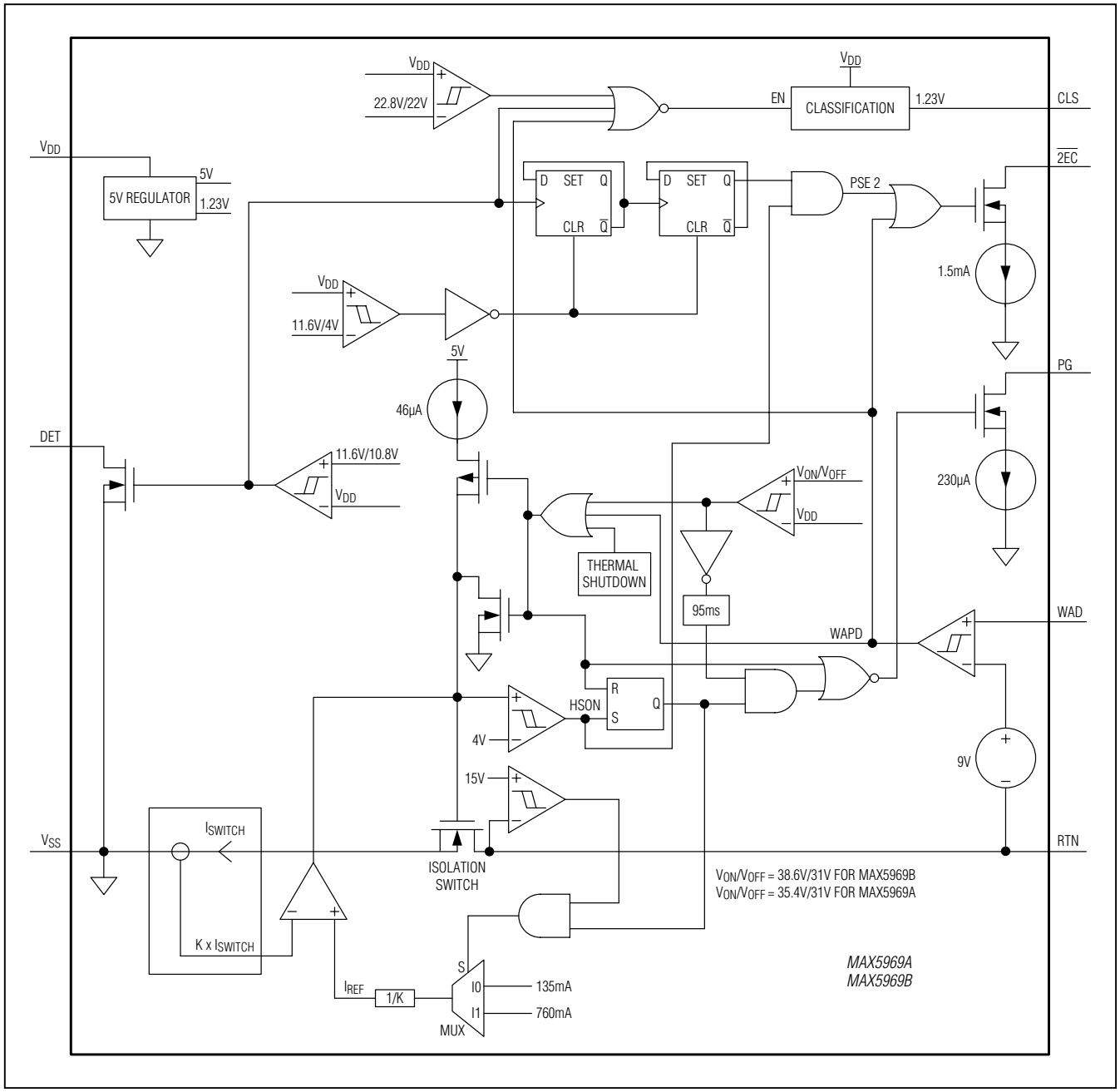
ENTERING POWER MODE WITH TYPE 2 CLASSIFICATION



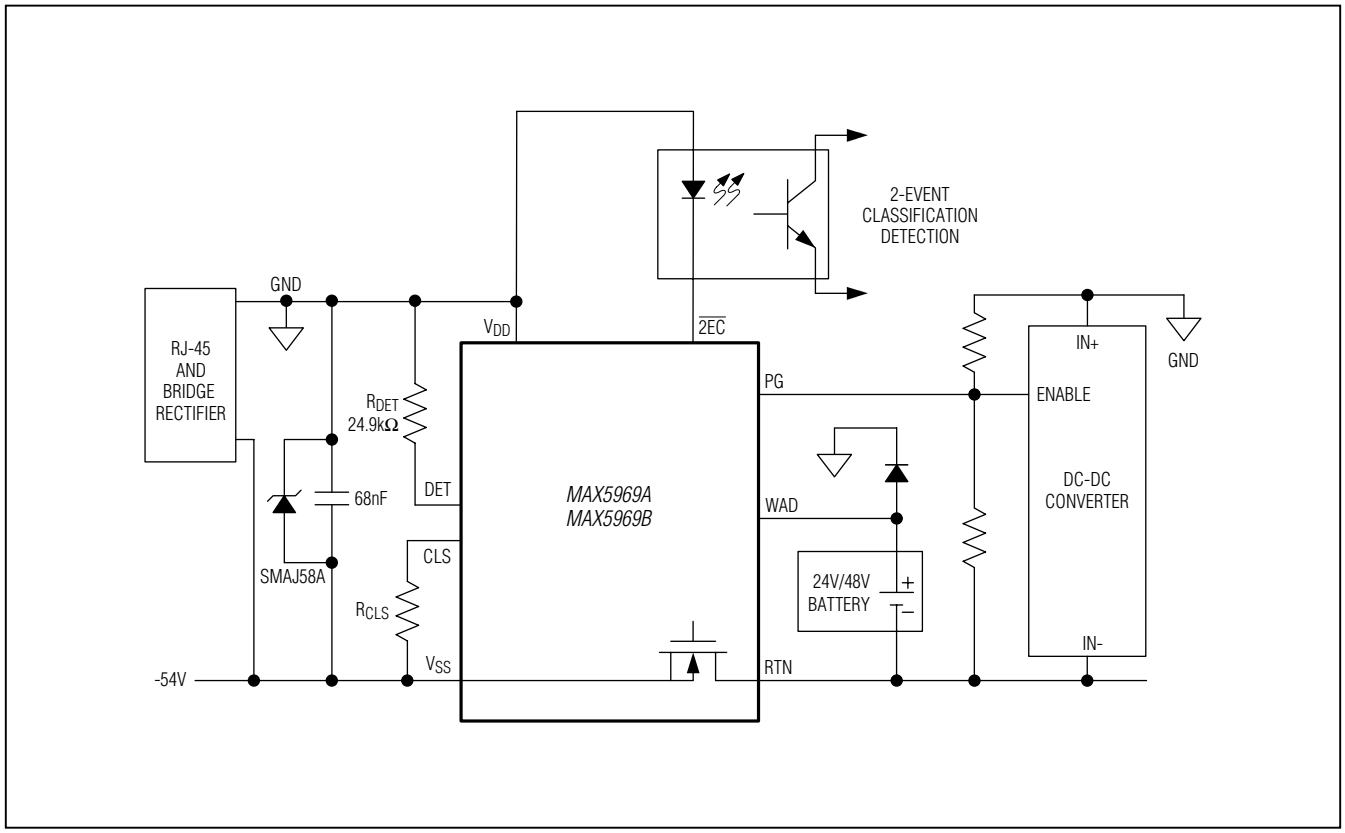
Pin Description

PIN	NAME	FUNCTION
1	V_{DD}	Positive Supply Input. Connect a 68nF (min) bypass capacitor between V_{DD} and V_{SS}.
2	DET	Detection Resistor Input. Connect a signature resistor (R_{DET} = 24.9kΩ) from DET to V_{DD}.
3	N.C.	No Connection. Not internally connected.
4	I.C.	Internally Connected. Leave unconnected.
5	V_{SS}	Negative Supply Input. V_{SS} connects to the source of the integrated isolation n-channel power MOSFET.
6	RTN	Drain of Isolation MOSFET. RTN connects to the drain of the integrated isolation n-channel power MOSFET. Connect RTN to the downstream DC-DC converter ground as shown in the *Typical Application Circuit*.
7	WAD	Wall Power Adapter Detector Input. Wall adapter detection is enabled the moment V_{DD} - V_{SS} crosses the mark event threshold. Detection occurs when the voltage from WAD to RTN is greater than 9V. When a wall power adapter is present, the isolation n-channel power MOSFET turns off, $\overline{2EC}$ current sink turns on. Connect WAD directly to RTN when the wall power adapter or other auxiliary power source is not used.
8	PG	Open-Drain Power-Good Indicator Output. PG sinks 230µA to disable the downstream DC-DC converter while turning on the hot-swap MOSFET switch until the hot-swap switch is fully on. PG current sink is disabled during detection, classification, and in the steady-state power mode.
9	$\overline{2EC}$	Active-Low 2-Event Classification Detect or Wall Adapter Detect Output. A 1.5mA current sink is enabled at $\overline{2EC}$ when a Type 2 PSE or a wall adapter is detected. When powered by a Type 2 PSE, the $\overline{2EC}$ current sink is enabled and latched low after the isolation MOSFET is fully on until V_{IN} drops below the UVLO threshold. $\overline{2EC}$ also asserts when a wall adapter supply, typically greater than 9V, is applied between WAD and RTN. $\overline{2EC}$ is not latched if asserted by WAD.
10	CLS	Classification Resistor Input. Connect a resistor (R_{CLS}) from CLS to V_{SS} to set the desired classification current. See the classification current specifications in the *Electrical Characteristics* table to find the resistor value for a particular PD classification.
—	EP	Exposed Pad. Do not use EP as an electrical connection to V_{SS}. EP is internally connected to V_{SS} through a resistive path and must be connected to V_{SS} externally. To optimize power dissipation, solder the exposed pad to a large copper power plane.

Simplified Block Diagram



Typical Operating Circuit



Detailed Description

Operating Modes

Depending on the input voltage (V_{IN} = V_{DD} - V_{SS}), the MAX5969A/MAX5969B operate in four different modes: PD detection, PD classification, mark event, and PD power. The devices enter PD detection mode when the input voltage is between 1.4V and 10.1V. The device enters PD classification mode when the input voltage is between 12.6V and 20V. The device enters PD power mode once the input voltage exceeds V_{ON}.

Detection Mode (1.4V ≤ V_{IN} ≤ 10.1V)

In detection mode, the PSE applies two voltages on V_{IN} in the range of 1.4V to 10.1V (1V step minimum) and then records the current measurements at the two points. The PSE then computes ΔV/ΔI to ensure the presence of the 24.9kΩ signature resistor. Connect the signature resistor (R_{DET}) from V_{DD} to DET for proper signature detection. The MAX5969A/MAX5969B pull DET low in detection mode. DET goes high impedance when the input voltage exceeds 12.5V. In detection mode, most of the MAX5969A/MAX5969B internal circuitry is off and the offset current is less than 10µA.

If the voltage applied to the PD is reversed, install protection diodes at the input terminal to prevent internal damage to the MAX5969A/MAX5969B (see the *Typical Application Circuit*). Since the PSE uses a slope technique (ΔV/ΔI) to calculate the signature resistance, the DC offset due to the protection diodes is subtracted and does not affect the detection process.

Classification Mode (12.6V ≤ V_{IN} ≤ 20V)

In the classification mode, the PSE classifies the PD based on the power consumption required by the PD. This allows the PSE to efficiently manage power distribution. Class 0 to 5 is defined as shown in Table 1. (The IEEE 802.3af/at standard defines only Class 0 to 4 and Class 5 for any special requirement.) An external resistor (R_{CLS}) connected from CLS to V_{SS} sets the classification current.

The PSE determines the class of a PD by applying a voltage at the PD input and measuring the current sourced out of the PSE. When the PSE applies a voltage between 12.6V and 20V, the MAX5969A/MAX5969B exhibit a current characteristic with a value shown in Table 1. The PSE uses the classification current information to classify the power requirement of the PD. The classification current includes the current drawn by R_{CLS} and the supply current of the MAX5969A/MAX5969B so the total current drawn by the PD is within the IEEE 802.3af/at standard figures. The classification current is turned off whenever the device is in power mode.

2-Event Classification and Detection

During 2-event classification, a Type 2 PSE probes PD for classification twice. In the first classification event, the PSE presents an input voltage between 12.6V and 20V and the MAX5969A/MAX5969B present the programmed load I_{CLASS}. The PSE then drops the probing voltage below the mark event threshold of 10.1V and the MAX5969A/MAX5969B present the mark current (I_{MARK}). This sequence is repeated one more time.

Table 1. Setting Classification Current

CLASS	MAXIMUM POWER USED BY PD (W)	R_{CLS} (Ω)	V_{IN}* (V)	CLASS CURRENT SEEN AT V_{IN} (mA)		IEEE 802.3af/at PSE CLASSIFICATION CURRENT SPECIFICATION (mA)	
				MIN	MAX	MIN	MAX
0	0.44 to 12.95	619	12.6 to 20	0	4	0	5
1	0.44 to 3.94	117	12.6 to 20	9	12	8	13
2	3.84 to 6.49	66.5	12.6 to 20	17	20	16	21
3	6.49 to 12.95	43.7	12.6 to 20	26	30	25	31
4	12.95 to 25.5	30.9	12.6 to 20	36	44	35	45
5	> 25.5	21.3	12.6 to 20	52	64	—	—

**V_{IN} is measured across the MAX5969A/MAX5969B input V_{DD} to V_{SS}.*

When the MAX5969A/MAX5969B are powered by a Type 2 PSE, the 2-event identification output $\overline{2EC}$ asserts low after the internal isolation n-channel MOSFET is fully turned on. $\overline{2EC}$ current sink is turned off when V_{DD} goes below the UVLO threshold (V_{OFF}) and turns on when V_{DD} goes above the UVLO threshold (V_{ON}), unless V_{DD} goes below V_{THR} to reset the latched output of the Type 2 PSE detection flag.

Alternatively, the $\overline{2EC}$ output also serves as a wall adapter detection output when the MAX5969A/MAX5969B are powered by an external wall power adapter. See the *Wall Power Adapter Detection and Operation* section for more information.

Power Mode (Wake Mode)

The MAX5969A/MAX5969B enter power mode when V_{IN} rises above the undervoltage lockout threshold (V_{ON}). When V_{IN} rises above V_{ON}, the MAX5969A/MAX5969B turn on the internal n-channel isolation MOSFET to connect V_{SS} to RTN with inrush current limit internally set to 135mA (typ). The isolation MOSFET is fully turned on when the voltage at RTN is near V_{SS} and the inrush current is reduced below the inrush limit. Once the isolation MOSFET is fully turned on, the MAX5969A/MAX5969B change the current limit to 800mA. The open-drain power-good output (PG) remains low for a minimum of t_{DELAY} until the power MOSFET fully turns on to keep the downstream DC-DC converter disabled during inrush.

Undervoltage Lockout

The MAX5969A/MAX5969B operate up to a 60V supply voltage with a turn-on UVLO threshold (V_{ON}) at 35.4V/38.6V and a turn-off UVLO threshold (V_{OFF}) at 31V. When the input voltage is above V_{ON}, the MAX5969A/MAX5969B enter power mode and the internal MOSFET is turned on. When the input voltage goes below V_{OFF} for more than t_{OFF_DLY}, the MOSFET turns off.

Power-Good Output

The enable pin of the downstream DC-DC control may see up to 375µA sinking current from PG to V_{SS}. To be safe, make sure the downstream controller is capable of handling 375µA current out from the enable pin or adding a circuit to satisfy the absolute maxim rating of the enable pin.

Thermal-Shutdown Protection

The MAX5969A/MAX5969B include thermal protection from excessive heating. If the junction temperature exceeds the thermal-shutdown threshold of +140°C, the MAX5969A/MAX5969B turn off the internal power MOSFET and $\overline{2EC}$ current sink. When the junction temperature falls below +112°C, the devices enter inrush mode and then return to power mode. Inrush mode ensures the downstream DC-DC converter is turned off as the internal power MOSFET is turned on.

Wall Power Adapter Detection and Operation

For applications where an auxiliary power source such as a wall power adapter is used to power the PD, the MAX5969A/MAX5969B feature wall power adapter detection. Once the input voltage (V_{DD} - V_{SS}) exceeds the mark event threshold, the MAX5969A/MAX5969B enable wall adapter detection. The wall power adapter is connected from WAD to RTN. The MAX5969A/MAX5969B detect the wall power adapter when the voltage from WAD to RTN is greater than 9V. When a wall power adapter is detected, the internal n-channel isolation MOSFET turns off, $\overline{2EC}$ current sink turns on, and classification current is disabled if V_{IN} is in the classification range.

Applications Information

Operation with 12V Adapter

Layout Procedure

Careful PCB layout is critical to achieve high efficiency and low EMI. Follow these layout guidelines for optimum performance:

1) Place the input capacitor, classification resistor, and transient voltage suppressor as close as possible to the MAX5969A/MAX5969B.
2) Use large SMT component pads for power dissipating devices such as the MAX5969A/MAX5969B and the external diodes.
3) Use short and wide traces for high-power paths.
4) Use the MAX5969 Evaluation Kit layout as a reference.

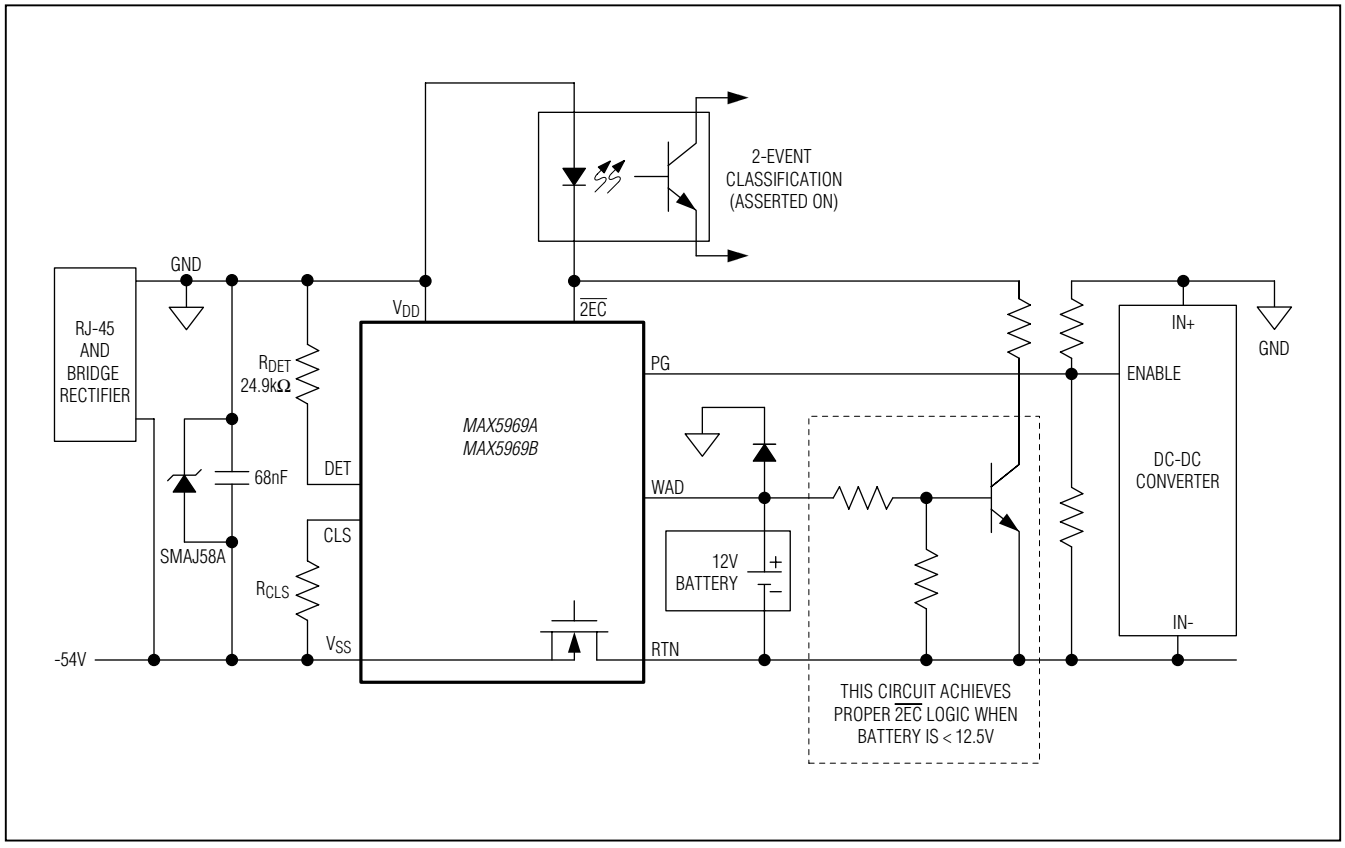
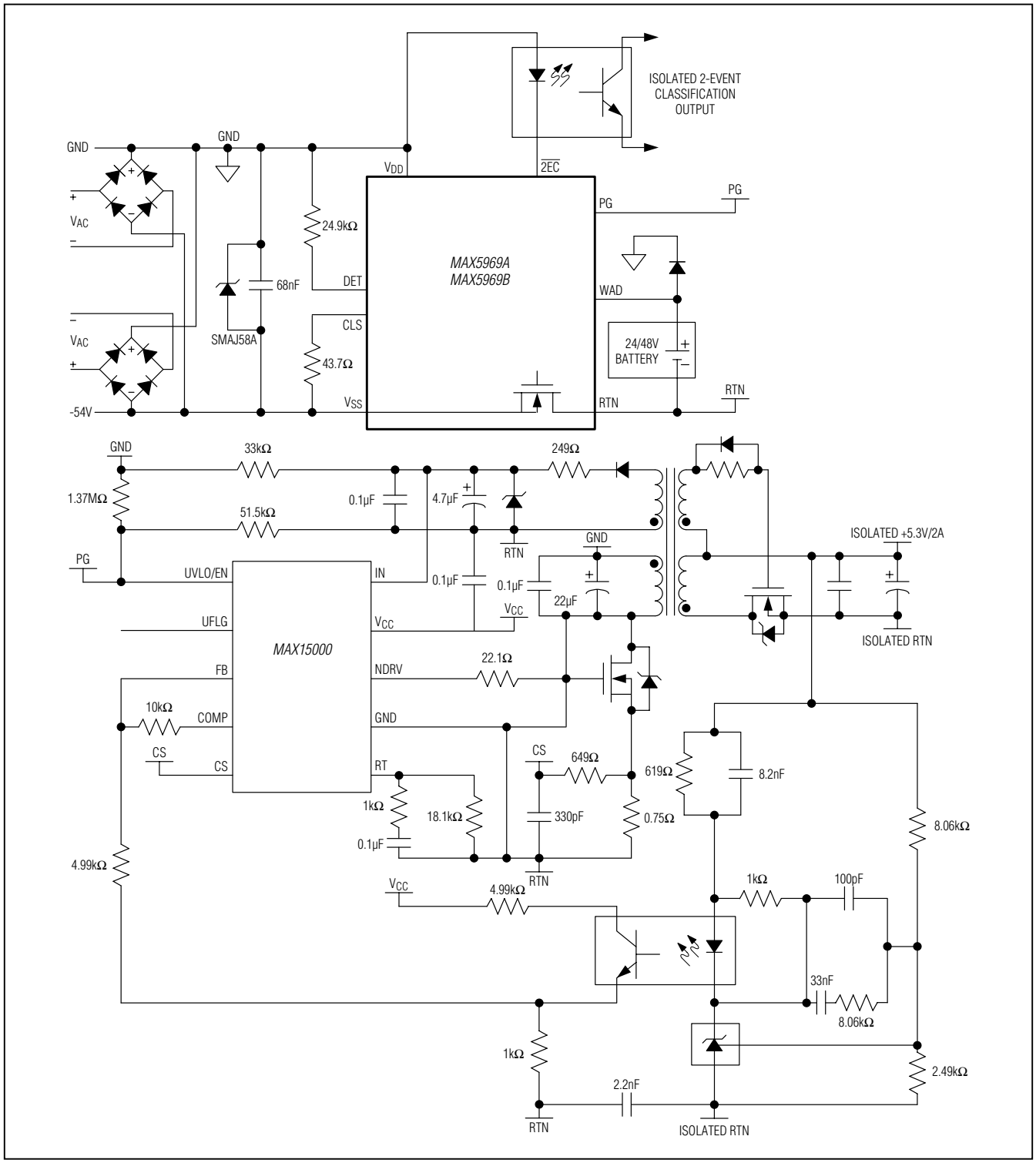


Figure 2. Typical Configuration When Using a 12V Wall Power Adapter

Typical Application Circuit



Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
10 TDFN-EP	T1033+1	21-0137

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/09	Initial release	—
1	7/15	Revised *Power-Good Output* section	11

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