2.7V to 3.6V and 4.5V to 5.5V, Low-Power, 4-/12-Channel, 2-Wire Serial 10-Bit ADCs

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +6V
AIN0–AIN11,
REF to GND .....-0.3V to the lower of (V_{DD} + 0.3V) and 6V
SDA, SCL to GND.....-0.3V to +6V
Maximum Current Into Any Pin .....±50mA
Continuous Power Dissipation (T_A = +70°C)
8-Pin µMAX (derate 5.9mW/°C above +70°C) 470.6mW
16-Pin QSOP (derate 8.3mW/°C above +70°C).....666.7mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.7V to 3.6V (MAX1137/MAX1139), V_{DD} = 4.5V to 5.5V (MAX1136/MAX1138), V_{REF} = 2.048V (MAX1137/MAX1139), V_{REF} = 4.096V (MAX1136/MAX1138), f_{SCL} = 1.7MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. See Tables 1–5 for programming notation.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)						
Resolution			10			Bits
Relative Accuracy	INL	(Note 2)			±1	LSB
Differential Nonlinearity	DNL	No missing codes over temperature			±1	LSB
Offset Error					±1	LSB
Offset-Error Temperature Coefficient		Relative to FSR		0.3		ppm/°C
Gain Error		(Note 3)			±1	LSB
Gain-Temperature Coefficient		Relative to FSR		0.3		ppm/°C
Channel-to-Channel Offset Matching				±0.1		LSB
Channel-to-Channel Gain Matching				±0.1		LSB
DYNAMIC PERFORMANCE ($f_{IN(SINE-WAVE)}$ = 10kHz, $V_{IN(P-P)}$ = V_{REF}, f_{SAMPLE} = 94.4ksps)						
Signal-to-Noise Plus Distortion	SINAD			60		dB
Total Harmonic Distortion	THD	Up to the 5th harmonic		-70		dB
Spurious Free Dynamic Range	SFDR			70		dB
Full-Power Bandwidth		SINAD > 57dB		3.0		MHz
Full-Linear Bandwidth		-3dB point		5.0		MHz
CONVERSION RATE						
Conversion Time (Note 4)	t_{CONV}	Internal clock			6.8	µs
		External clock	10.6			
Throughput Rate	f_{SAMPLE}	Internal clock, SCAN[1:0] = 01		53		ksps
		Internal clock, SCAN[1:0] = 00 CS[3:0] = 1011 (MAX1138/MAX1139)		53		
		External clock		94.4		
Track/Hold Acquisition Time			800			ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 2.7V to 3.6V (MAX1137/MAX1139), V_{DD} = 4.5V to 5.5V (MAX1136/MAX1138), V_{REF} = 2.048V (MAX1137/MAX1139), V_{REF} = 4.096V (MAX1136/MAX1138), f_{SCL} = 1.7MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. See Tables 1–5 for programming notation.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Internal Clock Frequency					2.8		MHz
Aperture Delay (Note 5)	t_{AD}	External clock, fast mode			60		ns
		External clock, high-speed mode			30		
ANALOG INPUT (AIN0–AIN11)							
Input-Voltage Range, Single-Ended and Differential (Note 6)		Unipolar		0		V_{REF}	V
		Bipolar		0		$\pm V_{REF}/2$	
Input Multiplexer Leakage Current		ON/OFF leakage current, VAIN_ = 0 or VDD			±0.01	±1	µA
Input Capacitance	CIN				22		pF
INTERNAL REFERENCE (Note 7)							
Reference Voltage	VREF	T_A = +25°C	MAX1137/MAX1139	1.968	2.048	2.128	V
			MAX1136/MAX1138	3.939	4.096	4.256	
Reference-Voltage Temperature Coefficient	TCVREF				25		ppm/°C
REF Short-Circuit Current						2	mA
REF Source Impedance					1.5		kΩ
EXTERNAL REFERENCE							
REF Input-Voltage Range	VREF	(Note 8)		1		VDD	V
REF Input Current	IREF	f_{SAMPLE} = 94.4ksps				40	µA
DIGITAL INPUTS/OUTPUTS (SCL, SDA)							
Input High Voltage	V_{IH}			$0.7 \times V_{DD}$			V
Input Low Voltage	V_{IL}					$0.3 \times V_{DD}$	V
Input Hysteresis	V_{HYST}			$0.1 \times V_{DD}$			V
Input Current	I_{IN}	V_{IN} 0 to V_{DD}				±10	µA
Input Capacitance	C_{IN}				15		pF
Output Low Voltage	V_{OL}	I_{SINK} = 3mA				0.4	V
POWER REQUIREMENTS							
Supply Voltage	V_{DD}	MAX1137/MAX1139		2.7		3.6	V
		MAX1136/MAX1138		4.5		5.5	
Supply Current	I_{DD}	f_{SAMPLE} = 94.4ksps external clock	Internal reference		900	1150	µA
			External reference		670	900	
		f_{SAMPLE} = 40ksps internal clock	Internal reference		530		
			External reference		230		
		f_{SAMPLE} = 10ksps internal clock	Internal reference		380		
			External reference		60		
		f_{SAMPLE} =1ksps internal clock	Internal reference		330		
			External reference		6		
		Shutdown (internal reference OFF)			0.5	10	

2.7V to 3.6V and 4.5V to 5.5V, Low-Power, 4-/12-Channel, 2-Wire Serial 10-Bit ADCs

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 2.7V to 3.6V (MAX1137/MAX1139), V_{DD} = 4.5V to 5.5V (MAX1136/MAX1138), V_{REF} = 2.048V (MAX1137/MAX1139), V_{REF} = 4.096V (MAX1136/MAX1138), f_{SCL} = 1.7MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. See Tables 1–5 for programming notation.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER REQUIREMENTS						
Power-Supply Rejection Ratio	PSRR	Full-scale input (Note 9)		±0.01	±0.5	LSB/V

TIMING CHARACTERISTICS (Figure 1)

(V_{DD} = 2.7V to 3.6V (MAX1137/MAX1139), V_{DD} = 4.5V to 5.5V (MAX1136/MAX1138), V_{REF} = 2.048V (MAX1137/MAX1139), V_{REF} = 4.096V (MAX1136/MAX1138), f_{SCL} = 1.7MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. See Tables 1–5 for programming notation.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS FOR FAST MODE						
Serial Clock Frequency	f_{SCL}				400	kHz
Bus Free Time Between a STOP (P) and a START (S) Condition	t_{BUF}		1.3			µs
Hold Time for START (S) Condition	$t_{HD, STA}$		0.6			µs
Low Period of the SCL Clock	t_{LOW}		1.3			µs
High Period of the SCL Clock	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition (Sr)	$t_{SU, STA}$		0.6			µs
Data Hold Time	$t_{HD, DAT}$	(Note 10)	0		900	ns
Data Setup Time	$t_{SU, DAT}$		100			ns
Rise Time of Both SDA and SCL Signals, Receiving	t_R	Measured from $0.3V_{DD}$ to $0.7V_{DD}$	$20 + 0.1C_B$		300	ns
Fall Time of SDA Transmitting	t_F	Measured from $0.3V_{DD}$ to $0.7V_{DD}$ (Note 11)	$20 + 0.1C_B$		300	ns
Setup Time for STOP (P) Condition	$t_{SU, STO}$		0.6			µs
Capacitive Load for Each Bus Line	C_B				400	pF
Pulse Width of Spike Suppressed	t_{SP}				50	ns
TIMING CHARACTERISTICS FOR HIGH-SPEED MODE (C_B = 400pF, Note 12)						
Serial Clock Frequency	f_{SCLH}	(Note 13)			1.7	MHz
Hold Time, Repeated START Condition (Sr)	$t_{HD, STA}$		160			ns
Low Period of the SCL Clock	t_{LOW}		320			ns
High Period of the SCL Clock	t_{HIGH}		120			ns
Setup Time for a Repeated START Condition (Sr)	$t_{SU, STA}$		160			ns
Data Hold Time	$t_{HD, DAT}$	(Note 10)	0		150	ns
Data Setup Time	$t_{SU, DAT}$		10			ns

TIMING CHARACTERISTICS (Figure 1) (continued)

(V_{DD} = 2.7V to 3.6V (MAX1137/MAX1139), V_{DD} = 4.5V to 5.5V (MAX1136/MAX1138), V_{REF} = 2.048V (MAX1137/MAX1139), V_{REF} = 4.096V (MAX1136/MAX1138), f_{SCL} = 1.7MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. See Tables 1–5 for programming notation.).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Rise Time of SCL Signal (Current Source Enabled)	t_{RCL}	Measured from $0.3V_{DD}$ to $0.7V_{DD}$	20		80	ns
Rise Time of SCL Signal after Acknowledge Bit	t_{RCL1}	Measured from $0.3V_{DD}$ to $0.7V_{DD}$	20		160	ns
Fall Time of SCL Signal	t_{FCL}	Measured from $0.3V_{DD}$ to $0.7V_{DD}$	20		80	ns
Rise Time of SDA Signal	t_{RDA}	Measured from $0.3V_{DD}$ to $0.7V_{DD}$	20		160	ns
Fall Time of SDA Signal	t_{FDA}	Measured from $0.3V_{DD}$ to $0.7V_{DD}$ (Note 11)	20		160	ns
Setup Time for STOP (P) Condition	$t_{SU, STO}$		160			ns
Capacitive Load for Each Bus Line	C_B				400	pF
Pulse Width of Spike Suppressed	t_{SP}	(Notes 10 and 13)	0		10	ns

Note 1: For DC accuracy, the MAX1136/MAX1138 are tested at V_{DD} = 5V and the MAX1137/MAX1139 are tested at V_{DD} = 3V. All devices are configured for unipolar, single-ended inputs.

Note 2: Relative accuracy is the deviation of the analog value at any code from its theoretical value after the full-scale range and offsets have been calibrated.

Note 3: Offset nulled.

Note 4: Conversion time is defined as the number of clock cycles needed for conversion multiplied by the clock period. Conversion time does not include acquisition time. SCL is the conversion clock in the external clock mode.

Note 5: A filter on the SDA and SCL inputs suppresses noise spikes and delays the sampling instant.

Note 6: The absolute input-voltage range for the analog inputs (AIN0–AIN11) is from GND to V_{DD}.

Note 7: When the internal reference is configured to be available at AIN_/REF (SEL[2:1] = 11) decouple AIN_/REF to GND with a 0.1µF capacitor and a 2kΩ series resistor (see the *Typical Operating Circuit*).

Note 8: ADC performance is limited by the converter's noise floor, typically $300\mu V_{P-P}$.

Note 9: Measured as for the MAX1137/MAX1139

$$\frac{\left[\left[V_{FS}(3.6V) - V_{FS}(2.7V)\right] \times \frac{2^N - 1}{V_{REF}}\right]}{(3.6V - 2.7V)}$$

and for the MAX1136/MAX1138

$$\frac{\left[\left[V_{FS}(5.5V) - V_{FS}(4.5V)\right] \times \frac{2^N - 1}{V_{REF}}\right]}{(5.5V - 4.5V)}$$

Note 10: A master device must provide a data hold time for SDA (referred to V_{IL} of SCL) in order to bridge the undefined region of SCL's falling edge (see Figure 1).

Note 11: The minimum value is specified at +25°C.

Note 12: C_B = total capacitance of one bus line in pF.

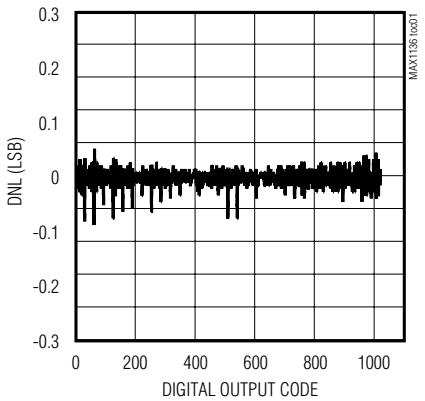
Note 13: f_{SCL} must meet the minimum clock low time plus the rise/fall times.

2.7V to 3.6V and 4.5V to 5.5V, Low-Power, 4-/12-Channel, 2-Wire Serial 10-Bit ADCs

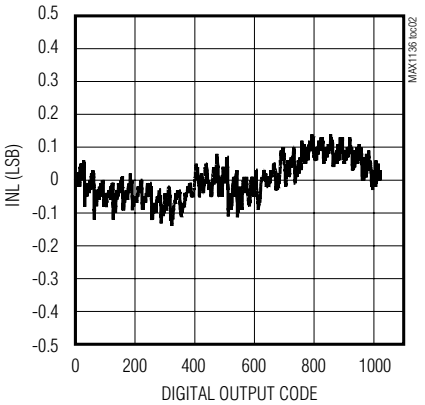
Typical Operating Characteristics

(V_{DD} = 3.3V (MAX1137/MAX1139), V_{DD} = 5V (MAX1136/MAX1138), f_{SCL} = 1.7MHz, external clock, f_{SAMPLE} = 94.4ksps, single-ended, unipolar, T_A = +25°C, unless otherwise noted.)

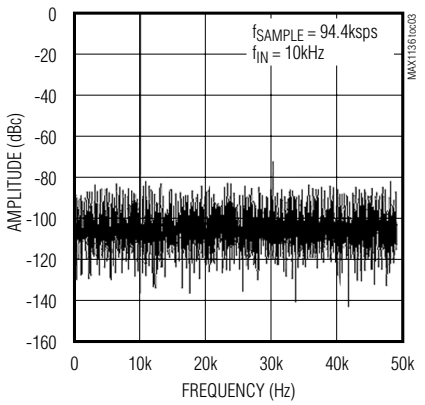
DIFFERENTIAL NONLINEARITY vs. DIGITAL CODE



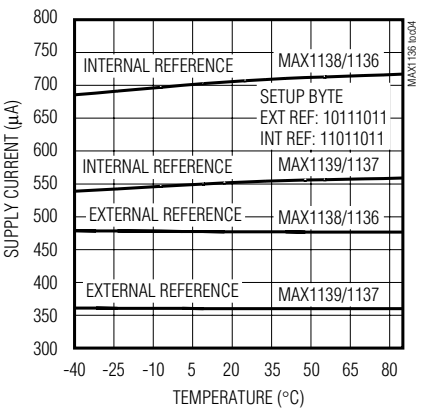
INTEGRAL NONLINEARITY vs. DIGITAL CODE



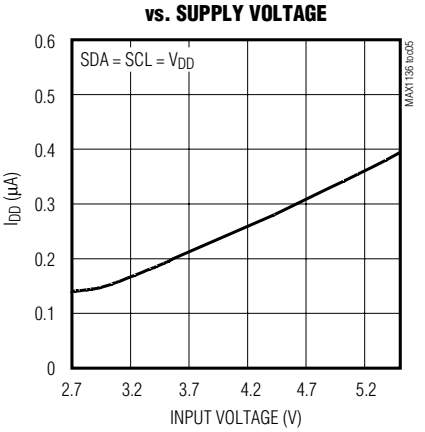
FFT PLOT



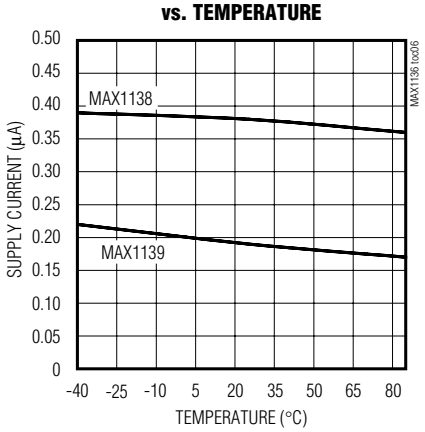
SUPPLY CURRENT vs. TEMPERATURE



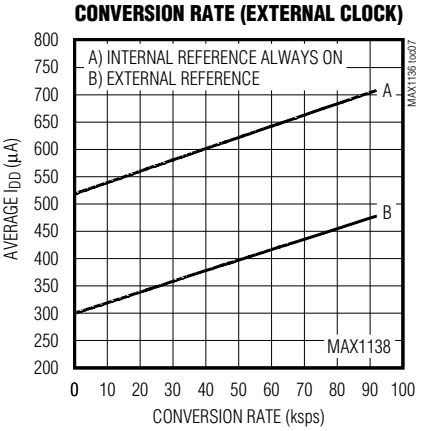
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



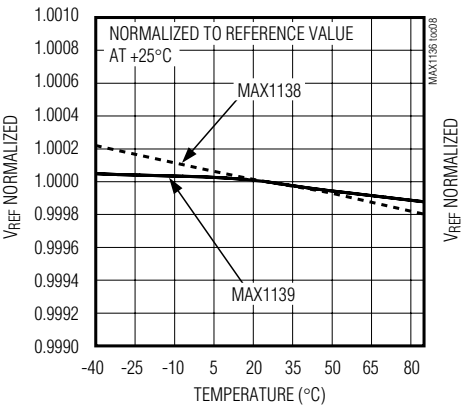
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



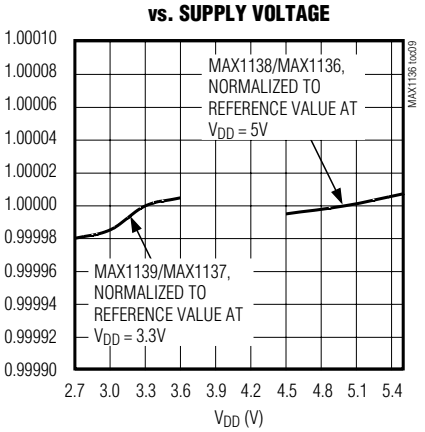
AVERAGE SUPPLY CURRENT vs. CONVERSION RATE (EXTERNAL CLOCK)



INTERNAL REFERENCE VOLTAGE vs. TEMPERATURE



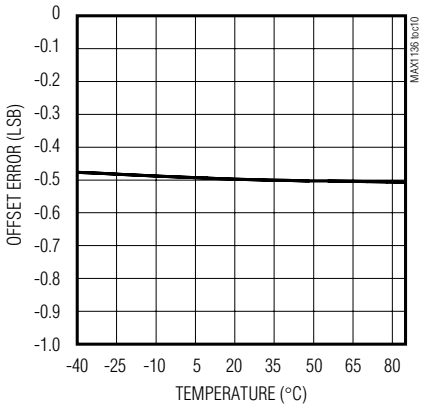
NORMALIZED REFERENCE VOLTAGE vs. SUPPLY VOLTAGE



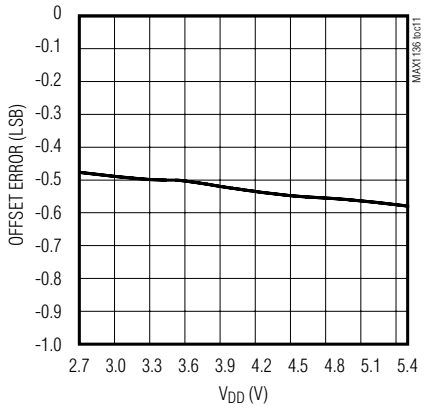
Typical Operating Characteristics (continued)

(V_{DD} = 3.3V (MAX1137/MAX1139), V_{DD} = 5V (MAX1136/MAX1138), f_{SCL} = 1.7MHz, external clock, f_{SAMPLE} = 94.4ksps, single-ended, unipolar, T_A = +25°C, unless otherwise noted.)

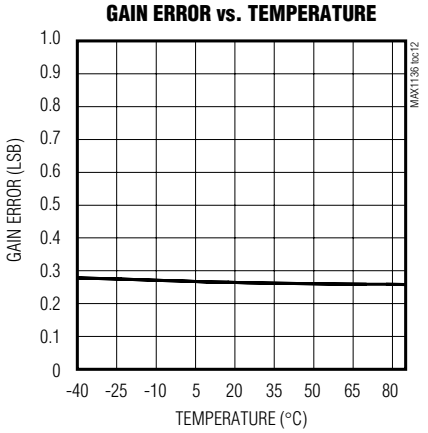
OFFSET ERROR vs. TEMPERATURE



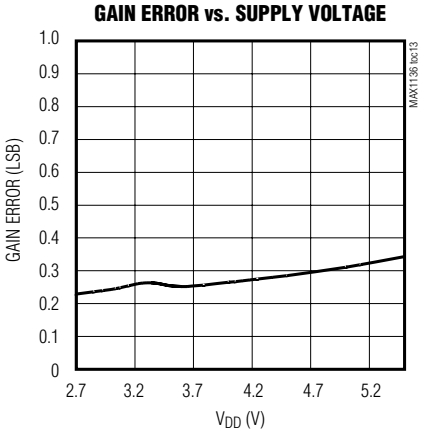
OFFSET ERROR vs. SUPPLY VOLTAGE



GAIN ERROR vs. TEMPERATURE



GAIN ERROR vs. SUPPLY VOLTAGE



2.7V to 3.6V and 4.5V to 5.5V, Low-Power, 4-/12-Channel, 2-Wire Serial 10-Bit ADCs

Pin Description

PIN		NAME	FUNCTION
MAX1136 MAX1137	MAX1138 MAX1139		
1, 2, 3	1, 2, 3	AIN0–AIN2	Analog Inputs
—	4–8	AIN3–AIN7	
—	16, 15, 14	AIN8–AIN10	
4	—	AIN3/REF	Analog Input 3/Reference Input or Output. Selected in the Setup Register. (See Tables 1 and 6.)
—	13	AIN11/REF	Analog Input 11/Reference Input or Output. Selected in the Setup Register. (See Tables 1 and 6.)
5	9	SCL	Clock Input
6	10	SDA	Data Input/Output
7	11	GND	Ground
8	12	V_{DD}	Positive Supply. Bypass to GND with a 0.1µF capacitor.

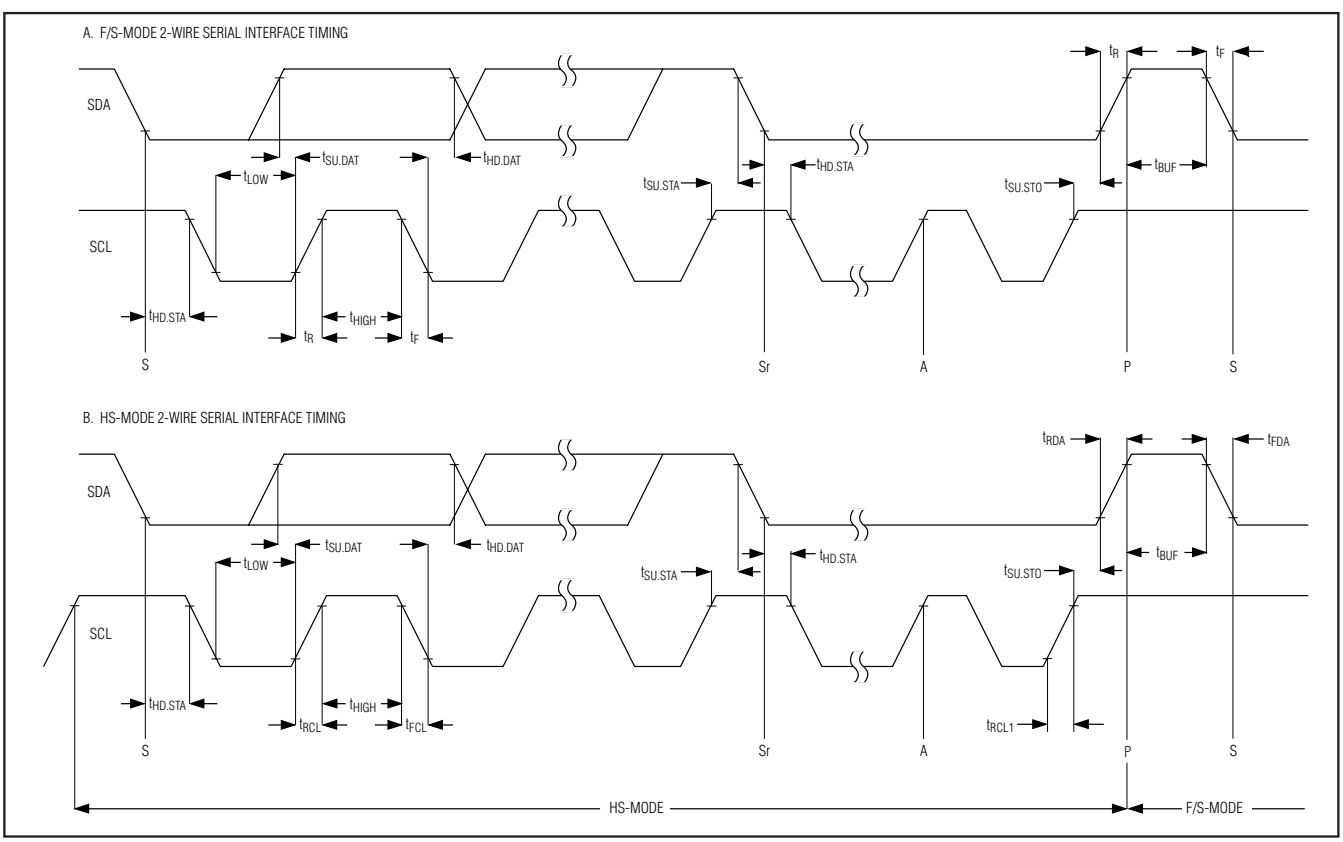


Figure 1. 2-Wire Serial Interface Timing

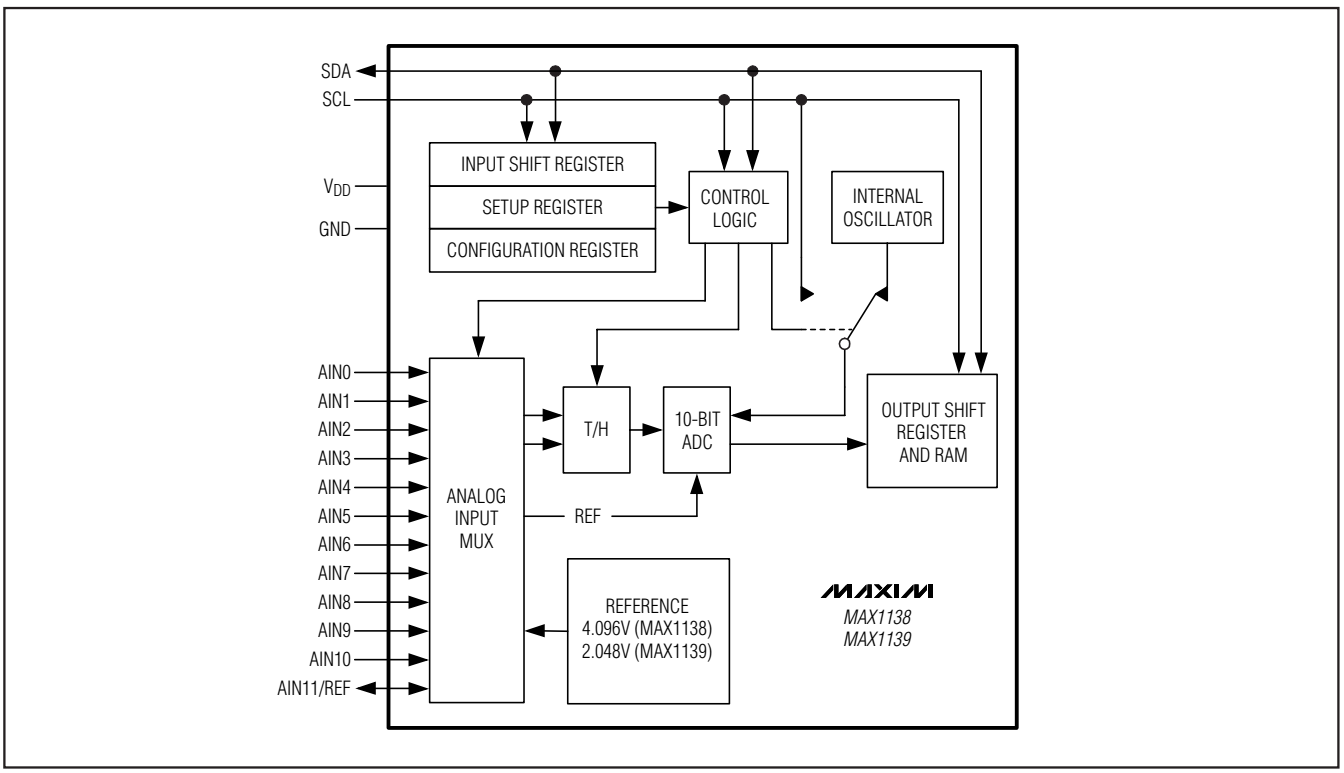


Figure 2. MAX1138/MAX1139 Functional Diagram

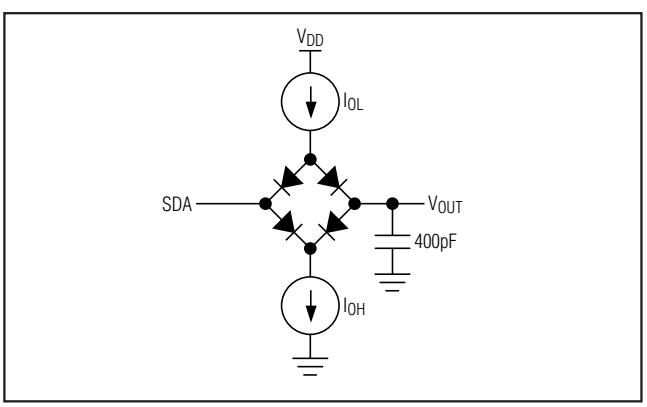


Figure 3. Load Circuit

Detailed Description

The MAX1136–MAX1139 analog-to-digital converters (ADCs) use successive-approximation conversion techniques and fully differential input track/hold (T/H) circuitry to capture and convert an analog signal to a serial 12-bit digital output. The MAX1136/MAX1137 are 4-channel ADCs, and the MAX1138/MAX1139 are 12-channel ADCs. These devices feature a high-speed 2-wire serial interface supporting data rates up to 1.7MHz. Figure 2 shows the simplified internal structure for the MAX1138/MAX1139.

Power Supply

The MAX1136–MAX1139 operates from a single supply and consumes 670µA (typ) at sampling rates up to 94.4ksps. The MAX1137/MAX1139 feature a 2.048V internal reference and the MAX1136/MAX1138 feature a 4.096V internal reference. All devices can be configured for use with an external reference from 1V to V_{DD}.

Analog Input and Track/Hold

The MAX1136–MAX1139 analog-input architecture contains an analog-input multiplexer (mux), a fully differential track-and-hold (T/H) capacitor, T/H switches, a comparator, and a fully differential switched capacitive digital-to-analog converter (DAC) (Figure 4).

In single-ended mode the analog-input multiplexer connects $C_{T/H}$ between the analog input selected by CS[3:0] (see the *Configuration/Setup Bytes* section) and GND (Table 3). In differential mode, the analog-input multiplexer connects $C_{T/H}$ to the "+" and "-" analog inputs selected by CS[3:0] (Table 4).

During the acquisition interval the T/H switches are in the track position and $C_{T/H}$ charges to the analog input

2.7V to 3.6V and 4.5V to 5.5V, Low-Power, 4-/12-Channel, 2-Wire Serial 10-Bit ADCs

signal. At the end of the acquisition interval, the T/H switches move to the hold position retaining the charge on $C_{T/H}$ as a stable sample of the input signal.

During the conversion interval, the switched capacitive DAC adjusts to restore the comparator input voltage to 0V within the limits of 10-bit resolution. This action requires 10 conversion clock cycles and is equivalent to transferring a charge of 11pF × (V_{IN+} - V_{IN-}) from $C_{T/H}$ to the binary weighted capacitive DAC, forming a digital representation of the analog input signal.

Sufficiently low source impedance is required to ensure an accurate sample. A source impedance of up to 1.5kΩ does not significantly degrade sampling accuracy. To minimize sampling errors with higher source impedances, connect a 100pF capacitor from the analog input to GND. This input capacitor forms an RC filter with the source impedance limiting the analog-input bandwidth. For larger source impedances, use a buffer amplifier to maintain analog-input signal integrity and bandwidth.

When operating in internal clock mode, the T/H circuitry enters its tracking mode on the eighth rising clock edge of the address byte (see the *Slave Address* section). The T/H circuitry enters hold mode on the falling clock edge of the acknowledge bit of the address byte (the ninth clock pulse). A conversion, or series of conversions, are then internally clocked and the MAX1136–MAX1139 holds SCL low. With external clock mode, the T/H circuitry enters track mode after a valid address on the rising edge of the clock during the read (R/$\overline{W}$ = 1) bit. Hold mode is then entered on the rising edge of the second clock pulse during the shifting out of the first byte of the result. The conversion is performed during the next 10 clock cycles.

The time required for the T/H circuitry to acquire an input signal is a function of the input sample capacitance. If the analog-input source impedance is high, the acquisition time constant lengthens and more time must be allowed between conversions. The acquisition time (t_{ACQ}) is the minimum time needed for the signal to be acquired. It is calculated by:

$$t_{ACQ} \geq 9 \times (R_{SOURCE} + R_{IN}) \times C_{IN}$$

where R_{SOURCE} is the analog-input source impedance, R_{IN} = 2.5kΩ, and C_{IN} = 22pF. t_{ACQ} is 1.5/f_{SCL} for internal clock mode and t_{ACQ} = 2/f_{SCL} for external clock mode.

Analog Input Bandwidth

The MAX1136–MAX1139 feature input-tracking circuitry with a 5MHz small-signal bandwidth. The 5MHz input bandwidth makes it possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using under sampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended.

Analog Input Range and Protection

Internal protection diodes clamp the analog input to V_{DD} and GND. These diodes allow the analog inputs to

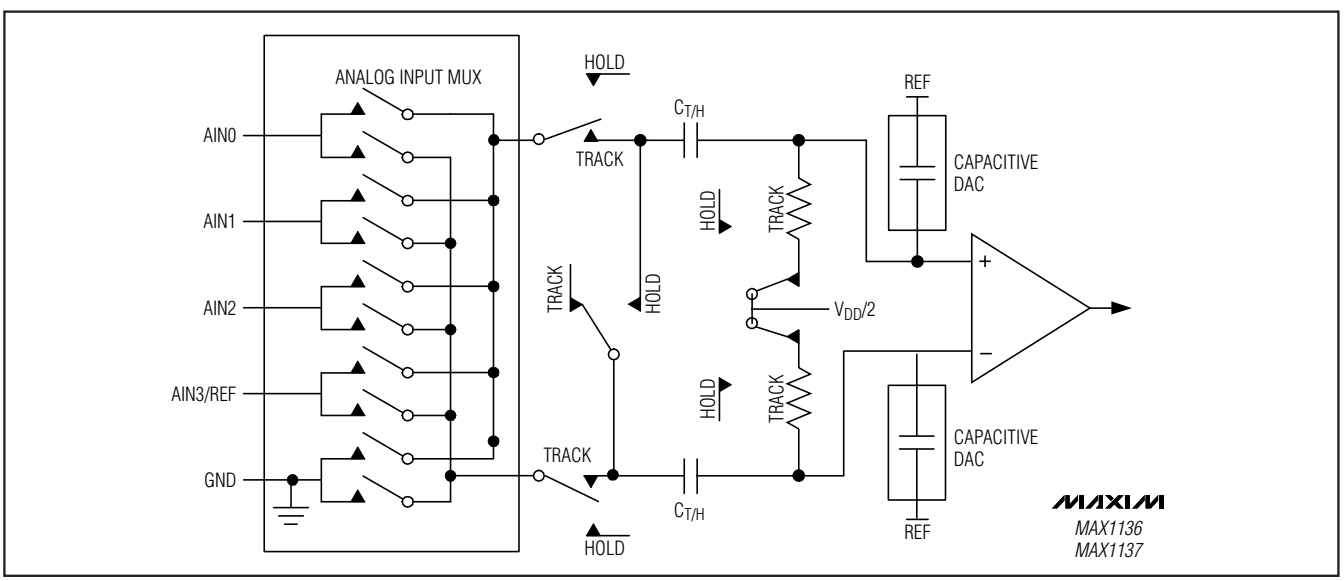


Figure 4. Equivalent Input Circuit

swing from (GND - 0.3V) to (V_{DD} + 0.3V) without causing damage to the device. For accurate conversions the inputs must not go more than 50mV below GND or above V_{DD}.

Single-Ended/Differential Input

The SGL/$\overline{DIF}$ of the configuration byte configures the MAX1136–MAX1139 analog-input circuitry for single-ended or differential inputs (Table 2). In single-ended mode (SGL/$\overline{DIF}$ = 1), the digital conversion results are the difference between the analog input selected by CS[3:0] and GND (Table 3). In differential mode (SGL/ $\overline{DIF}$ = 0) the digital conversion results are the difference between the "+" and the "-" analog inputs selected by CS[3:0] (Table 4).

Unipolar/Bipolar

When operating in differential mode, the BIP/$\overline{UNI}$ bit of the setup byte (Table 1) selects unipolar or bipolar operation. Unipolar mode sets the differential input range from 0 to V_{REF}. A negative differential analog input in unipolar mode will cause the digital output code to be zero. Selecting bipolar mode sets the differential input range to ±V_{REF}/2. The digital output code is binary in unipolar mode and two's complement in bipolar mode, see the *Transfer Functions* section.

In single-ended mode the MAX1136–MAX1139 will always operate in unipolar mode irrespective of BIP/$\overline{UNI}$. The analog inputs are internally referenced to GND with a full-scale input range from 0 to V_{REF}.

2-Wire Digital Interface

The MAX1136–MAX1139 feature a 2-wire interface consisting of a serial data line (SDA) and serial clock line (SCL). SDA and SCL facilitate bidirectional communication between the MAX1136–MAX1139 and the master at rates up to 1.7MHz. The MAX1136–MAX1139 are slaves that transfer and receive data. The master (typically a microcontroller) initiates data transfer on the bus and generates the SCL signal to permit that transfer.

SDA and SCL must be pulled high. This is typically done with pullup resistors (750Ω or greater) (see the *Typical Operating Circuit*). Series resistors (R_S) are optional. They protect the input architecture of the MAX1136–MAX1139 from high voltage spikes on the bus lines, minimize crosstalk, and undershoot of the bus signals.

Bit Transfer

One data bit is transferred during each SCL clock cycle. A minimum of eighteen clock cycles are required to transfer the data in or out of the MAX1136–MAX1139. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is stable are considered control signals (see the *START and STOP Conditions* section). Both SDA and SCL remain high when the bus is not busy.

START and STOP Conditions

The master initiates a transmission with a START condition (S), a high-to-low transition on SDA while SCL is high. The master terminates a transmission with a STOP condition (P), a low-to-high transition on SDA while SCL is high (Figure 5). A repeated START condition (Sr) can be used in place of a STOP condition to leave the bus active and the mode unchanged (see HS-mode).

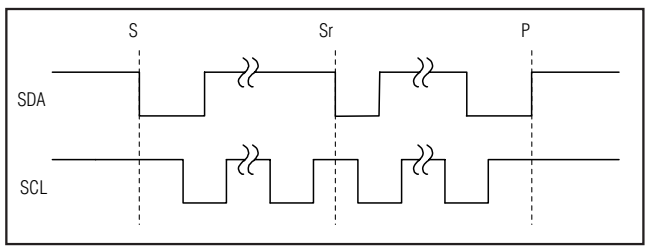


Figure 5. START and STOP Conditions

Acknowledge Bits

Data transfers are acknowledged with an acknowledge bit (A) or a not-acknowledge bit ($\overline{A}$). Both the master and the MAX1136–MAX1139 (slave) generate acknowledge bits. To generate an acknowledge, the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse (Figure 6). To generate a not-acknowledge, the receiver allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse and leaves SDA high during the high period of the clock pulse. Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer happens if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer the bus master should reattempt communication at a later time.

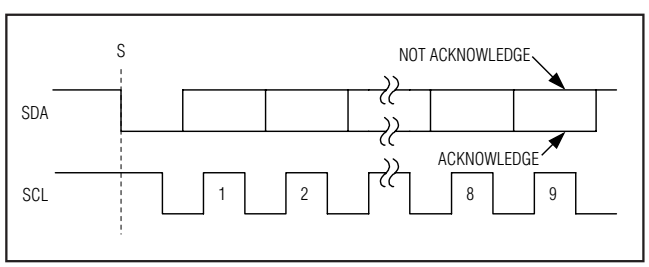


Figure 6. Acknowledge Bits

2.7V to 3.6V and 4.5V to 5.5V, Low-Power, 4-/12-Channel, 2-Wire Serial 10-Bit ADCs

DEVICE	SLAVE ADDRESS
MAX1136/MAX1137	0110100
MAX1138/MAX1139	0110101

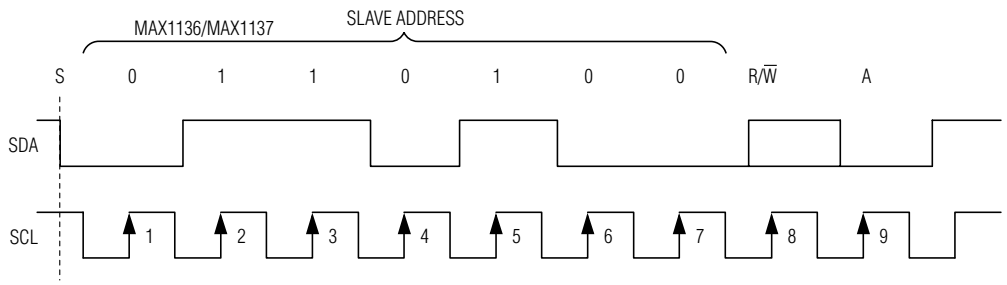


Figure 7. MAX1136/MAX1137 Slave Address Byte

Slave Address

A bus master initiates communication with a slave device by issuing a START condition followed by a slave address. When idle, the MAX1136–MAX1139 continuously wait for a START condition followed by their slave address. When the MAX1136–MAX1139 recognize their slave address, they are ready to accept or send data. The slave address has been factory programmed and is always 0110100 for the MAX1136/MAX1137, and 0110101 for MAX1138/MAX1139 (Figure 7). The least significant bit (LSB) of the address byte (R/$\overline{W}$) determines whether the master is writing to or reading from the MAX1136–MAX1139 (R/$\overline{W}$ = 0 selects a write condition, R/$\overline{W}$ = 1 selects a read condition). After receiving the address, the MAX1136–MAX1139 (slave) issues an acknowledge by pulling SDA low for one clock cycle.

Bus Timing

At power-up, the MAX1136–MAX1139 bus timing is set for fast mode (F/S-mode) which allows conversion rates up to 22.2ksps. The MAX1136–MAX1139 must operate in high-speed mode (HS-mode) to achieve conversion rates up to 94.4ksps. Figure 1 shows the bus timing for the MAX1136–MAX1139's 2-wire interface.

HS-Mode

At power-up, the MAX1136–MAX1139 bus timing is set for F/S-mode. The bus master selects HS-mode by addressing all devices on the bus with the HS-mode master code 0000 1XXX (X = don't care). After successfully receiving the HS-mode master code, the MAX1136–MAX1139 issue a not-acknowledge allowing SDA to be pulled high for one clock cycle (Figure 8). After the not-acknowledge, the MAX1136–MAX1139 are in HS-mode. The bus master must then send a repeated START followed by a slave address to initiate HS-mode communication. If the master generates a STOP condition the MAX1136–MAX1139 returns to F/S-mode.

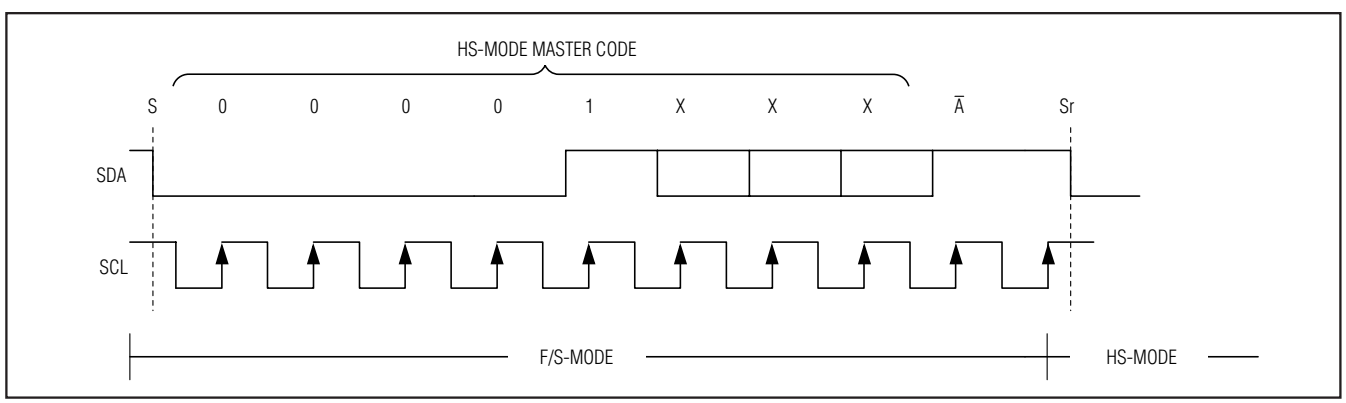


Figure 8. F/S-Mode to HS-Mode Transfer

Configuration/Setup Bytes (Write Cycle)

A write cycle begins with the bus master issuing a START condition followed by seven address bits (Figure 7) and a write bit (R/$\overline{W}$ = 0). If the address byte is successfully received, the MAX1136–MAX1139 (slave) issues an acknowledge. The master then writes to the slave. The slave recognizes the received byte as the setup byte (Table 1) if the most significant bit (MSB) is 1. If the MSB is 0, the slave recognizes that byte as the configuration byte (Table 2). The master can write either one or two bytes to the slave in any order (setup byte then configuration byte; configuration byte then setup byte; setup byte or configuration byte only; Figure 9). If the slave receives a byte successfully, it issues an acknowledge. The master ends the write cycle by issuing a STOP condition or a repeated START condition. When operating in HS-mode, a STOP condition returns the bus into F/S-mode (see the *HS-Mode* section).

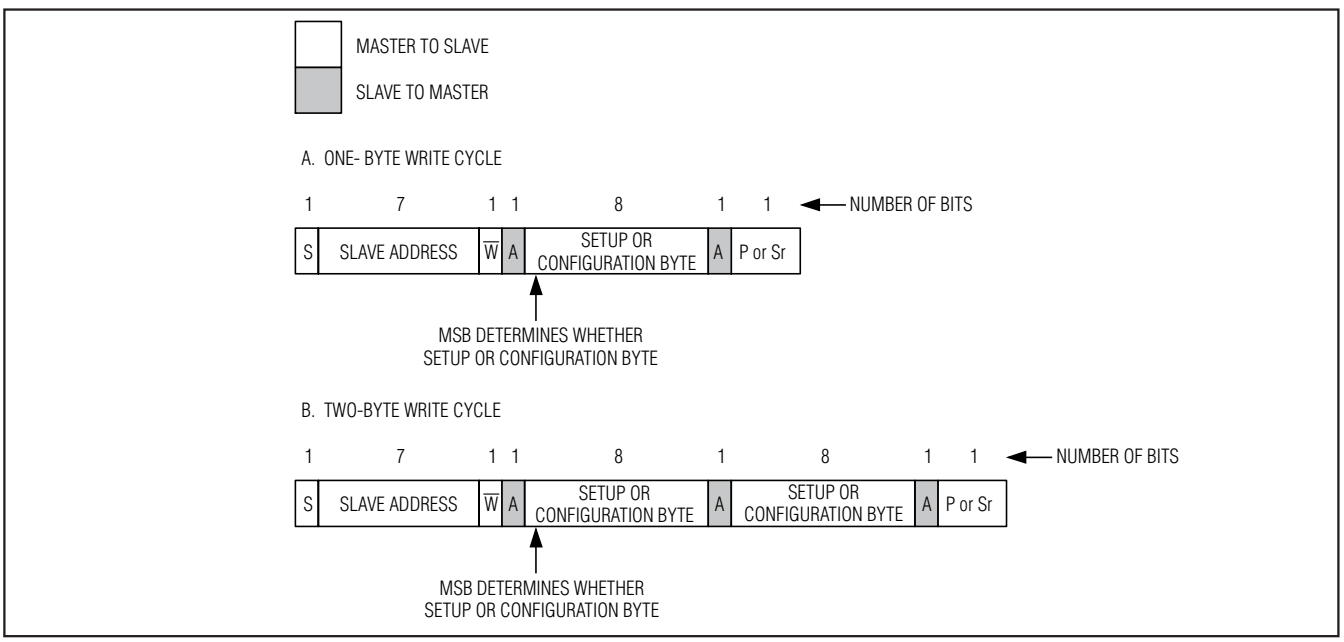


Figure 9. Write Cycle

Table 1. Setup Byte Format

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
REG	SEL2	SEL1	SEL0	CLK	BIP/$\overline{UNI}$	$\overline{RST}$	X

BIT	NAME	DESCRIPTION
7	REG	Register bit. 1 = setup byte, 0 = configuration byte (see Table 2).
6	SEL2	Three bits select the reference voltage and the state of AIN_/REF (Table 6). Defaulted to 000 at power-up.
5	SEL1	
4	SEL0	
3	CLK	1 = external clock, 0 = internal clock. Defaulted to 0 at power-up.
2	BIP/$\overline{UNI}$	1 = bipolar, 0 = unipolar. Defaulted to 0 at power-up.
1	$\overline{RST}$	1 = no action, 0 = resets the configuration register to default. Setup register remains unchanged.
0	X	Don't care, can be set to 1 or 0.

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Table 2. Configuration Byte Format

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
REG	SCAN1	SCAN0	CS3	CS2	CS1	CS0	SGL/$\overline{DIF}$

BIT	NAME	DESCRIPTION
7	REG	Register bit 1= setup byte (see Table 1), 0 = configuration byte
6	SCAN1	Scan select bits. Two bits select the scanning configuration (Table 5). Defaulted to 00 at power-up.
5	SCAN0	
4	CS3	Channel select bits. Four bits select which analog input channels are to be used for conversion (Tables 3 and 4). Defaulted to 0000 at power-up. For MAX1136/MAX1137, CS3 and CS2 are internally set to 0.
3	CS2	
2	CS1	
1	CS0	
0	SGL/$\overline{DIF}$	1 = single-ended, 0 = differential (Tables 3 and 4). Defaulted to 1 at power-up. See the *Single-Ended/Differential Input* section.

Table 3. Channel Selection in Single-Ended Mode (SGL/$\overline{DIF}$ = 1)

CS3[1]	CS2[1]	CS1	CS0	AIN0	AIN1	AIN2	AIN3[2]	AIN4	AIN5	AIN6	AIN7	AIN8	AIN9	AIN10	AIN11[2]	GND
0	0	0	0	+												-
0	0	0	1		+											-
0	0	1	0			+										-
0	0	1	1				+									-
0	1	0	0					+								-
0	1	0	1						+							-
0	1	1	0							+						-
0	1	1	1								+					-
1	0	0	0									+				-
1	0	0	1										+			-
1	0	1	0											+		-
1	0	1	1												+	-
1	1	0	0	RESERVED												
1	1	0	1	RESERVED												
1	1	1	0	RESERVED												
1	1	1	1	RESERVED												

1. For MAX1136/MAX1137, CS3 and CS2 are internally set to 0.

2. When SEL1 = 1, a single-ended read of AIN3/REF (MAX1136/MAX1137) or AIN11/REF (MAX1138/MAX1139) will be ignored; scan will stop at AIN2 or AIN10.

Table 4. Channel Selection in Differential Mode (SGL/$\overline{DIF}$ = 0)

CS3[1]	CS2[1]	CS1	CS0	AIN0	AIN1	AIN2	AIN3[2]	AIN4	AIN5	AIN6	AIN7	AIN8	AIN9	AIN10	AIN11[2]
0	0	0	0	+	-										
0	0	0	1	-	+										
0	0	1	0			+	-								
0	0	1	1			-	+								
0	1	0	0					+	-						
0	1	0	1					-	+						
0	1	1	0							+	-				
0	1	1	1							-	+				
1	0	0	0									+	-		
1	0	0	1									-	+		
1	0	1	0											+	-
1	0	1	1											-	+
1	1	0	0	RESERVED											
1	1	0	1	RESERVED											
1	1	1	0	RESERVED											
1	1	1	1	RESERVED											

1. For MAX1136/MAX1137, CS3 and CS2 are internally set to 0.

2. When SEL1 = 1, a differential read between AIN2 and AIN3/REF (MAX1136/MAX1137) or AIN10 and AIN11/REF (MAX1138/MAX1139) will return the difference between GND and AIN2 or AIN10, respectively. For example, a differential read of 1011 will return the negative difference between AIN10 and GND. In differential scanning, the address increments by 2 until limit set by CS3:CS1 has been reached.

Data Byte (Read Cycle)

A read cycle must be initiated to obtain conversion results. Read cycles begin with the bus master issuing a START condition followed by seven address bits and a read bit (R/$\overline{W}$ = 1). If the address byte is successfully received, the MAX1136–MAX1139 (slave) issues an acknowledge. The master then reads from the slave. The result is transmitted in two bytes; first six bits of the first byte are high, then MSB through LSB are consecutively clocked out. After the master has received the byte(s) it can issue an acknowledge if it wants to continue reading or a not-acknowledge if it no longer wishes to read. If the MAX1136–MAX1139 receive a not-acknowledge, they release SDA allowing the master to generate a STOP or a repeated START condition. See the *Clock Mode* and *Scan Mode* sections for detailed information on how data is obtained and converted.

Clock Modes

The clock mode determines the conversion clock and the data acquisition and conversion time. The clock mode also affects the scan mode. The state of the set-up byte's CLK bit determines the clock mode (Table 1).

At power-up the MAX1136–MAX1139 are defaulted to internal clock mode (CLK = 0).

Internal Clock

When configured for internal clock mode (CLK = 0), the MAX1136–MAX1139 use their internal oscillator as the conversion clock. In internal clock mode, the MAX1136–MAX1139 begin tracking the analog input after a valid address on the eighth rising edge of the clock. On the falling edge of the ninth clock the analog signal is acquired and the conversion begins. While converting the analog input signal, the MAX1136–MAX1139 holds SCL low (clock stretching). After the conversion completes, the results are stored in internal memory. If the scan mode is set for multiple conversions, they will all happen in succession with each additional result stored in memory.The MAX1136/MAX1137 contain four 10-bit blocks of memory, and the MAX1138/MAX1139 contain twelve 10-bit blocks of memory. Once all conversions are complete, the MAX1136–MAX1139 release SCL allowing it to be pulled high. The master may now clock the results out of the memory in the same order the scan conversion has been done at a clock rate of up to 1.7MHz. SCL will be stretched for a maximum of 7.6µs per channel (see Figure 10).

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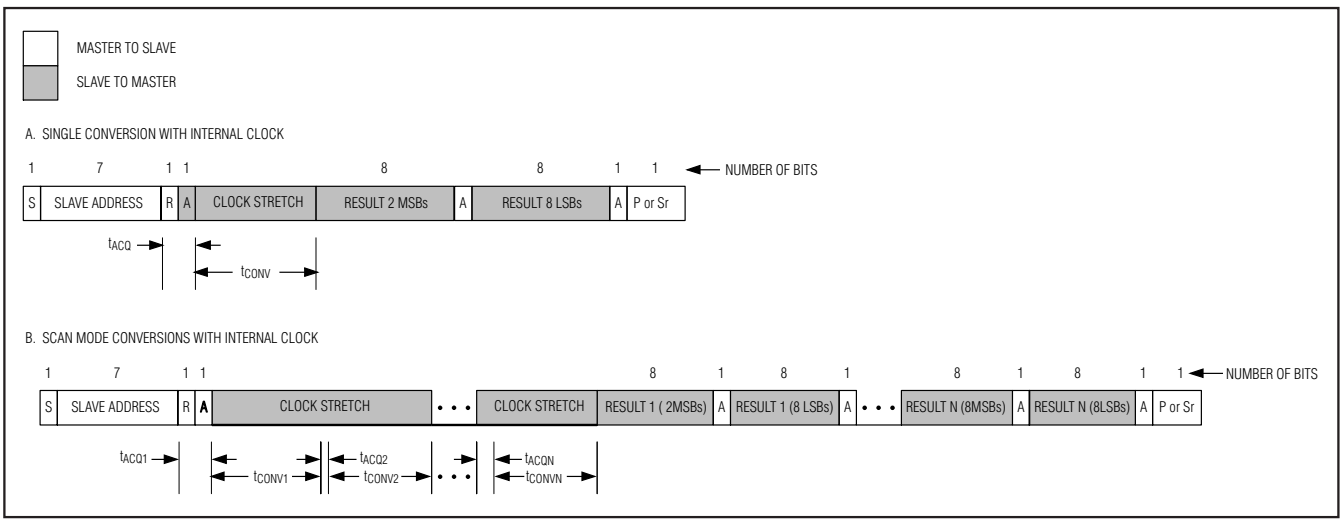

Figure 10. Internal Clock Mode Read Cycles

The device memory contains all of the conversion results when the MAX1136–MAX1139 release SCL. The converted results are read back in a first-in-first-out (FIFO) sequence. If AIN_/REF is set to be a reference input or output (SEL1 = 1, Table 6), AIN_/REF will be excluded from a multichannel scan. The memory contents can be read continuously. If reading continues past the result stored in memory, the pointer will wrap around and point to the first result. Note that only the current conversion results will be read from memory. The device must be addressed with a read command to obtain new conversion results.

The internal clock mode's clock stretching quiets the SCL bus signal reducing the system noise during conversion. Using the internal clock also frees the bus master (typically a microcontroller) from the burden of running the conversion clock, allowing it to perform other tasks that do not need to use the bus.

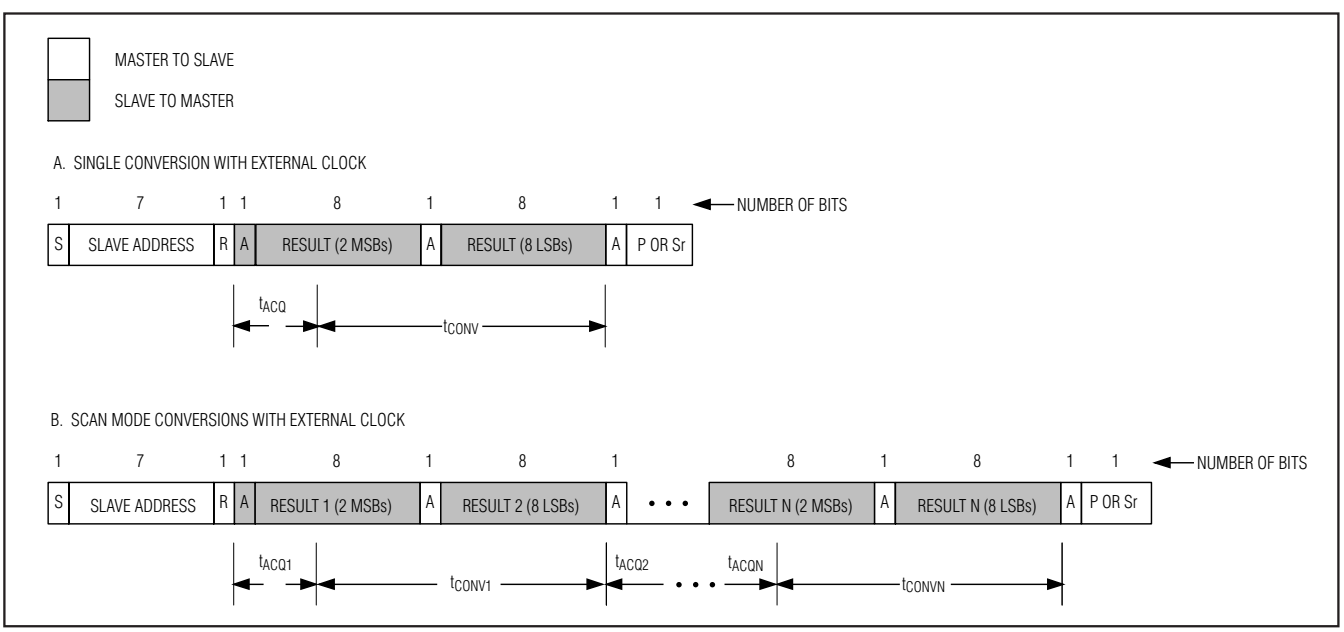

Figure 11. External Clock Mode Read Cycle

Table 5. Scanning Configuration

SCAN1	SCAN0	SCANNING CONFIGURATION
0	0	Scans up from AIN0 to the input selected by CS3–CS0. When CS3–CS0 exceeds 1011, the scanning will stop at AIN11. When AIN_/REF is set to be a reference input/output, scanning will stop at AIN2 and AIN10.
0	1	*Converts the input selected by CS3–CS0 eight times. (See Tables 3 and 4)
1	0	Scans up from AIN2 to the input selected by CS1 and CS0. When CS1 and CS0 are set for AIN0–AIN2, the only scan that takes place is AIN2 (MAX1136/MAX1137). When AIN/REF is set to be a reference input/output, scanning stops at AIN2.
		Scans up from AIN6 to the input selected by CS3–CS0. When CS3–CS0 is set for AIN0–AIN6, the only scan that takes place is AIN6 (MAX1138/MAX1139). When AIN/REF is set to be a reference input/output, scanning stops at selected channel or AIN10.
1	1	*Converts channel selected by CS3–CS0.

**When operating in external clock mode there is no difference between SCAN[1:0] = 01 and SCAN[1:0] = 11 and converting will occur perpetually until not acknowledge occurs.*

External Clock

When configured for external clock mode (CLK = 1), the MAX1136–MAX1139 use the SCL as the conversion clock. In external clock mode, the MAX1136–MAX1139 begin tracking the analog input on the ninth rising clock edge of a valid slave address byte. Two SCL clock cycles later the analog signal is acquired and the conversion begins. Unlike internal clock mode, converted data is available immediately after the first four empty high bits. The device will continuously convert input channels dictated by the scan mode until given a not acknowledge. There is no need to re-address the device with a read command to obtain new conversion results (see Figure 11).

The conversion must complete in 1ms or droop on the track-and-hold capacitor will degrade conversion results. Use internal clock mode if the SCL clock period exceeds 60µs.

The MAX1136–MAX1139 must operate in external clock mode for conversion rates from 40ksps to 94.4ksps. Below 40ksps internal clock mode is recommended due to much smaller power consumption.

Scan Mode

SCAN0 and SCAN1 of the configuration byte set the scan mode configuration. Table 5 shows the scanning configurations. If AIN_/REF is set to be a reference input or output (SEL1 = 1, Table 6), AIN_/REF will be excluded from a multichannel scan. The scanned results are written to memory in the same order as the conversion. Read the results from memory in the order they were converted. Each result needs a 2-byte transmission, the first byte begins with six empty bits during which SDA is left high. Each byte has to be acknowledged by the master or the memory transmission will be terminated. It is not possible to read the memory independently of conversion.

Applications Information

Power-On Reset

The configuration and setup registers (Tables 1 and 2) will default to a single-ended, unipolar, single-channel conversion on AIN0 using the internal clock with V_{DD} as the reference and AIN_/REF configured as an analog input. The memory contents are unknown after power-up.

Automatic Shutdown

Automatic shutdown occurs between conversions when the MAX1136–MAX1139 are idle. All analog circuits participate in automatic shutdown except the internal reference due to its prohibitively long wake-up time. When operating in external clock mode, a STOP, not-acknowledge or repeated START, condition must be issued to place the devices in idle mode and benefit from automatic shutdown. A STOP condition is not necessary in internal clock mode to benefit from automatic shutdown because power-down occurs once all conversion results are written to memory (Figure 10). When using an external reference or V_{DD} as a reference, all analog circuitry is inactive in shutdown and supply current is less than 0.5µA (typ). The digital conversion results obtained in internal clock mode are maintained in memory during shutdown and are available for access through the serial interface at any time prior to a STOP or a repeated START condition.

When idle the MAX1136–MAX1139 continuously wait for a START condition followed by their slave address (see *Slave Address* section). Upon reading a valid address byte the MAX1136–MAX1139 power-up. The internal reference requires 10ms to wake up, so when using the internal reference it should be powered up

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Table 6. Reference Voltage and AIN_/REF Format

SEL2	SEL1	SEL0	REFERENCE VOLTAGE	AIN_/REF	INTERNAL REFERENCE STATE
0	0	X	V_{DD}	Analog Input	Always Off
0	1	X	External Reference	Reference Input	Always Off
1	0	0	Internal Reference	Analog Input	Always Off
1	0	1	Internal Reference	Analog Input	Always On
1	1	0	Internal Reference	Reference Output	Always Off
1	1	1	Internal Reference	Reference Output	Always On

10ms prior to conversion or powered continuously. Wake-up is invisible when using an external reference or V_{DD} as the reference.

Automatic shutdown results in dramatic power savings, particularly at slow conversion rates and with internal clock. For example, at a conversion rate of 10ksps, the average supply current for the MAX1137 is 60µA (typ) and drops to 6µA (typ) at 1ksps. At 0.1ksps the average supply current is just 1µA, or a minuscule 3µW of power consumption, see Average Supply Current vs. Conversion Rate in the *Typical Operating Characteristics*.

Reference Voltage

SEL[2:0] of the setup byte (Table 1) control the reference and the AIN_/REF configuration (Table 6). When AIN_/REF is configured to be a reference input or reference output (SEL1 = 1), differential conversions on AIN_/REF appear as if AIN_/REF is connected to GND (see Note 2 and Table 4). Single-ended conversion in scan mode on AIN_/REF will be ignored by internal limiter, which sets the highest available channel at AIN2 or AIN10.

Internal Reference

The internal reference is 4.096V for the MAX1136/MAX1138 and 2.048V for the MAX1137/MAX1139. SEL1 of the setup byte controls whether AIN_/REF is used for an analog input or a reference (Table 6). When AIN_/REF is configured to be an internal reference output (SEL[2:1] = 11), decouple AIN_/REF to GND with a 0.1µF capacitor and a 2kΩ sereis resistor (see the *Typical Operating Circuit*). Once powered up, the reference always remains on until reconfigured. The internal reference requires 10ms to wake up and is accessed using SEL0 (Table 6). When in shutdown, the internal reference output is in a high-impedance state. The reference should not be used to supply current for external circuitry. The internal reference does not require an external bypass capacitor and works best when not connected to the pin (SEL1 = 0).

External Reference

The external reference can range from 1V to V_{DD}. For maximum conversion accuracy, the reference must be able to deliver up to 40µA and have an output impedance of 500Ω or less. If the reference has a higher output impedance or is noisy, bypass it to GND as close to AIN_/REF as possible with a 0.1µF capacitor.

Transfer Functions

Output data coding for the MAX1136–MAX1139 is binary in unipolar mode and two's complement in bipolar mode with 1 LSB = (V_{REF}/2N) where 'N' is the number of bits (10). Code transitions occur halfway between successive-integer LSB values. Figure 12 and Figure 13 show the input/output (I/O) transfer functions for unipolar and bipolar operations, respectively.

Layout, Grounding, and Bypassing

Only use PC boards. Wire-wrap configurations are not recommended since the layout should ensure proper separation of analog and digital traces. Do not run analog and digital lines parallel to each other, and do not layout digital signal paths underneath the ADC pack-

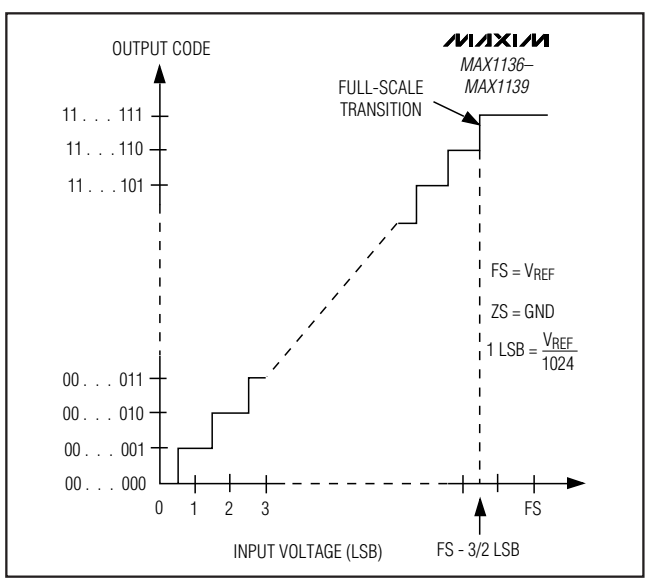

Figure 12. Unipolar Transfer Function

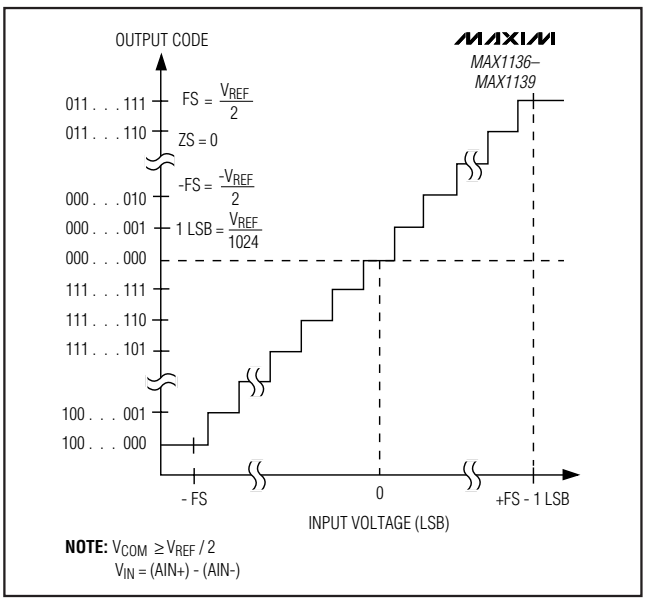

Figure 13. Bipolar Transfer Function

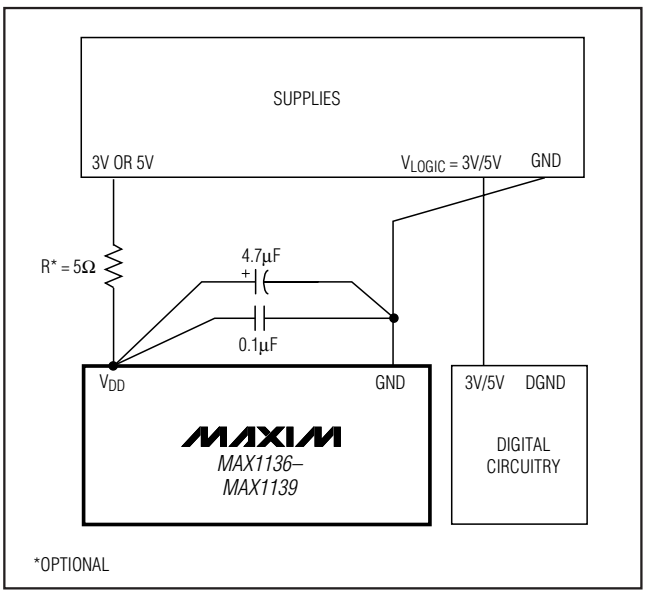

Figure 14. Power-Supply Grounding Connection

age. Use separate analog and digital PC board ground sections with only one star point (Figure 14) connecting the two ground systems (analog and digital). For lowest noise operation, ensure the ground return to the star ground's power supply is low impedance and as short as possible. Route digital signals far away from sensitive analog and reference inputs.

High-frequency noise in the power supply (V_{DD}) could influence the proper operation of the ADC's fast comparator. Bypass V_{DD} to the star ground with a network of two parallel capacitors, 0.1µF and 4.7µF, located as close as possible to the MAX1136–MAX1139 power-supply pin. Minimize capacitor lead length for best supply noise rejection, and add an attenuation resistor (5Ω) in series with the power supply, if it is extremely noisy.

Definitions

Integral Nonlinearity

Integral nonlinearity (INL) is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best straight-line fit or a line drawn between the endpoints of the transfer function, once offset and gain errors have been nullified. The MAX1136–MAX1139's INL is measured using the endpoint.

Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between an actual step width and the ideal value of 1 LSB. A DNL error specification of less than 1 LSB guarantees no missing codes and a monotonic transfer function.

Aperture Jitter

Aperture jitter (t_{AJ}) is the sample-to-sample variation in the time between the samples.

Aperture Delay

Aperture delay (t_{AD}) is the time between the falling edge of the sampling clock and the instant when an actual sample is taken.

Signal-to-Noise Ratio

For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization error only and results directly from the ADC's resolution (N Bits):

$$SNR_{MAX[dB]} = 6.02_{dB} \times N + 1.76_{dB}$$

In reality, there are other noise sources besides quantization noise: thermal noise, reference noise, clock jitter, etc. SNR is computed by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components minus the fundamental, the first five harmonics, and the DC offset.

Signal-to-Noise Plus Distortion

Signal-to-noise plus distortion (SINAD) is the ratio of the fundamental input frequency's RMS amplitude to RMS equivalent of all other ADC output signals.

$$SINAD\ (dB) = 20 \times \log\ (SignalRMS/NoiseRMS)$$

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Effective Number of Bits

Effective number of bits (ENOB) indicates the global accuracy of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. With an input range equal to the ADC's full-scale range, calculate the ENOB as follows:

$$SINAD(dB) = 20 \times \log\left[\frac{SignalRMS}{NoiseRMS + THDRMS}\right]$$

$$ENOB = (SINAD - 1.76)/6.02$$

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of the input signal's first five harmonics to the fundamental itself. This is expressed as:

$$THD = 20 \times \log\left(\sqrt{\left(\frac{V_2^2 + V_3^2 + V_4^2 + V_5^2}{V_1}\right)}\right)$$

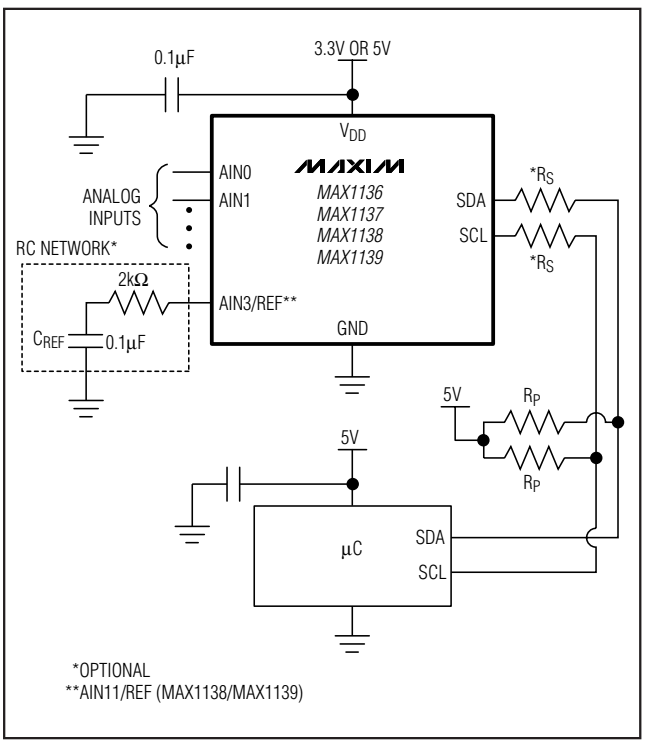
where V_1 is the fundamental amplitude, and V_2 through V_5 are the amplitudes of the 2nd through 5th order harmonics.

Spurious-Free Dynamic Range

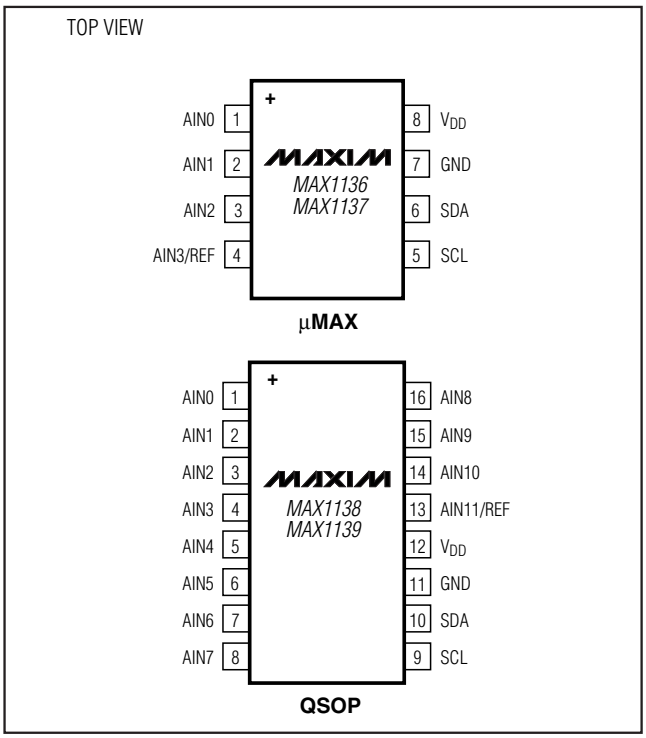
Spurious-free dynamic range (SFDR) is the ratio of RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next largest distortion component.

2.7V to 3.6V and 4.5V to 5.5V, Low-Power, 4-/12-Channel, 2-Wire Serial 10-Bit ADCs

Typical Operating Circuit



Pin Configurations



Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
8 µMAX	U8+1	21-0036
16 QSOP	E16+4	21-0055

2.7V to 3.6V and 4.5V to 5.5V, Low-Power, 4-/12-Channel, 2-Wire Serial 10-Bit ADCs

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
5	5/09	Discontinued some versions of the family	1–5, 13, 17–21
6	3/10	Changed *Absolute Maximum Ratings* and timing diagram	2, 12

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