Table 2. Thermal Characteristics

Characteristic	Symbol	Value (1,2)	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C, 60 W CW Case Temperature 80°C, 14 W CW	$R_{\theta JC}$	 0.77 0.88	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1A (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD 22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 68 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 200 μA)	$V_{GS(th)}$	1	2	3	Vdc
Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_D = 450 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	—	2.9	—	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 1.5 Adc)	$V_{DS(on)}$	—	0.18	0.4	Vdc
Dynamic Characteristics					
Output Capacitance (V_{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	33	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	1.4	—	pF
Input Capacitance (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc ± 30 mV(rms)ac @ 1 MHz)	C_{iss}	—	106	—	pF

Functional Tests (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 450 mA, P_{out} = 14 W Avg., f = 880 MHz, Single-Carrier N-CDMA, 1.2288 MHz Channel Bandwidth Carrier. ACPR measured in 30 kHz Channel Bandwidth @ ±750 kHz Offset. PAR = 9.8 dB @ 0.01% Probability on CCDF

Power Gain	G_{ps}	20.5	21.4	23.5	dB
Drain Efficiency	η_D	30.5	32.1	—	%
Adjacent Channel Power Ratio	ACPR	—	-47.6	-45	dBc
Input Return Loss	IRL	—	-15.3	-9	dB

1. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
2. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.

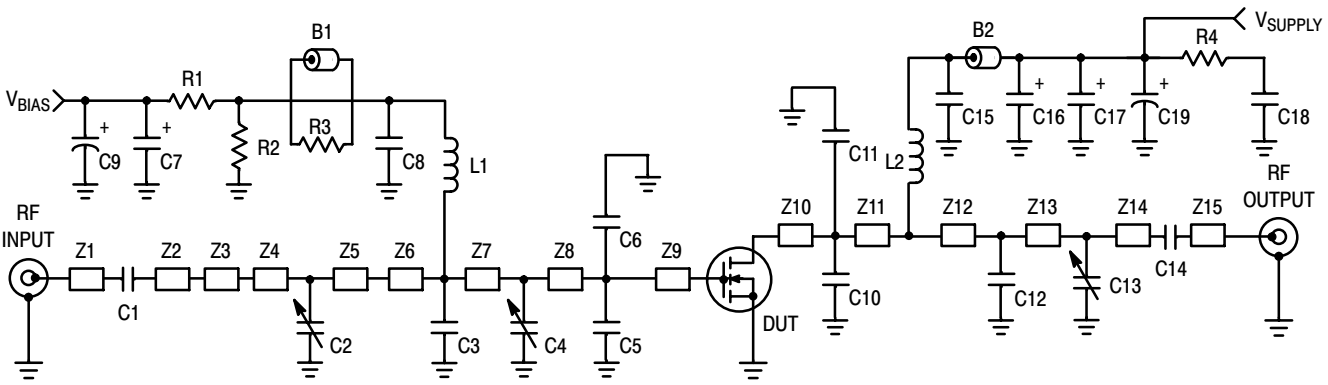
(continued)

ARCHIVE INFORMATION

Table 5. Electrical Characteristics (T_C = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Typical GSM EDGE Performances (In Freescale GSM EDGE Test Fixture Optimized for 921 - 960 MHz, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 500 mA, P_{out} = 21 W Avg., f = 921 - 960 MHz, GSM EDGE Signal					
Power Gain	G_{ps}	—	20	—	dB
Drain Efficiency	η_D	—	46	—	%
Error Vector Magnitude	EVM	—	1.5	—	%
Spectral Regrowth at 400 kHz Offset	SR1	—	-62	—	dBc
Spectral Regrowth at 600 kHz Offset	SR2	—	-78	—	dBc
Typical CW Performances (In Freescale GSM Test Fixture Optimized for 921 - 960 MHz, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 500 mA, P_{out} = 60 W, f = 921 - 960 MHz					
Power Gain	G_{ps}	—	20	—	dB
Drain Efficiency	η_D	—	63	—	%
Input Return Loss	IRL	—	-12	—	dB
P_{out} @ 1 dB Compression Point (f = 940 MHz)	P1dB	—	67	—	W

ARCHIVE INFORMATION



Z1	0.215″ x 0.065″ Microstrip	Z9	0.057″ x 0.525″ Microstrip
Z2	0.221″ x 0.065″ Microstrip	Z10	0.360″ x 0.270″ Microstrip
Z3	0.500″ x 0.100″ Microstrip	Z11	0.063″ x 0.270″ Microstrip
Z4	0.460″ x 0.270″ Microstrip	Z12	0.360″ x 0.065″ Microstrip
Z5	0.040″ x 0.270″ Microstrip	Z13	0.170″ x 0.065″ Microstrip
Z6	0.280″ x 0.270″ x 0.530″ Taper	Z14	0.880″ x 0.065″ Microstrip
Z7	0.087″ x 0.525″ Microstrip	Z15	0.260″ x 0.065″ Microstrip
Z8	0.435″ x 0.525″ Microstrip	PCB	Taconic RF-35 0.030″, ε_r = 3.5

Figure 1. MRF6S9060NR1(NBR1) Test Circuit Schematic

Table 6. MRF6S9060NR1(NBR1) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
B1	Ferrite Bead	2743019447	Fair-Rite
B2	Ferrite Bead	2743021447	Fair-Rite
C1, C8, C14, C15	47 pF Chip Capacitors	ATC100B470JT500XT	ATC
C2, C4, C13	0.8-8.0 pF Variable Capacitors, Gigatrim	27290	Johanson
C3	3.0 pF Chip Capacitor	ATC100B3R0JT500XT	ATC
C5, C6	15 pF Chip Capacitors	ATC100B150JT500XT	ATC
C7, C16, C17	10 μF, 35 V Tantalum Capacitors	T491D106K035AT	Kemet
C9	100 μF, 50 V Electrolytic Capacitor	MCHT101M1HB-1017-RH	Multicomp
C10, C11	13 pF Chip Capacitors	ATC100B130JT500XT	ATC
C12	3.9 pF Chip Capacitor	ATC100B3R9JT500XT	ATC
C18	0.56 μF Chip Capacitor	ATC700A561MT150XT	ATC
C19	470 μF, 63 V Electrolytic Capacitor	477KXM063M	Illinois Capacitor
L1, L2	12.5 nH Inductor	A04T-5	Coilcraft
R1	1 kΩ, 1/4 W Chip Resistor	CRCW12061001FKEA	Vishay
R2	560 kΩ, 1/4 W Chip Resistor	CRCW12065600FKEA	Vishay
R3	12 Ω, 1/4 W Chip Resistor	CRCW120612R0FKEA	Vishay
R4	27 Ω, 1/4 W Chip Resistor	CRCW120627R0FKEA	Vishay

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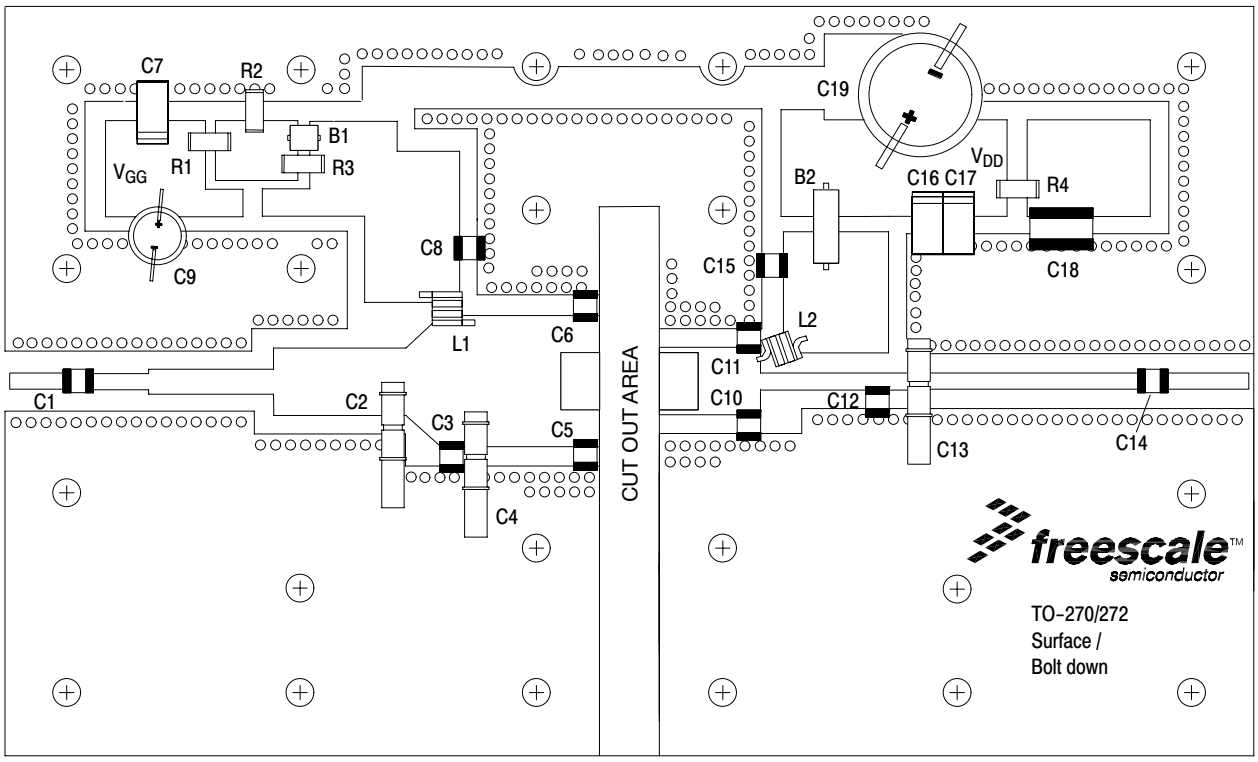

Figure 2. MRF6S9060NR1(NBR1) Test Circuit Component Layout

TYPICAL CHARACTERISTICS

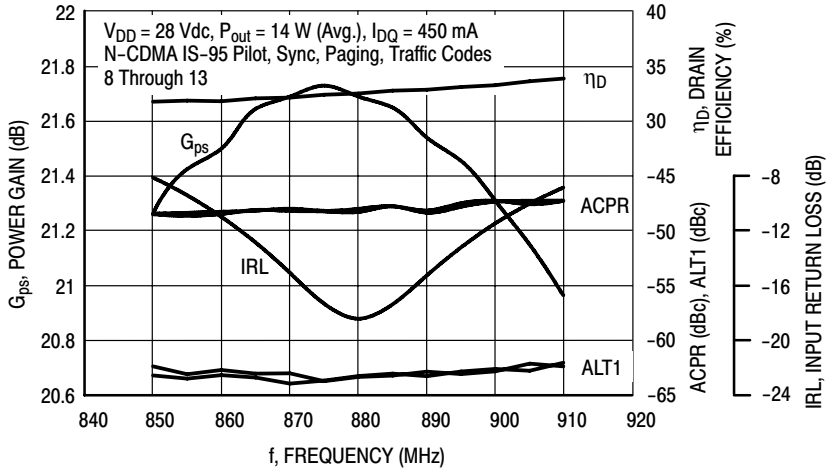

Figure 3. Single-Carrier N-CDMA Broadband Performance @ P_{out} = 14 Watts Avg.

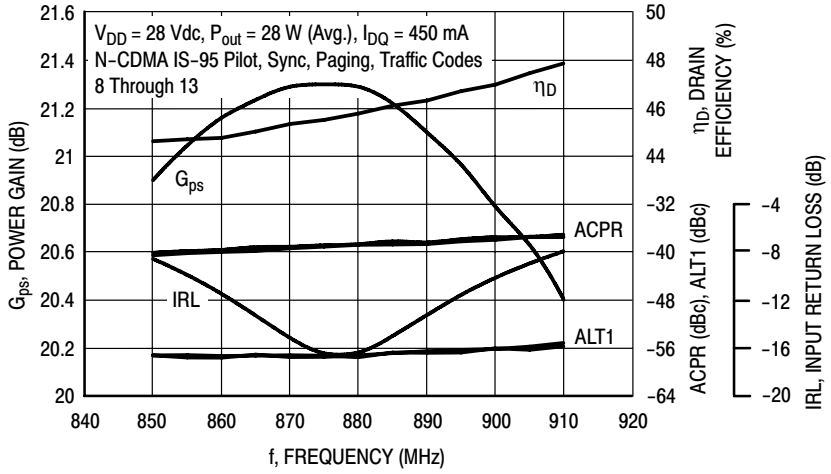

Figure 4. Single-Carrier N-CDMA Broadband Performance @ P_{out} = 28 Watts Avg.

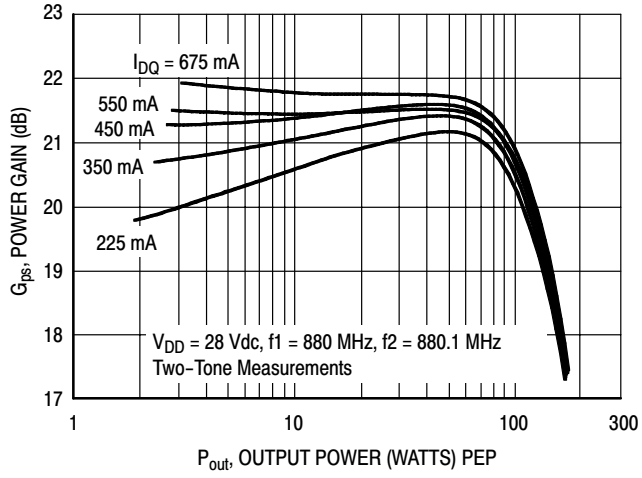

Figure 5. Two-Tone Power Gain versus Output Power

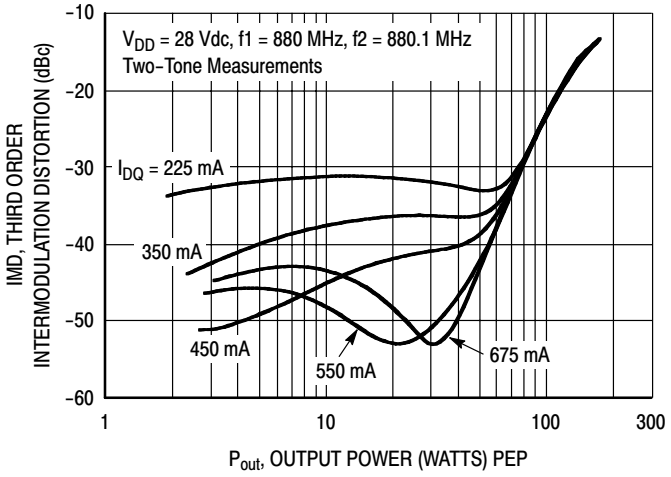

Figure 6. Third Order Intermodulation Distortion versus Output Power

ARCHIVE INFORMATION

TYPICAL CHARACTERISTICS

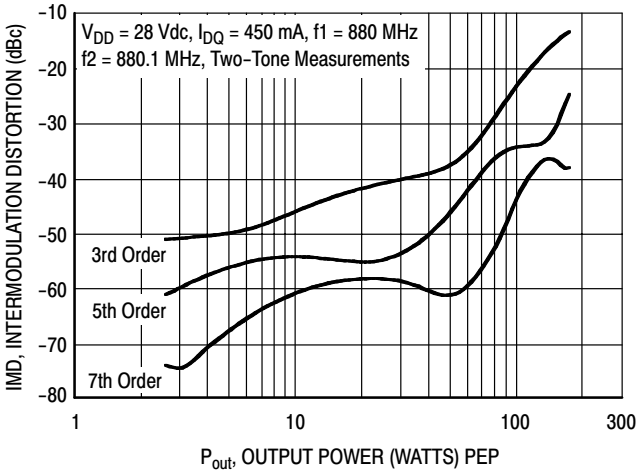

Figure 7. Intermodulation Distortion Products versus Output Power

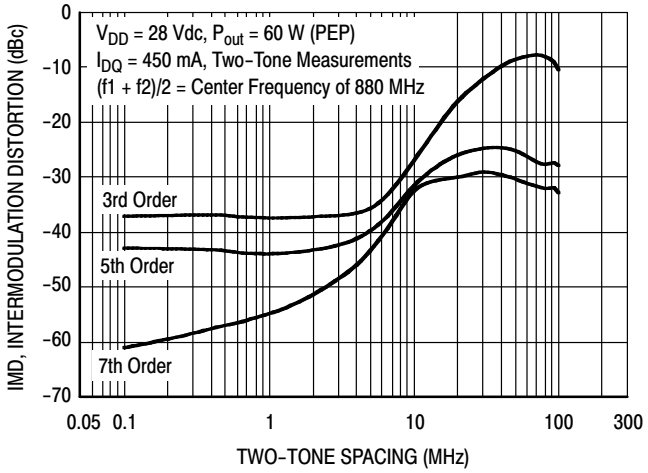

Figure 8. Intermodulation Distortion Products versus Tone Spacing

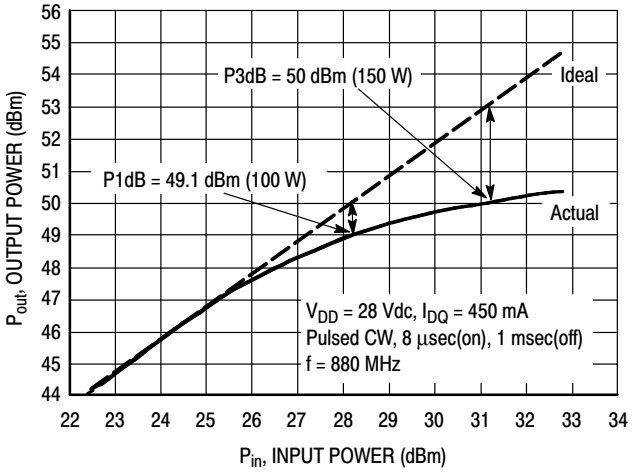

Figure 9. Pulsed CW Output Power versus Input Power

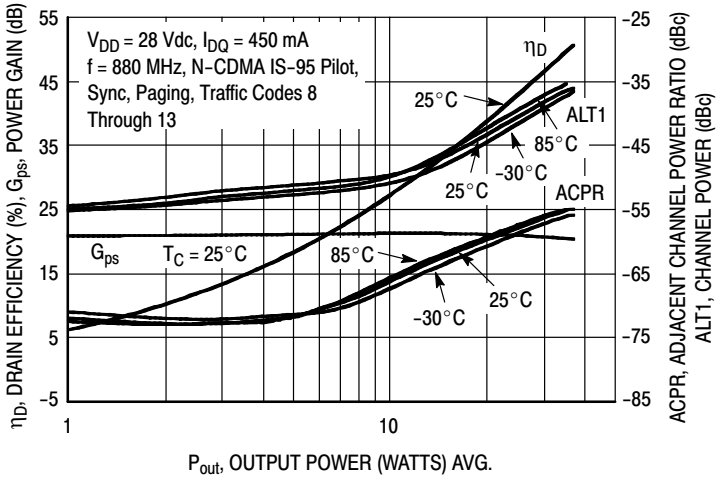

Figure 10. Single-Carrier N-CDMA ACPR, ALT1, Power Gain and Drain Efficiency versus Output Power

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TYPICAL CHARACTERISTICS

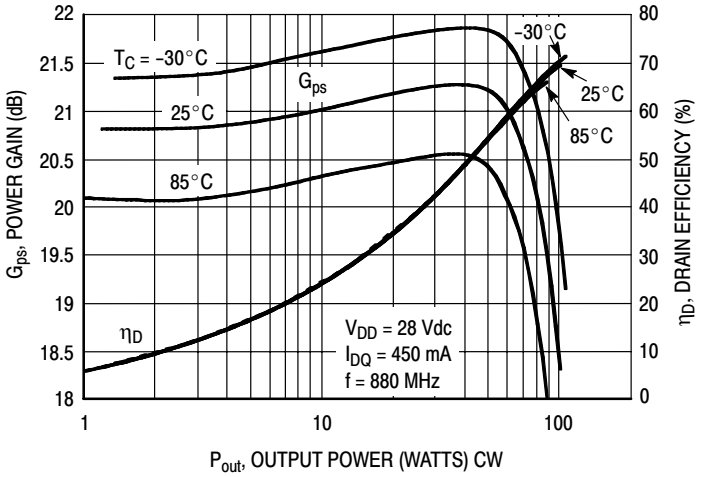


Figure 11. Power Gain and Drain Efficiency versus CW Output Power

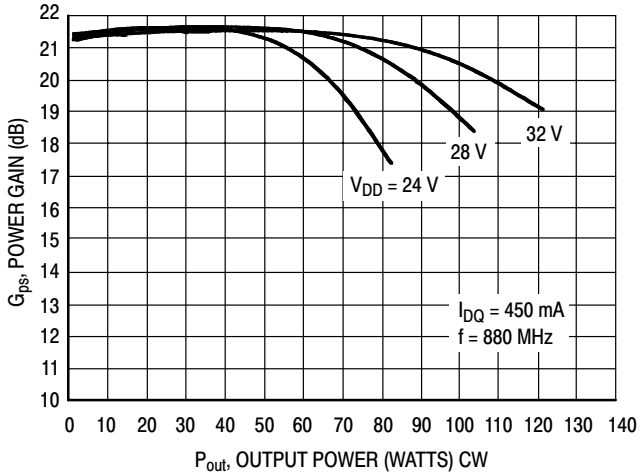
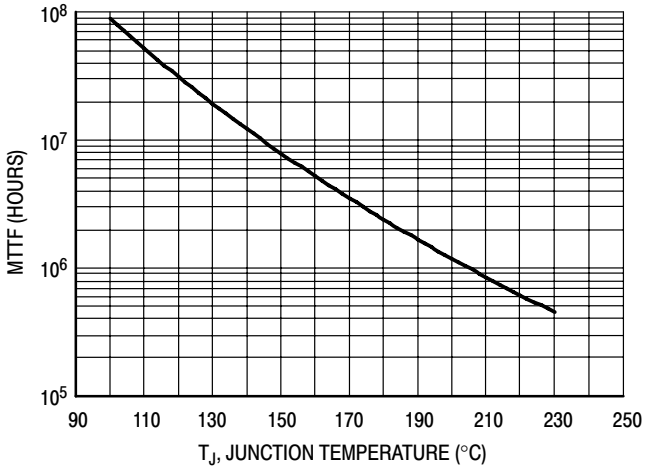


Figure 12. Power Gain versus Output Power



This above graph displays calculated MTTF in hours when the device is operated at V_{DD} = 28 Vdc, P_{out} = 14 W Avg., and η_D = 32.1%.

MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

Figure 13. MTTF Factor versus Junction Temperature

N-CDMA TEST SIGNAL

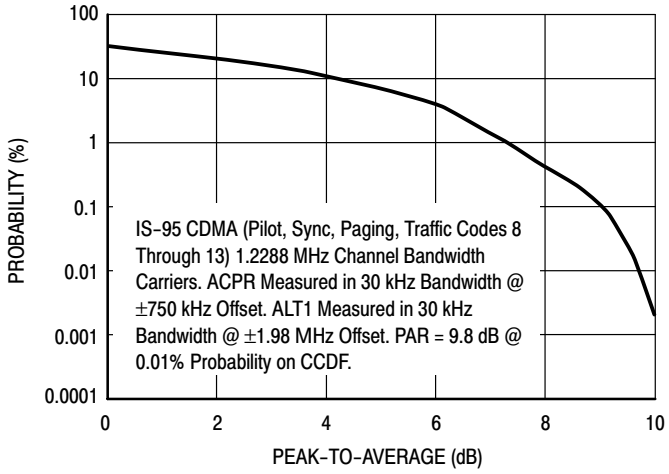


Figure 14. Single-Carrier CCDF N-CDMA

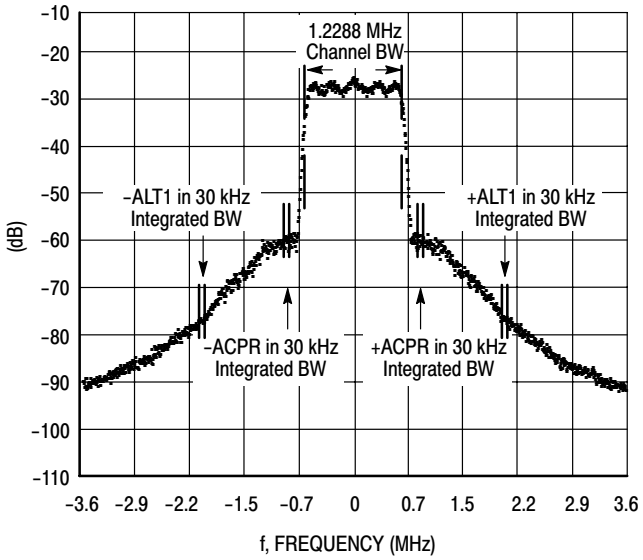


Figure 15. Single-Carrier N-CDMA Spectrum

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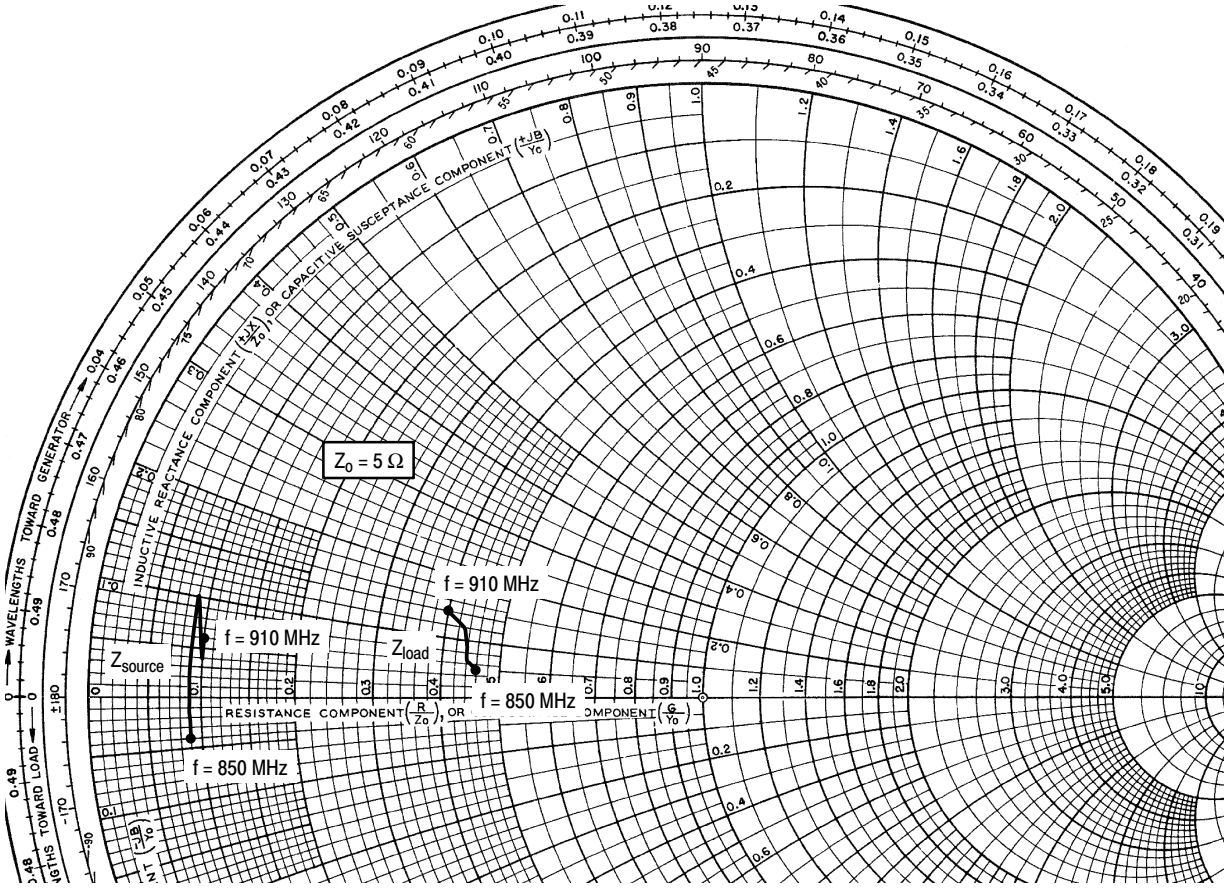


V_{DD} = 28 Vdc, I_{DQ} = 450 mA, P_{out} = 14 W Avg.

f MHz	Z_{source} Ω	Z_{load} Ω
850	0.44 - j0.20	2.28 + j0.23
865	0.44 - j0.07	2.18 + j0.33
880	0.45 + j0.50	2.20 + j0.47
895	0.48 + j0.18	2.15 + j0.61
910	0.52 + j0.29	2.00 + j0.68

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

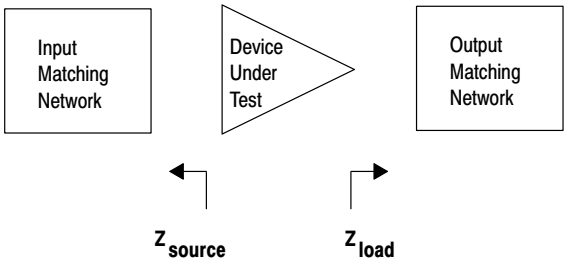
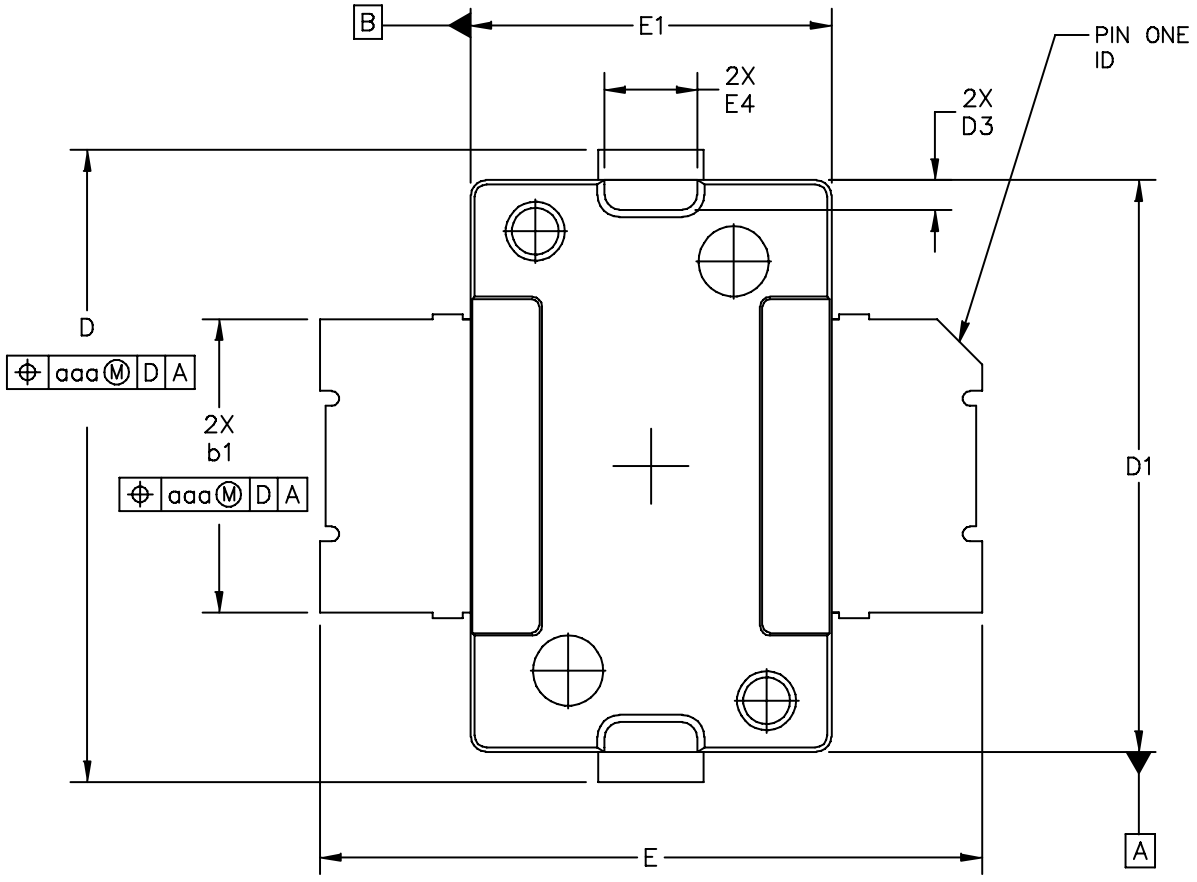
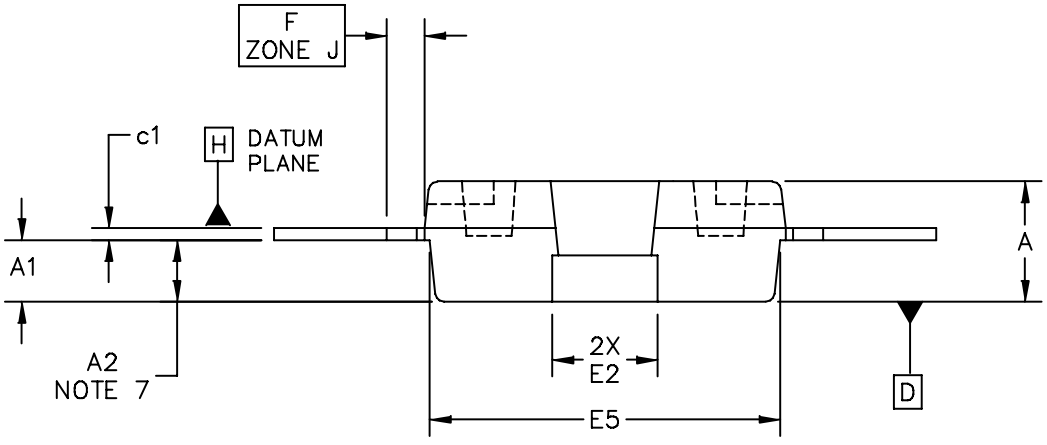


Figure 16. Series Equivalent Source and Load Impedance

ARCHIVE INFORMATION

PACKAGE DIMENSIONS





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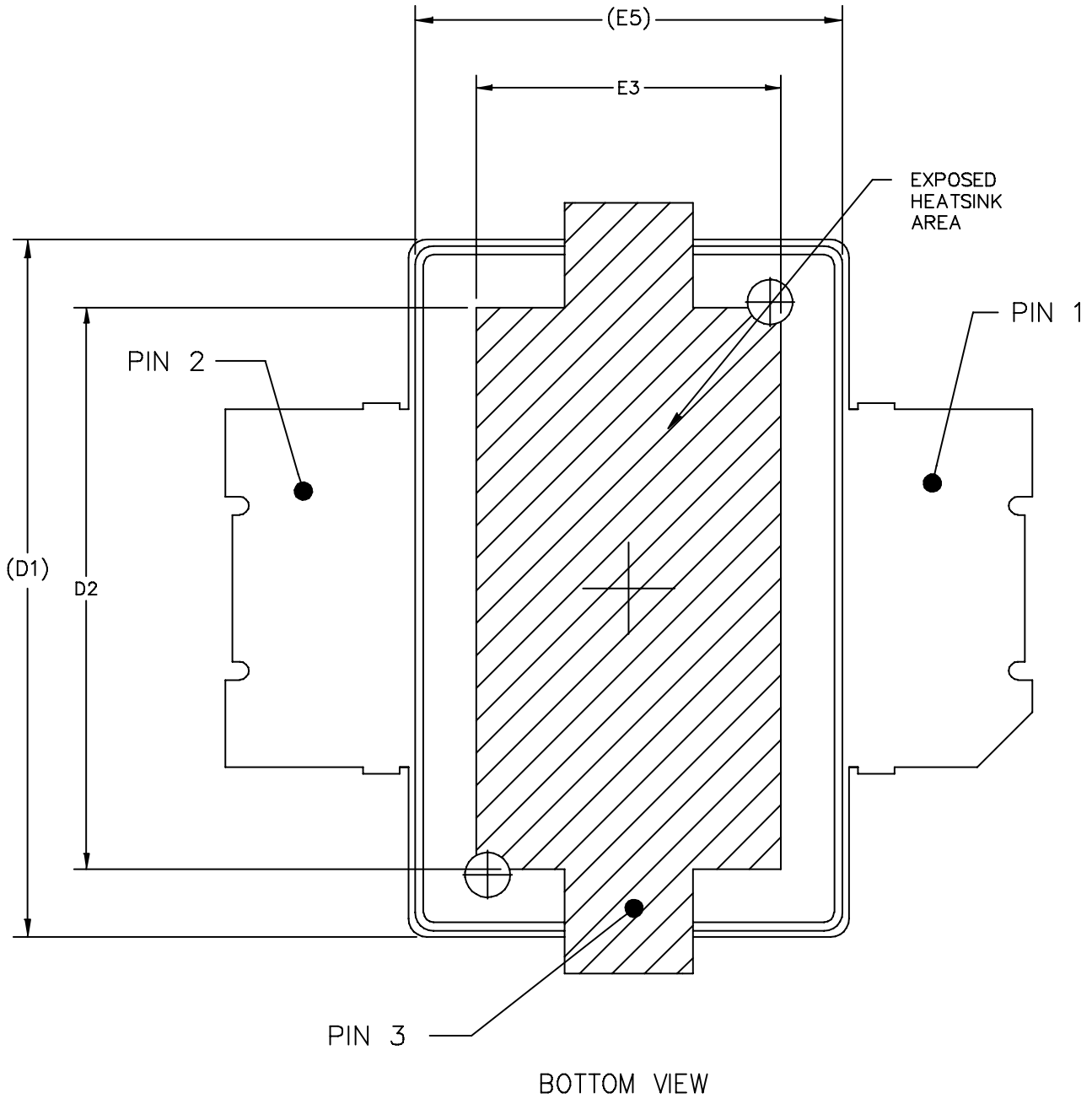
TITLE: TO−270 SURFACE MOUNT	DOCUMENT NO: 98ASH98117A	REV: K
	CASE NUMBER: 1265−09	29 JUN 2007
	STANDARD: JEDEC TO−270 AA	

ARCHIVE INFORMATION



BOTTOM VIEW

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	CASE NUMBER: 1265−09	29 JUN 2007
	STANDARD: JEDEC TO−270 AA	

NOTES:
1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M−1994.

3. DATUM PLANE −H− IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D1 AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE −H−.

5. DIMENSION "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. DATUMS −A− AND −B− TO BE DETERMINED AT DATUM PLANE −H−.

7. DIMENSION "A2" APPLIES WITHIN ZONE "J" ONLY.

8. DIMENSIONS "D" AND "E2" DO NOT INCLUDE MOLD PROTRUSION. OVERALL LENGTH INCLUDING MOLD PROTRUSION SHOULD NOT EXCEED 0.430 INCH FOR DIMENSION "D" AND 0.080 INCH FOR DIMENSION "E2". DIMENSIONS "D" AND "E2" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE −D−.

STYLE 1:
PIN 1 − DRAIN
PIN 2 − GATE
PIN 3 − SOURCE

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
A	.078	.082	1.98	2.08	F	.025 BSC		0.64 BSC	
A1	.039	.043	0.99	1.09	b1	.193	.199	4.90	5.06
A2	.040	.042	1.02	1.07	c1	.007	.011	0.18	0.28
D	.416	.424	10.57	10.77	aaa	.004		0.10	
D1	.378	.382	9.60	9.70					
D2	.290	----	7.37	----					
D3	.016	.024	0.41	0.61					
E	.436	.444	11.07	11.28					
E1	.238	.242	6.04	6.15					
E2	.066	.074	1.68	1.88					
E3	.150	----	3.81	----					
E4	.058	.066	1.47	1.68					
E5	.231	.235	5.87	5.97					

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TO−270 SURFACE MOUNT	CASE NUMBER: 1265−09	29 JUN 2007
	STANDARD: JEDEC TO−270 AA	

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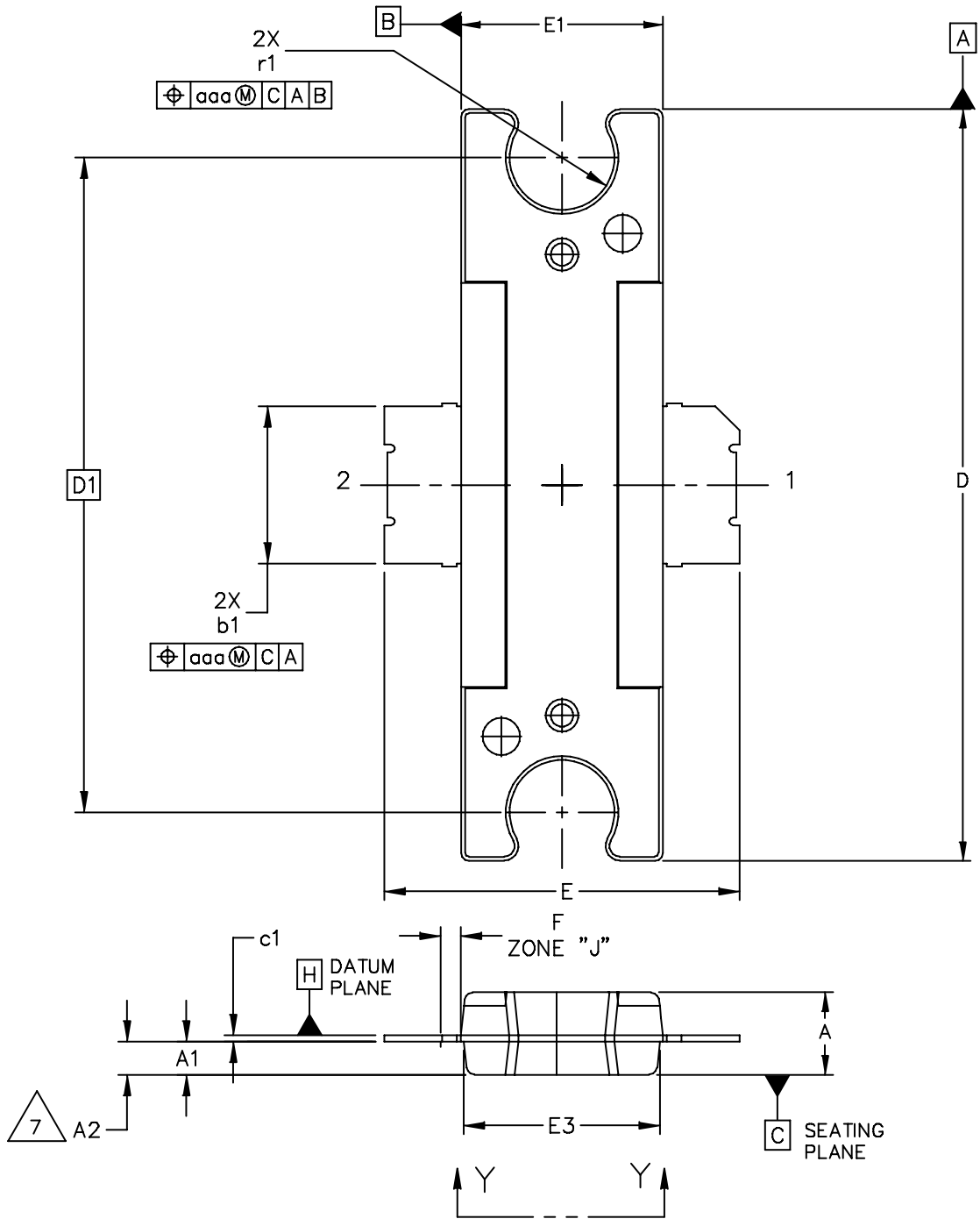

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	CASE NUMBER: 1337−04	10 SEP 2007
	STANDARD: JEDEC TO−272 BC	

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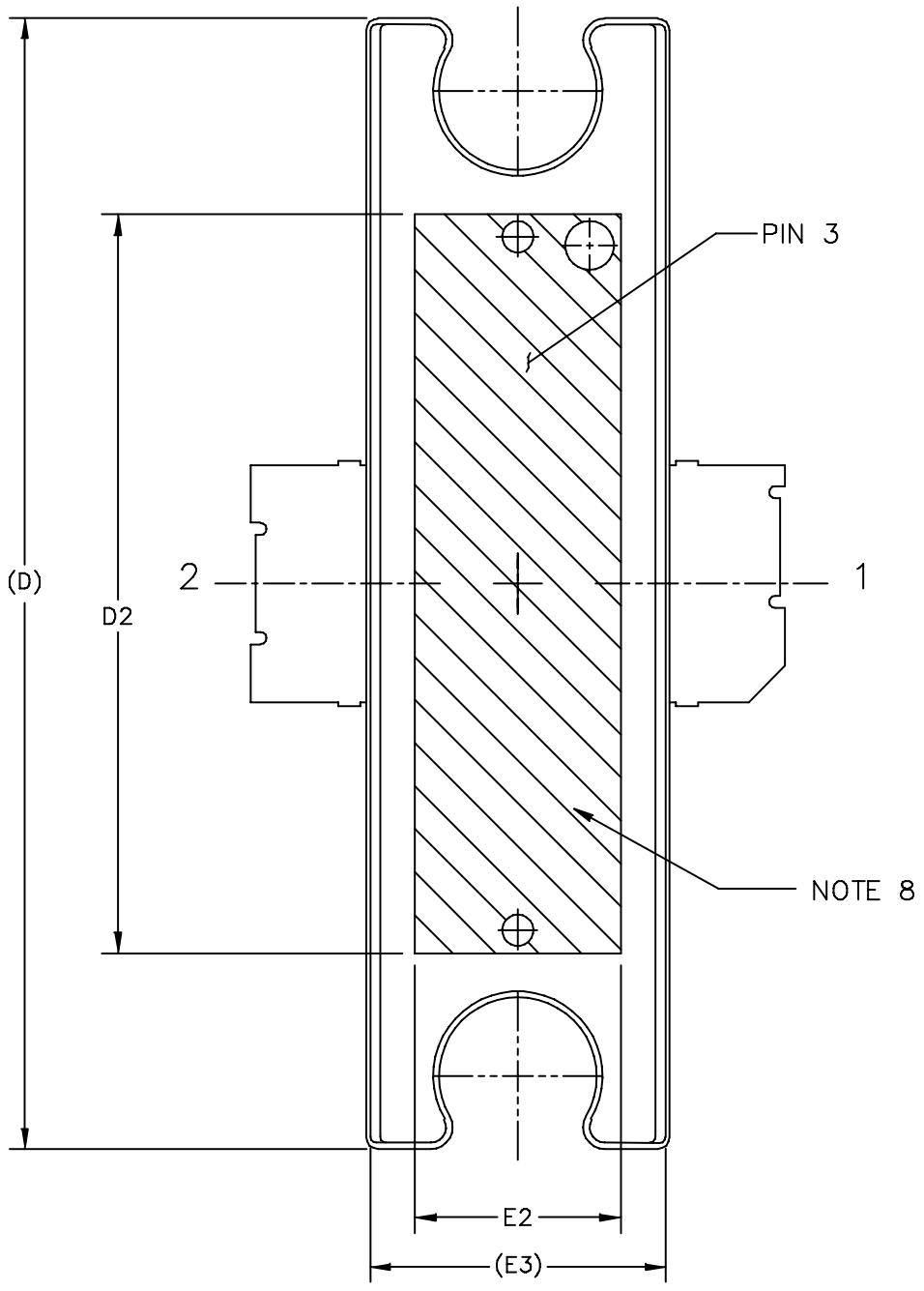

VIEW Y–Y

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TITLE: TO–272 2 LEAD	DOCUMENT NO: 98ASA99191D	REV: E
	CASE NUMBER: 1337–04	10 SEP 2007
	STANDARD: JEDEC TO–272 BC	

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE –H– IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.

5. DIMENSIONS "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. DATUMS –A– AND –B– TO BE DETERMINED AT DATUM PLANE –H–.

7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.

8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

STYLE 1:
PIN 1 – DRAIN
PIN 2 – GATE
PIN 3 – SOURCE

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	.100	.104	2.54	2.64	b1	.193	.199	4.90	5.05
A1	.039	.043	0.99	1.09	c1	.007	.011	0.18	0.28
A2	.040	.042	1.02	1.07	r1	.063	.068	1.60	1.73
D	.928	.932	23.57	23.67	aaa		.004		0.1
D1	.810 BSC		20.57 BSC						
D2	.604	----	15.34	----					
E	.438	.442	11.12	11.23					
E1	.248	.252	6.30	6.40					
E2	.162	----	4.11	----					
E3	.241	.245	6.12	6.22					
F	.025 BSC		0.64 BSC						

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TITLE:	DOCUMENT NO: 98ASA99191D	REV: E
TO–272 2 LEAD	CASE NUMBER: 1337–04	10 SEP 2007
	STANDARD: JEDEC TO–272 BS	

ARCHIVE INFORMATION

PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN3263: Bolt Down Mounting Method for High Power RF Transistors and RFICs in Over-Molded Plastic Packages

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
4	Aug. 2008	• Listed replacement part and Device Migration notification reference number, p. 1 • Listed MRF6S9060NBR1 as no longer manufactured, p. 1 • Replaced Case Outline 1265-08 with 1265-09, Issue K, p. 1, 11-13. Corrected cross hatch pattern in bottom view and changed its dimensions (D2 and E3) to minimum value on source contact (D2 changed from Min-Max .290-.320 to .290 Min; E3 changed from Min-Max .150-.180 to .150 Min). Added JEDEC Standard Package Number. • Replaced Case Outline 1337-03 with 1337-04, p. 1, 14-16. Issue D: Removed Drain-ID label from View Y-Y on Sheet 2. Renamed E2 to E3. Added cross-hatch region dimensions D2 and E2. Added JEDEC Standard Package Number. Issue E: Corrected document number 98ASA99191D on Sheet 3. • Removed Total Device Dissipation from Max Ratings table as data was redundant (information already provided in Thermal Characteristics table), p. 1 • Added Case Operating Temperature limit to the Maximum Ratings table and set limit to 150°C, p. 1 • Operating Junction Temperature increased from 200°C to 225°C in Maximum Ratings table and related “Continuous use at maximum temperature will affect MTTF” footnote added and changed 200°C to 225°C in Capable Plastic Package bullet, p. 1 • Corrected V_{DS} to V_{DD} in the RF test condition voltage callout for $V_{GS(Q)}$, and added “Measured in Functional Test”, On Characteristics table, p. 2 • Removed Forward Transconductance from On Characteristics table as it no longer provided usable information, p. 2 • Corrected C_{iss} test condition to indicate AC stimulus on the V_{GS} connection versus the V_{DS} connection, Dynamic Characteristics table, p. 2 • Updated Part Numbers in Table 6, Component Designations and Values, to latest RoHS compliant part numbers, p. 4 • Removed lower voltage tests from Fig. 12, Power Gain versus Output Power, due to fixed tuned fixture limitations, p. 8 • Replaced Fig. 13, MTTF versus Junction Temperature with updated graph. Removed $Amps^2$ and listed operating characteristics and location of MTTF calculator for device, p. 8 • Added Product Documentation and Revision History, p. 17

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