Device Description

The ZABG series of devices are designed to meet the bias requirements of GaAs and HEMT FETs commonly used in satellite receiver LNBs with a minimum of external components whilst operating from a minimal voltage supply and using minimal current.

The ZABG4002 provides four FET bias stages, arranged in two pairs of two. Resistors connected to pins R_{CAL1} and R_{CAL2} set the FET drain currents of each pair over the range of 0 to 15mA, allowing input FETs to be biased for optimum noise and amplifier FETs for optimum gain.

Drain voltages of all stages are set at 2.0V. The drain supplies are current limited to approximately 5% above the operating currents set by the R_{CAL} resistors.

As an additional feature the R_{CAL} pins can also be used as logic inputs to disable pairs of FETs as part of a power management scheme or simply an alternative to LNA switching. Driven to a logic high (>3.0V), the inputs disable their associated FET bias stages by switching gate feeds to -2.5V and drain feeds open circuit.

Depletion mode FETs require a negative voltage bias supply when operated in grounded source circuits. The ZABG4002 includes an integrated low noise switched capacitor DC-DC converter generating a regulated output of -2.5V to allow single supply operation.

To facilitate the design of efficient low voltage 3.3V LNB systems and to maintain compatibility with higher voltage legacy designs, the ZABG4002 is capable of operating within the supply of 3.0V to 8V.

These devices are unconditionally stable over the full working temperature with the FETs in place, subject to the inclusion of the recommended gate and drain capacitors. These ensure RF stability and minimal injected noise.

It is possible to use less than the devices full complement of FET bias controls, unused drain and gate connections can be left open circuit without affecting operation of the remaining bias circuits.

To protect the external FETs the circuits have been designed to ensure that, under any conditions including power up/down transients, the gate drive from the bias circuits cannot exceed -3V. Additionally each stage has its own individual current limiter. Furthermore if the negative rail experiences a fault condition, such as overload or short circuit, the drain supply to the FETs will shut down avoiding excessive current flow.

To minimise PCB space ZABG4002 is packaged in the 16 pin 3mm x 3mm QFN1633 package.

Device operating temperature is -40°C to +85°C to suit a wide range of environmental conditions.

Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.6 to +10	V
Supply Current	80	mA
Power Dissipation	500	mW
Operating Temperature Range	-40 to +85	°C
Storage Temperature Range	-40 to +150	°C

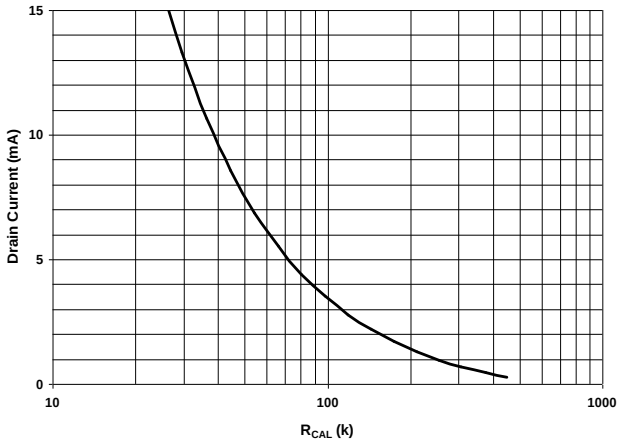
Electrical Characteristics (Measured at T_A = +25°C, V_{CC} = 3.3V (Note 4), R_{CAL1} = R_{CAL2} = 39kΩ (setting I_D to 10mA), unless otherwise stated.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating Voltage Range (Note 4)	—	3.0	—	8.0	V
I_{CC}	Supply Current	I_{D1} = I_{D2} = I_{D3} = I_{D4} = 0	—	1.2	4.0	mA
$I_{CC(L)}$		I_{D1} = I_{D2} = I_{D3} = I_{D4} = 10mA	—	42	44	mA
V_{CSUB}	Substrate Voltage	I_{CSUB} = 0	-3.0	-2.65	-2.0	V
$V_{CSUB(L)}$		I_{CSUB} = -200µA	—	-2.55	-2.0	V
f_{OSC}	Oscillator Frequency	—	150	240	600	kHz
Gate Characteristics						
Gate (G1 to G4)						
I_G	Current Range	—	-100	—	+500	µA
$V_{G(L)}$	Voltage Low	I_D = 12mA, I_G = -10µA	-3.0	-2.5	-2.0	V
$V_{G(H)}$	Voltage High	I_D = 8mA, I_G = 0	0	0.7	1.0	V
$V_{G(DIS)}$	Voltage Disabled	I_D = 0, I_G = -10µA, V_{RCAL} = 3.0V	-3.0	-2.5	-2.0	V
Drain Characteristics						
Drain (D1 to D4)						
I_D	Current Range	—	0	—	15	mA
$I_{D(OP)}$	Current Operating	Standard Application Circuit	8	10	12	mA
$I_{D(DIS)}$	Current Disabled	V_D = 0, V_{RCAL} = 3.0V	—	—	10	µA
$V_{D(OP)}$	Voltage Operating	I_D = 10mA	1.8	2.0	2.2	V
dI_D/dV_{CC}	Delta I_D vs V_{CC}	V_{CC} = 3.3 to 8.0V	—	1.2	—	%/V
dI_D/dT_{OP}	Delta I_D vs T_{OP}	T_{OP} = -40°C to +85°C	—	0.05	—	%/°C
dV_D/dV_{CC}	Delta V_D vs V_{CC}	V_{CC} = 3.3 to 8.0V	—	0.05	—	%/V
dV_D/dT_{OP}	Delta V_D vs T_{OP}	T_{OP} = -40°C to +85°C	—	50	—	ppm/°C
R_{CAL}(1 and 2)						
$V_{RCAL(DIS)}$	Disable Threshold	—	1.8	2.7	3.0	V
$I_{RCAL(DIS)}$	Input Current	V_{RCAL} = 3.0V	—	1.7	10	µA
Output Noise						
$V_{D(NOISE)}$	Drain Voltage	$C_{GATE-GND}$ = 10nF, $C_{DRAIN-GND}$ = 10nF	—	—	0.02	Vpk-pk
$V_{G(NOISE)}$	Gate Voltage	$C_{GATE-GND}$ = 10nF, $C_{DRAIN-GND}$ = 10nF	—	—	0.005	Vpk-pk

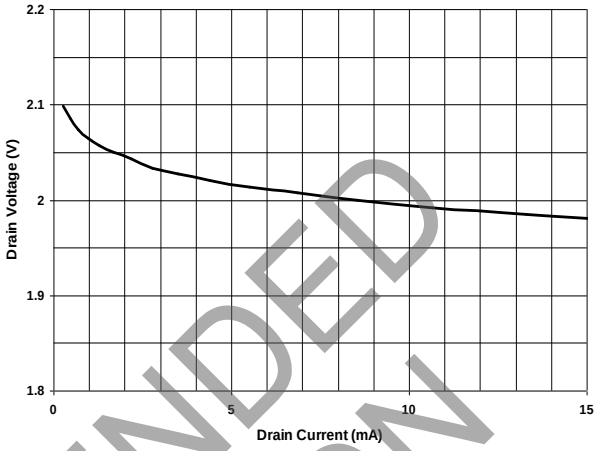
Notes:
4. The two V_{CC} pins are internally connected, only one of the pins needs to be powered for the device to function. See applications section for further information.
5. ESD sensitive, handling precautions are recommended.
6. The negative bias voltages are generated on-chip using an internal oscillator. Two external capacitors, C_{NB} and C_{SUB} of value 47nF are required for this purpose.
7. The package (QFN1633) exposed pad must either be connected to C_{SUB} or left open circuit.
8. The characteristics are measured using two external reference resistors R_{CAL1} and R_{CAL2} of value 39kΩ, wired from pins $R_{CAL1/2}$ to ground. Resistor R_{CAL1} sets the drain current of FETs 1 and 3, resistor R_{CAL2} sets the drain currents of FETs 2 and 4.
9. Noise voltage measurements are made with FETs and gate and drain capacitors of value 10nF in place. Noise voltages are not measured in production.

Typical Characteristics (Measured at T_A = +25°C, V_{CC} = 3.3V, R_{CAL1} = R_{CAL2} = 39kΩ (setting I_D to 10mA), unless otherwise stated.)

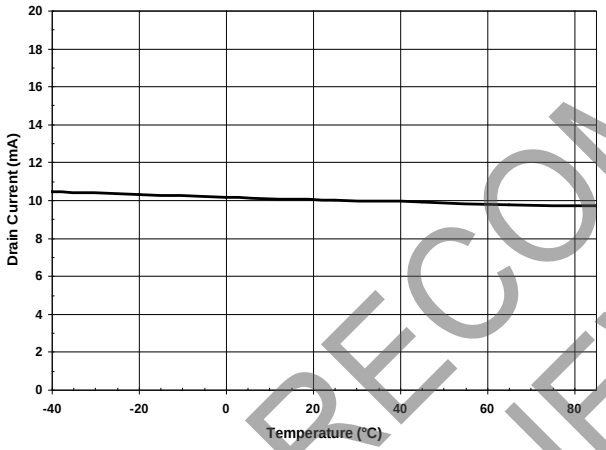
ZABG4002 Drain Current vs R_{CAL}



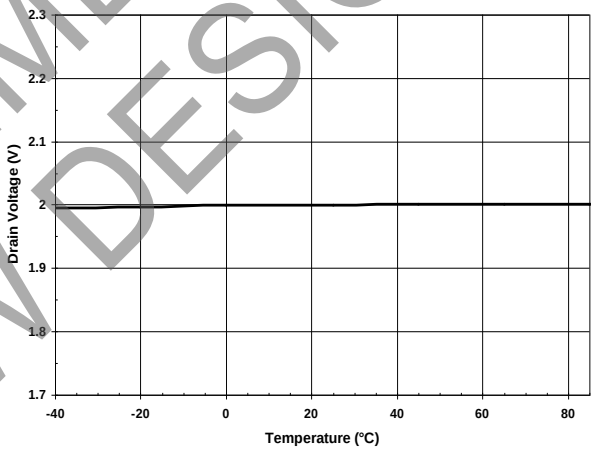
ZABG4002 Drain Voltage vs Drain Current



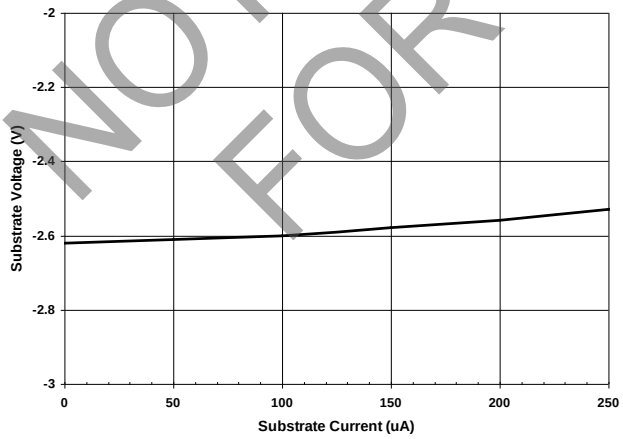
ZABG4002 Drain Current vs Temperature



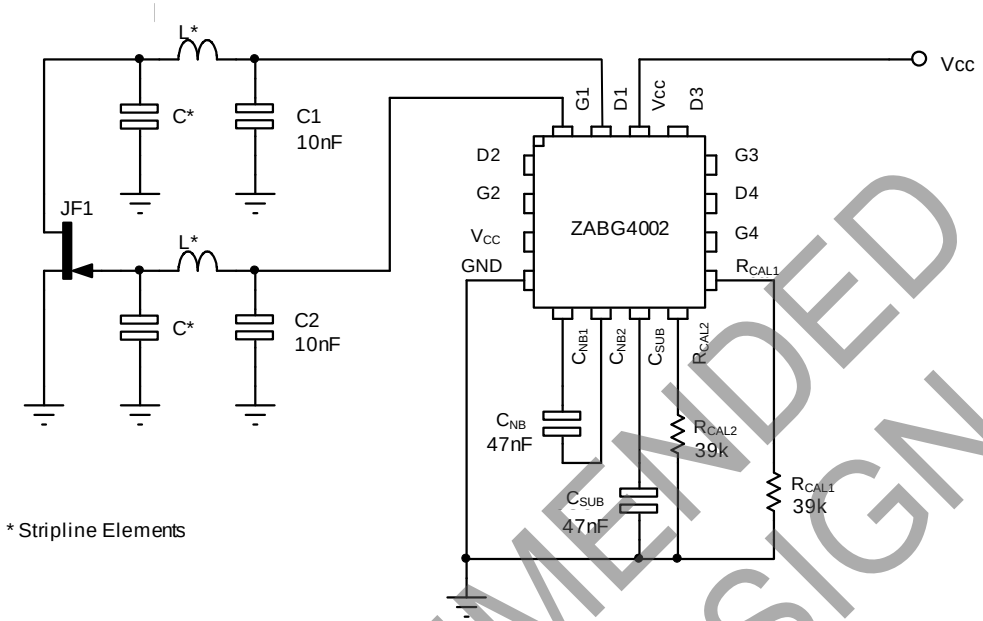
ZABG4002 Drain Voltage vs Temperature



ZABG4002 Substrate Voltage vs Substrate Current



Applications Circuit



Applications Information

Above is a partial applications circuit for the ZABG4002 showing all external components needed for biasing one of the four FET stages available. Each bias stage is provided with a gate and drain pin. The drain pin provides a regulated 2.0V supply that includes a drain current monitor. The drain current taken by the external FET is compared with a user selected level, generating a signal that adjusts the gate voltage of the FET to obtain the required drain current. If for any reason, an attempt is made to draw more than the user set drain current from the drain pin, the drain voltage will be reduced to ensure excess current is not taken. The gate pin drivers are also current limited.

The bias stages are split up into two pairs, with the drain current of each pair set by an external R_{CAL} resistor. R_{CAL1} sets the drain currents of stages 1 and 3, whilst R_{CAL2} sets the drain currents of stages 2 and 4. This allows the optimisation of drain currents for differing tasks such as input stages where noise can be critical and later amplifier stages where gain may be more important. A graph showing the relationship between the value of R_{CAL} and I_D is provided in the Typical Characteristics section of this datasheet. The R_{CAL} pins can also be used as logic inputs. If set to a logic high state (>3.0V), the associated FET bias stages are disabled, driving gate pins to -2.5V and switching drain pins open-circuit. This feature can be used as part of a power management system that turns off any unwanted stages in a multi input receiver.

The ZABG4002 includes a switched capacitor DC-DC converter that is used to generate the negative supply required to bias depletion mode FETs used in common source circuit configuration as shown above. This converter uses two external capacitors, C_{NB} the charge transfer capacitor and C_{SUB} the output reservoir capacitor. The circuit provides a regulated -2.5V supply both for gate driver use and for external use if required (for extra discrete bias stages, mixer bias, local oscillator bias etc.). The -2.5V supply is available from the C_{SUB} pin.

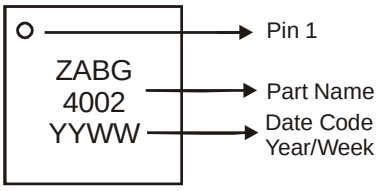
If any bias stages are not required, their gate and drain pins may be left open circuit. If all bias stages associated with an R_{CAL} resistor are not required, then this resistor may be omitted.

To ease PCB layout, the pinout for the ZABG4002 includes two V_{CC} pins. These pins are internally connected so only one of the pins needs to be powered for the device to function. It is probable that the extra pin will help avoid the need for trace cross-over components or ground plane disruption from reverse side PCB links. Note that the exposed pad of the package must be either left floating or connected to C_{SUB}.

Ordering Information

Part Number	Package	Reel Size (inches)	Tape Width (mm)	Quantity (Per Reel)
ZABG4002JA16TC	QFN1633	13	8	3000

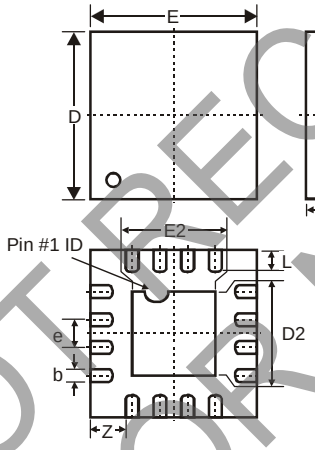
Marking Information



Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

QFN1633



QFN1633		
Dim	**Min**	**Max**
A	0.55	0.65
A1	0.00	0.05
A3	0.15 Typ	
b	0.18	0.28
D	2.95	3.05
D2	1.40	1.60
e	0.50 BSC	
E	2.95	3.05
E2	1.40	1.60
L	0.35	0.45
Z	0.625 Typ	
All Dimensions in mm		

Note 10: Controlling dimensions are in millimetres. Approximate dimensions are provided in inches.
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