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REVISION HISTORY

4/13—Rev. 0 to Rev. A

Changes to Figure 33 and Figure 34 ... 12
Changes to Gain Selection Section and Table 5 ... 13
Updated Outline Dimensions ... 15

9/10—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 5.0 V, T_A = 25°C, R_L = 8 Ω +33 µH, EDGE = GND, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DEVICE CHARACTERISTICS						
Output Power	P_O	f = 1 kHz, 20 kHz BW				
		R_L = 8 Ω, THD = 1%, V_{DD} = 5.0 V		1.42		W
		R_L = 8 Ω, THD = 1%, V_{DD} = 3.6 V		0.72		W
		R_L = 8 Ω, THD = 1%, V_{DD} = 2.5 V		0.33		W
		R_L = 8 Ω, THD = 10%, V_{DD} = 5.0 V		1.77		W
		R_L = 8 Ω, THD = 10%, V_{DD} = 3.6 V		0.91		W
		R_L = 8 Ω, THD = 10%, V_{DD} = 2.5 V		0.42		W
		R_L = 4 Ω, THD = 1%, V_{DD} = 5.0 V		2.52		W
		R_L = 4 Ω, THD = 1%, V_{DD} = 3.6 V		1.28		W
		R_L = 4 Ω, THD = 1%, V_{DD} = 2.5 V		0.56		W
		R_L = 4 Ω, THD = 10%, V_{DD} = 5.0 V		3.17[1]		W
		R_L = 4 Ω, THD = 10%, V_{DD} = 3.6 V		1.6		W
		R_L = 4 Ω, THD = 10%, V_{DD} = 2.5 V		0.72		W
		R_L = 3 Ω, THD = 1%, V_{DD} = 5.0 V		3.2[1]		W
		R_L = 3 Ω, THD = 1%, V_{DD} = 3.6 V		1.52		W
		R_L = 3 Ω, THD = 1%, V_{DD} = 2.5 V		0.68		W
		R_L = 3 Ω, THD = 10%, V_{DD} = 5.0 V		3.7[1]		W
		R_L = 3 Ω, THD = 10%, V_{DD} = 3.6 V		1.9		W
		R_L = 3 Ω, THD = 10%, V_{DD} = 2.5 V		0.85		W
Efficiency	η	P_O = 1.4 W into 8 Ω, V_{DD} = 5.0 V		93		%
Total Harmonic Distortion + Noise	THD + N	P_O = 1 W into 8 Ω, f = 1 kHz, V_{DD} = 5.0 V		0.01		%
		P_O = 0.5 W into 8 Ω, f = 1 kHz, V_{DD} = 3.6 V		0.01		%
Input Common-Mode Voltage Range	V_{CM}		1.0		V_{DD} − 1	V
Common-Mode Rejection Ratio	$CMRR_{GSM}$	V_{CM} = 2.5 V ± 100 mV, f = 217 Hz, output referred		55		dB
Average Switching Frequency	f_{SW}			250		kHz
Differential Output Offset Voltage	V_{OOS}	Gain = 6 dB		0.1	2.0	mV
POWER SUPPLY						
Supply Voltage Range	V_{DD}	Guaranteed from PSRR test	2.5		5.5	V
Power Supply Rejection Ratio	PSRR	Inputs are ac-grounded, C_{IN} = 0.1 µF				
		V_{RIPPLE} = 100 mV at 217 Hz		80		dB
		V_{RIPPLE} = 100 mV at 1 kHz		80		dB
Supply Current	I_{SY}	V_{IN} = 0 V, no load, V_{DD} = 5.0 V		3.0		mA
		V_{IN} = 0 V, no load, V_{DD} = 3.6 V		2.7		mA
		V_{IN} = 0 V, no load, V_{DD} = 2.5 V		2.5		mA
		V_{IN} = 0 V, R_L = 8 Ω + 33 µH, V_{DD} = 5.0 V		3.1		mA
		V_{IN} = 0 V, R_L = 8 Ω + 33 µH, V_{DD} = 3.6 V		2.8		mA
		V_{IN} = 0 V, R_L = 8 Ω + 33 µH, V_{DD} = 2.5 V		2.6		mA
Shutdown Current	I_{SD}	$\overline{SD}$ = GND		20		nA
GAIN CONTROL						
Closed-Loop Gain	Gain		0		12	dB
Input Impedance	Z_{IN}	$\overline{SD}$ = VDD, fixed input impedance (0 dB to 12 dB)		80		kΩ
SHUTDOWN CONTROL						
Input Voltage High	V_{IH}		1.35			V
Input Voltage Low	V_{IL}				0.35	V
Turn-On Time	t_{WU}	$\overline{SD}$ rising edge from GND to VDD		12.5		ms
Turn-Off Time	t_{SD}	$\overline{SD}$ falling edge from VDD to GND		5		µs
Output Impedance	Z_{OUT}	$\overline{SD}$ = GND		>100		kΩ

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
NOISE PERFORMANCE						
Output Voltage Noise	e_n	V_{DD} = 5.0 V, f = 20 Hz to 20 kHz, inputs are ac-grounded, gain = 6 dB, A-weighted		30		μV rms
Signal-to-Noise Ratio	SNR	P_O = 1.4 W, R_L = 8 Ω		100		dB

[1] Although the SSM2375 has good audio quality above 3 W, continuous output power beyond 3 W without a heat sink must be avoided due to device packaging limitations.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings apply at 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	V_{DD}
Common-Mode Input Voltage	V_{DD}
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	−65°C to +165°C
Lead Temperature (Soldering, 60 sec)	300°C
ESD Susceptibility	4 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	PCB	θ_{JA}	θ_{JB}	Unit
9-Ball, 1.5 mm × 1.5 mm WLCSP	1S0P	162	39	°C/W
	2S0P	76	21	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

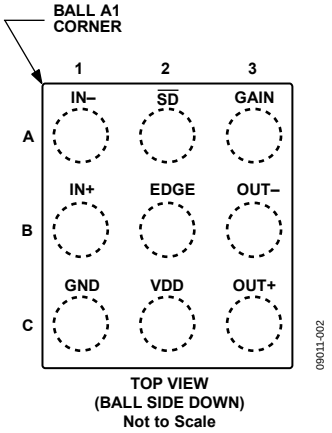

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1A	IN–	Inverting Input.
1B	IN+	Noninverting Input.
1C	GND	Ground.
2A	$\overline{SD}$	Shutdown Input. Active low digital input.
2B	EDGE	Edge Rate Control. Active high.
2C	VDD	Power Supply.
3A	GAIN	Gain Control Pin.
3B	OUT–	Inverting Output.
3C	OUT+	Noninverting Output.

TYPICAL PERFORMANCE CHARACTERISTICS

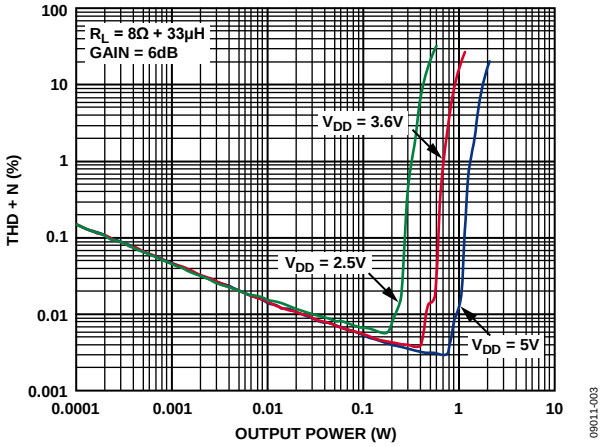

Figure 3. THD + N vs. Output Power into 8 Ω, Gain = 6 dB

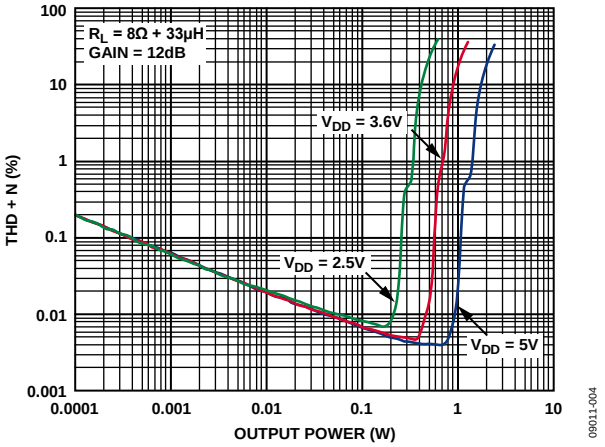

Figure 6. THD + N vs. Output Power into 8 Ω, Gain = 12 dB

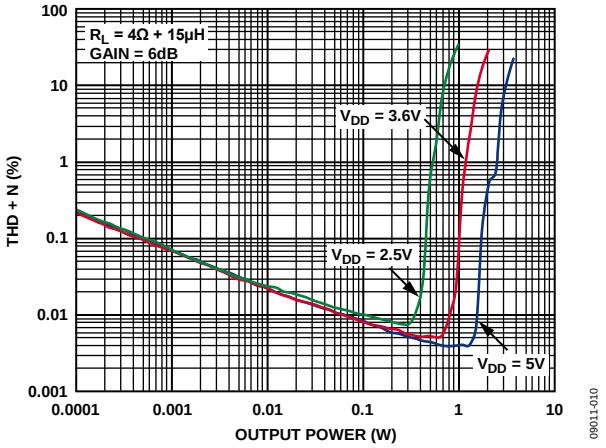

Figure 4. THD + N vs. Output Power into 4 Ω, Gain = 6 dB

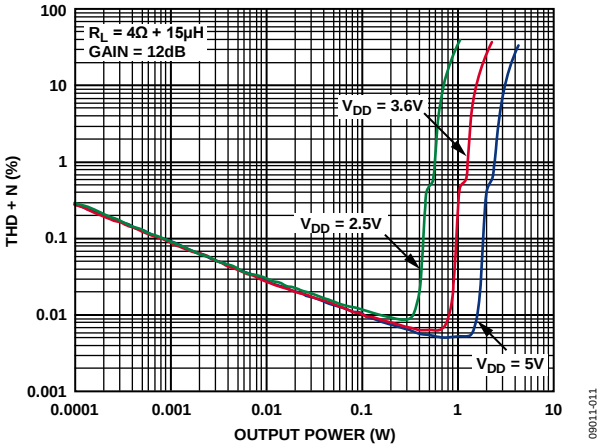

Figure 7. THD + N vs. Output Power into 4 Ω, Gain = 12 dB

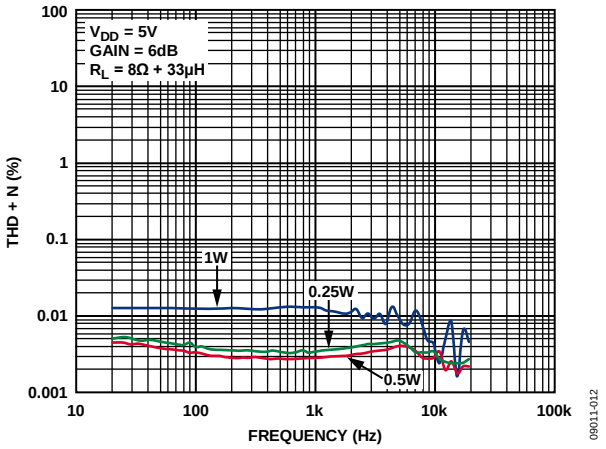

Figure 5. THD + N vs. Frequency, V_{DD} = 5 V, R_L = 8 Ω, Gain = 6 dB

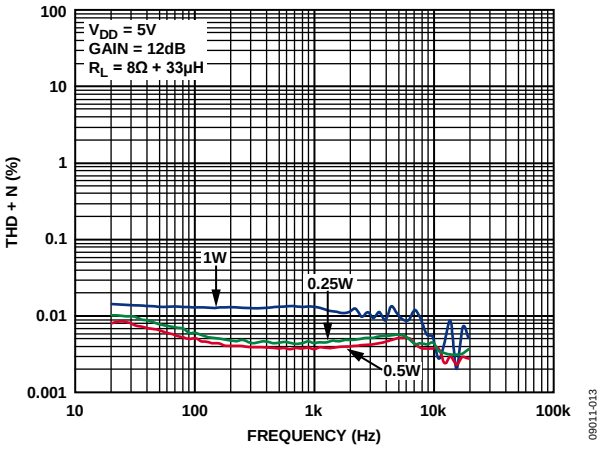

Figure 8. THD + N vs. Frequency, V_{DD} = 5 V, R_L = 8 Ω, Gain = 12 dB

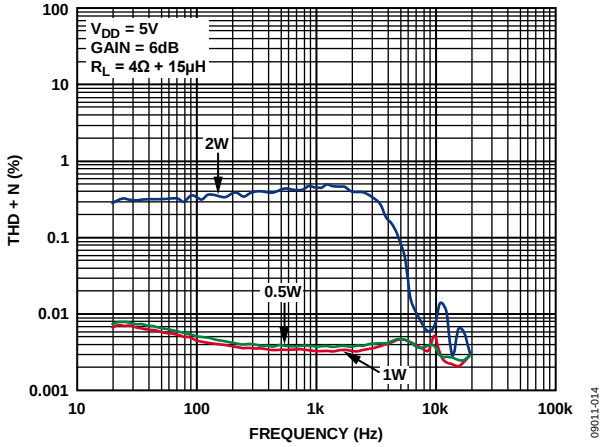

Figure 9. THD + N vs. Frequency, V_{DD} = 5 V, R_L = 4 Ω, Gain = 6 dB

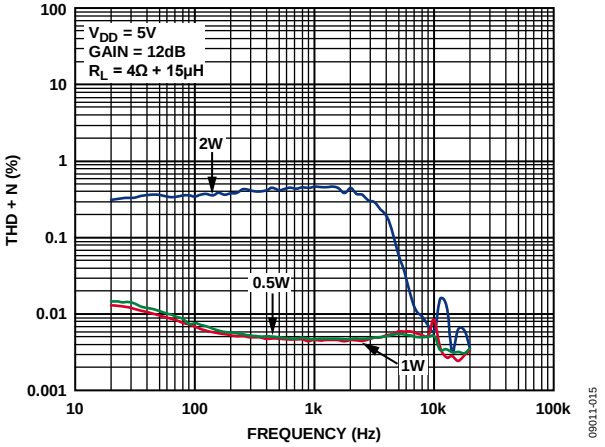

Figure 12. THD + N vs. Frequency, V_{DD} = 5 V, R_L = 4 Ω, Gain = 12 dB

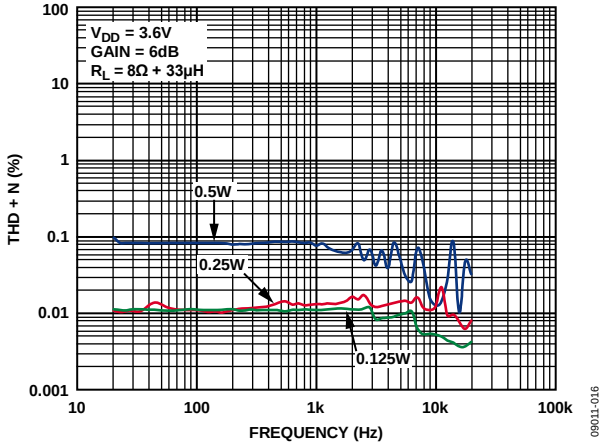

Figure 10. THD + N vs. Frequency, V_{DD} = 3.6 V, R_L = 8 Ω, Gain = 6 dB

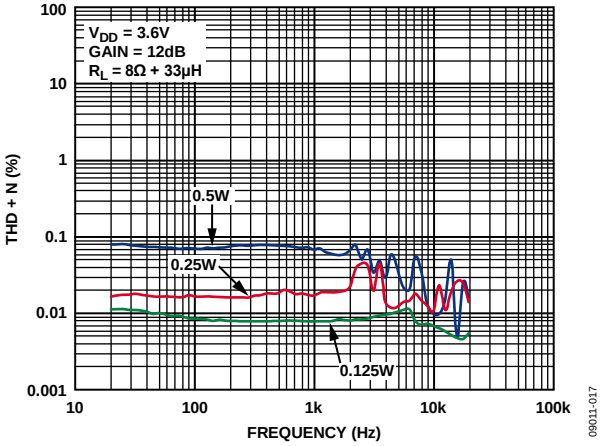

Figure 13. THD + N vs. Frequency, V_{DD} = 3.6 V, R_L = 8 Ω, Gain = 12 dB

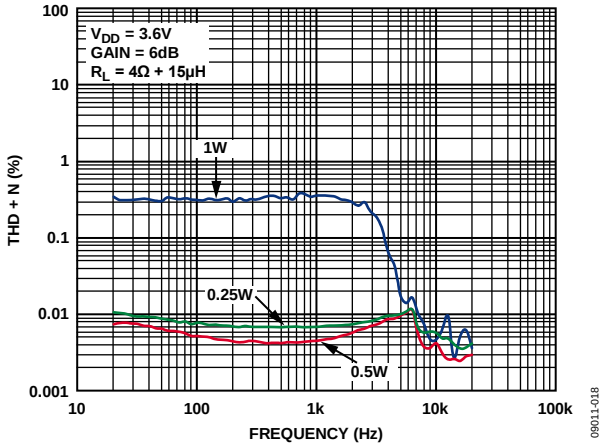

Figure 11. THD + N vs. Frequency, V_{DD} = 3.6 V, R_L = 4 Ω, Gain = 6 dB

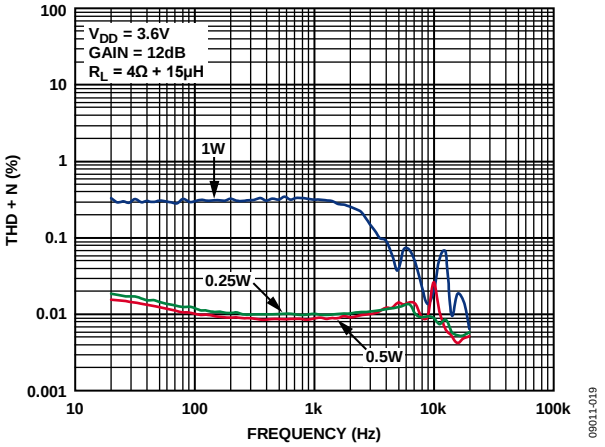

Figure 14. THD + N vs. Frequency, V_{DD} = 3.6 V, R_L = 4 Ω, Gain = 12 dB

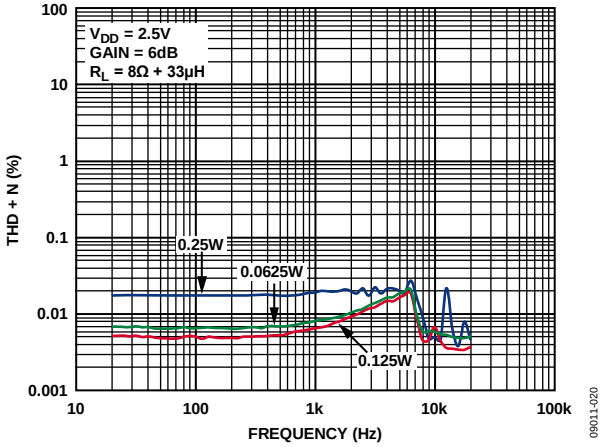

Figure 15. THD + N vs. Frequency, V_{DD} = 2.5 V, R_L = 8 Ω, Gain = 6 dB

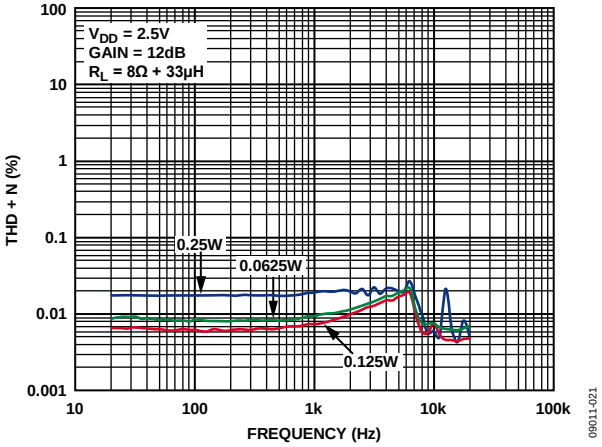

Figure 18. THD + N vs. Frequency, V_{DD} = 2.5 V, R_L = 8 Ω, Gain = 12 dB

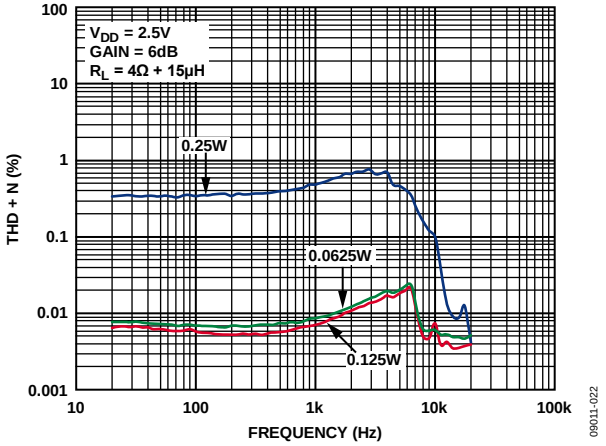

Figure 16. THD + N vs. Frequency, V_{DD} = 2.5 V, R_L = 4 Ω, Gain = 6 dB

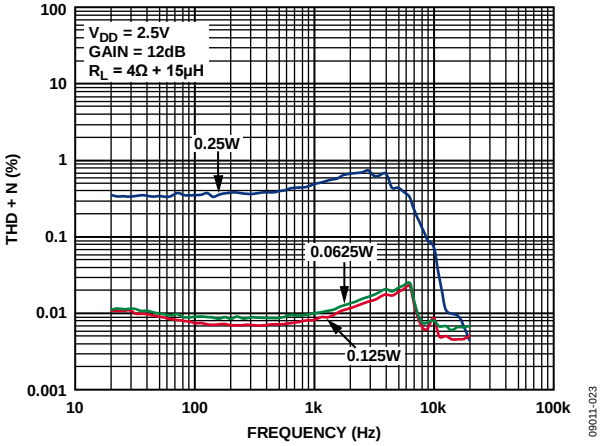

Figure 19. THD + N vs. Frequency, V_{DD} = 2.5 V, R_L = 4 Ω, Gain = 12 dB

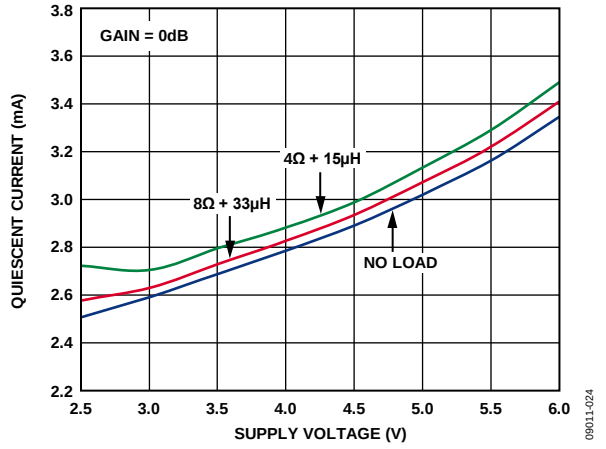

Figure 17. Quiescent Current vs. Supply Voltage, Gain = 0 dB

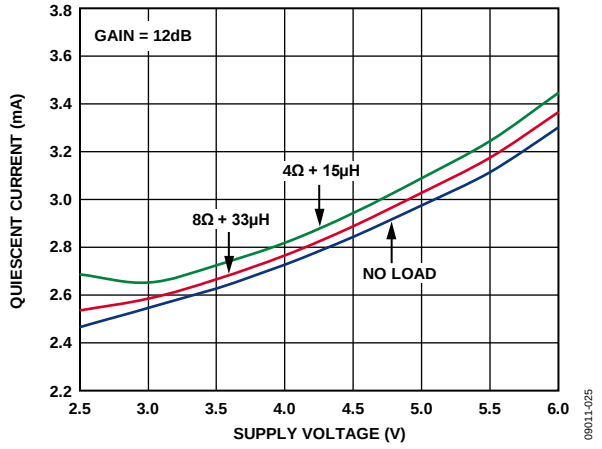

Figure 20. Quiescent Current vs. Supply Voltage, Gain = 12 dB

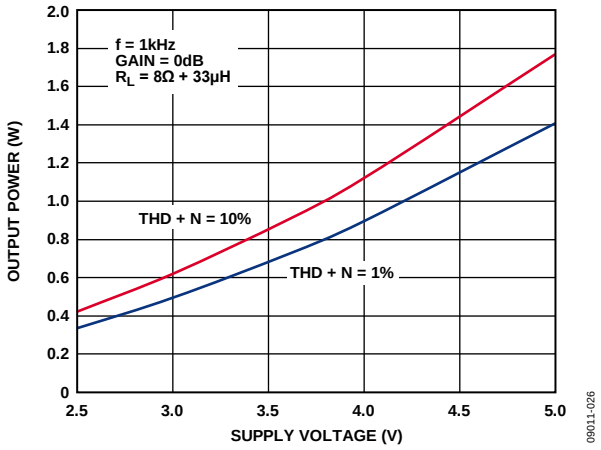

Figure 21. Maximum Output Power vs. Supply Voltage, R_L = 8 Ω, Gain = 0 dB

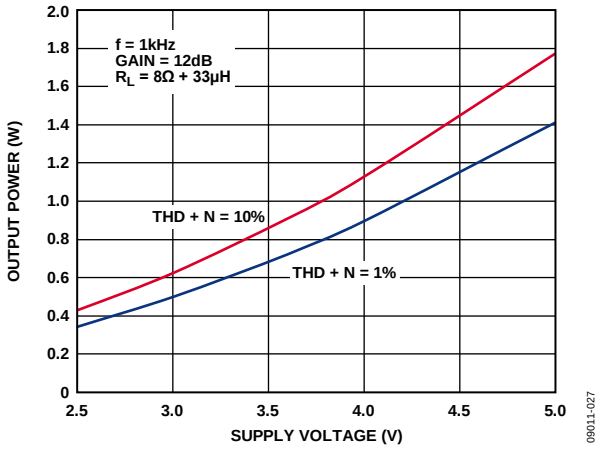

Figure 24. Maximum Output Power vs. Supply Voltage, R_L = 8 Ω, Gain = 12 dB

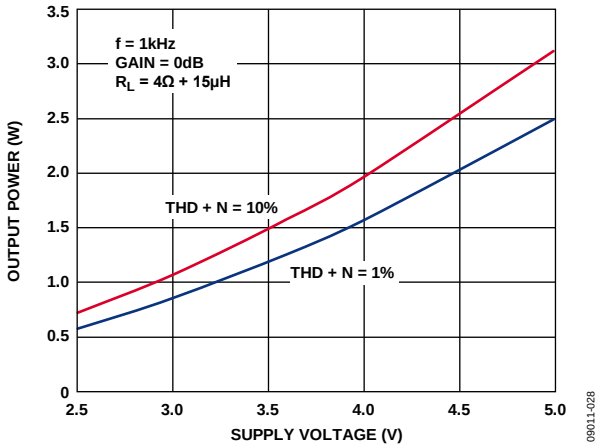

Figure 22. Maximum Output Power vs. Supply Voltage, R_L = 4 Ω, Gain = 0 dB

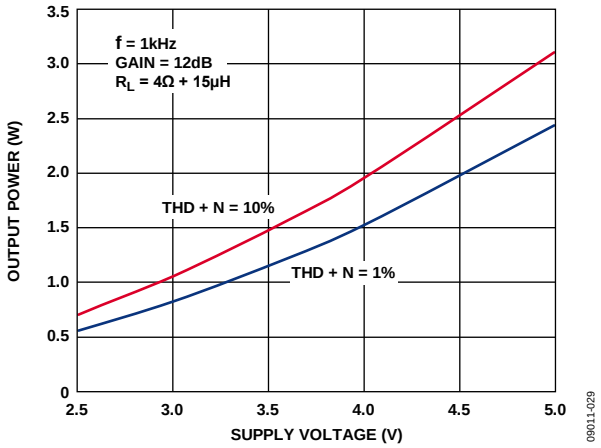

Figure 25. Maximum Output Power vs. Supply Voltage, R_L = 4 Ω, Gain = 12 dB

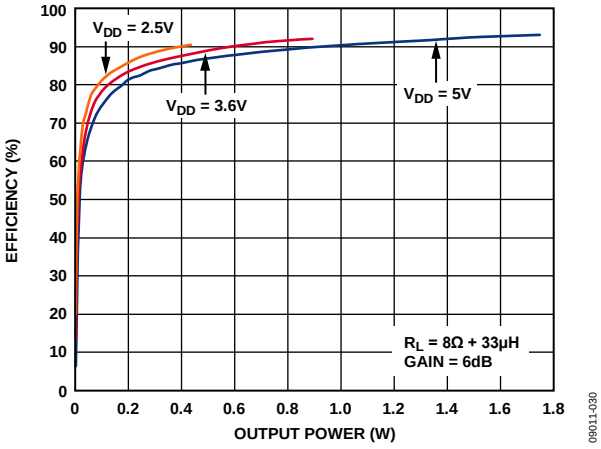

Figure 23. Efficiency vs. Output Power into 8 Ω, Gain = 6 dB

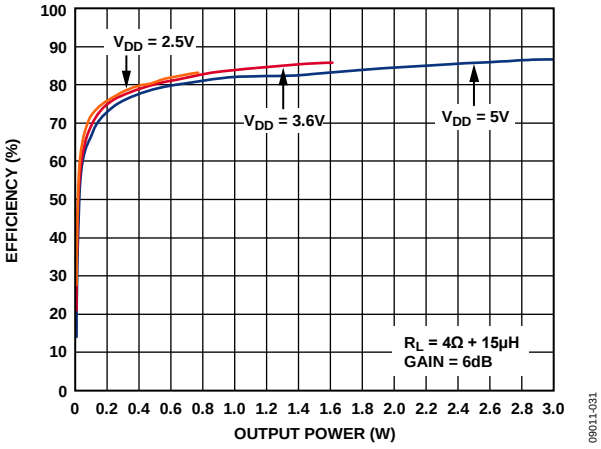

Figure 26. Efficiency vs. Output Power into 4 Ω, Gain = 6 dB

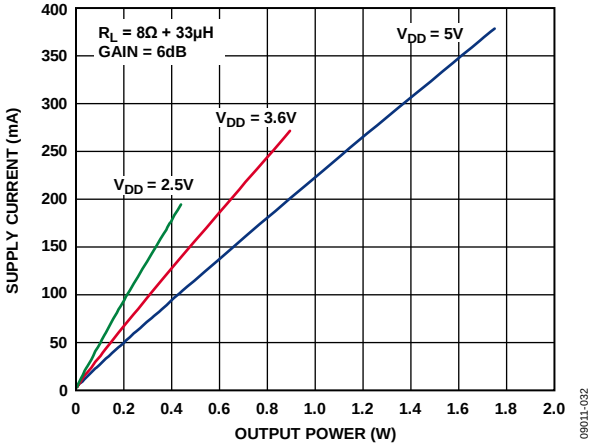

Figure 27. Supply Current vs. Output Power into 8 Ω, Gain = 6 dB

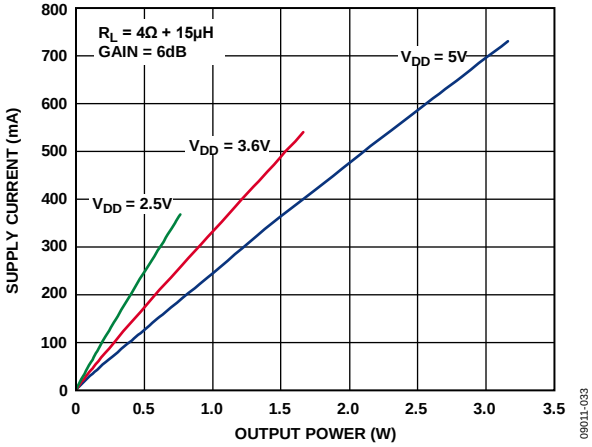

Figure 30. Supply Current vs. Output Power into 4 Ω, Gain = 6 dB

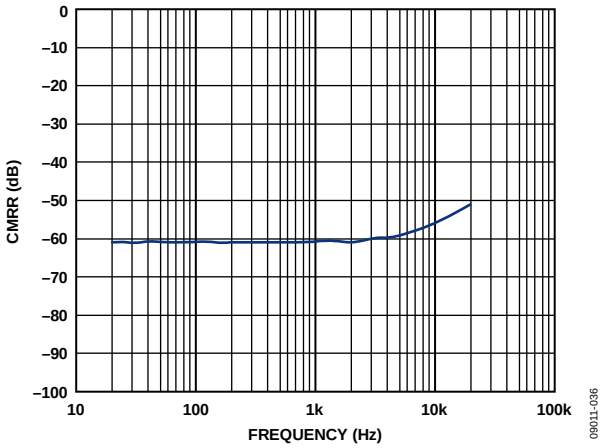

Figure 28. Common-Mode Rejection Ratio (CMRR) vs. Frequency

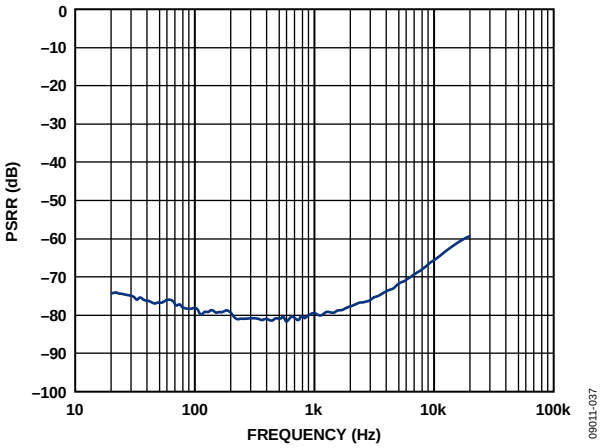

Figure 31. Power Supply Rejection Ratio (PSRR) vs. Frequency

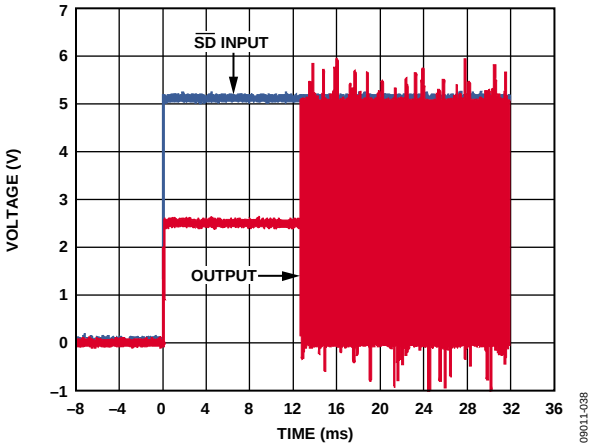

Figure 29. Turn-On Response

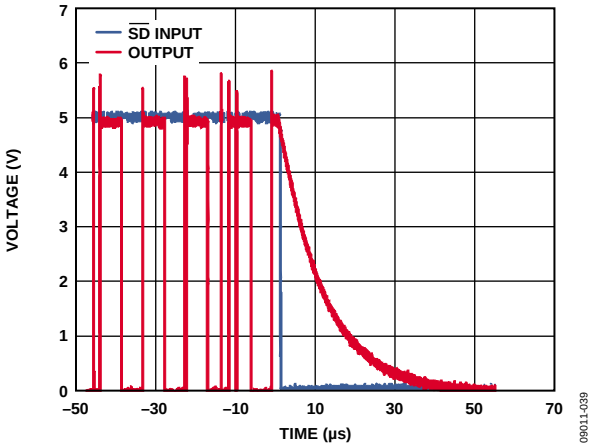

Figure 32. Turn-Off Response

TYPICAL APPLICATION CIRCUITS

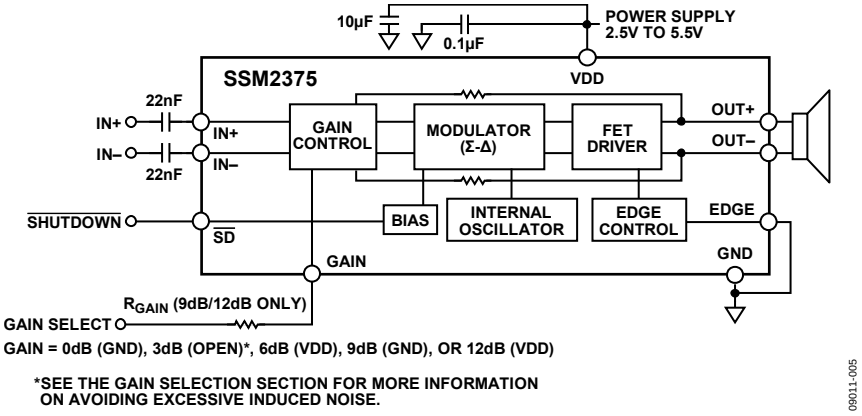

Figure 33. Monaural Differential Input Configuration

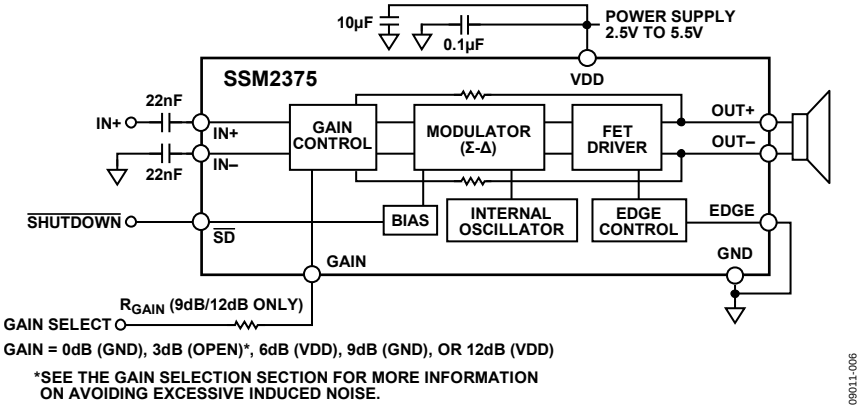

Figure 34. Monaural Single-Ended Input Configuration

THEORY OF OPERATION

OVERVIEW

The SSM2375 mono Class-D audio amplifier features a filterless modulation scheme that greatly reduces the external component count, conserving board space and, thus, reducing systems cost. The SSM2375 does not require an output filter but, instead, relies on the inherent inductance of the speaker coil and the natural filtering of the speaker and human ear to fully recover the audio component of the switching output.

Most Class-D amplifiers use some variation of pulse-width modulation (PWM), but the SSM2375 uses Σ-Δ modulation to determine the switching pattern of the output devices, resulting in a number of important benefits.

- Σ-Δ modulators do not produce a sharp peak with many harmonics in the AM frequency band, as pulse-width modulators often do.
- Σ-Δ modulation provides the benefits of reducing the amplitude of spectral components at high frequencies, that is, reducing EMI emissions that might otherwise be radiated by speakers and long cable traces.
- Due to the inherent spread-spectrum nature of Σ-Δ modulation, the need for oscillator synchronization is eliminated for designs that incorporate multiple SSM2375 amplifiers.

The SSM2375 also integrates overcurrent and overtemperature protection.

GAIN SELECTION

The preset gain of the SSM2375 can be set from 0 dB to 12 dB in 3 dB steps with one external resistor (optional). The external resistor is used to select the 9 dB or 12 dB gain setting, as shown in Table 5.

To avoid excessive induced noise at high output power, observe caution under the following conditions: GAIN pin is configured to the 3 dB gain setting (open) and using both low impedance (less than 3 Ω + 10 μH) loading and configured for low emissions mode (EDGE = VDD). To safeguard against the potential induced noise at high power levels in this configuration, connect a capacitor from GAIN to GND with a value ranging from 2.2 μF to 4.7 μF. Alternatively, apply a fixed voltage of VDD/2 to the GAIN pin to stabilize the gain setting operation under the low impedance/high power condition stated above.

Table 5. Gain Function Descriptions

Gain Setting (dB)	GAIN Pin Configuration
12	Tie to VDD through 47 kΩ resistor
9	Tie to GND through 47 kΩ resistor
6	Tie to VDD
3[1]	Open
0	Tie to GND

[1] See the Gain Selection section for more information on avoiding excessive induced noise.

POP-AND-CLICK SUPPRESSION

Voltage transients at the output of audio amplifiers can occur when shutdown is activated or deactivated. Voltage transients as low as 10 mV can be heard as an audio pop in a low sensitivity handset speaker. Clicks and pops can also be classified as undesirable audible transients generated by the amplifier system and, therefore, as not coming from the system input signal.

The SSM2375 has a pop-and-click suppression architecture that reduces these output transients, resulting in noiseless activation and deactivation from the $\overline{SD}$ control pin while operating in a typical audio configuration.

EMI NOISE

The SSM2375 uses a proprietary modulation and spread-spectrum technology to minimize EMI emissions from the device. For applications that have difficulty passing FCC Class B emission tests, the SSM2375 includes a modulation select pin (ultralow EMI emissions mode) that significantly reduces the radiated emissions at the Class-D outputs, particularly above 100 MHz.

EMI emission tests on the SSM2375 were performed in a certified FCC Class B laboratory in low emissions mode (EDGE = VDD). With a pink noise source, an 8 Ω speaker load, and a 5 V supply, the SSM2375 was able to pass FCC Class B limits with 50 cm, unshielded twisted pair speaker cable. Note that reducing the power supply voltage greatly reduces radiated emissions.

OUTPUT MODULATION DESCRIPTION

The SSM2375 uses three-level, Σ-Δ output modulation. Each output can swing from GND to V_{DD} and vice versa. Ideally, when no input signal is present, the output differential voltage is 0 V because there is no need to generate a pulse. In a real-world situation, there are always noise sources present.

Due to this constant presence of noise, a differential pulse is generated, when required, in response to this stimulus. A small amount of current flows into the inductive load when the differential pulse is generated.

Most of the time, however, the output differential voltage is 0 V, due to the Analog Devices, Inc., three-level, Σ-Δ output modulation. This feature ensures that the current flowing through the inductive load is small.

When the user wants to send an input signal, an output pulse is generated to follow the input voltage. The differential pulse density is increased by raising the input signal level. Figure 35 depicts three-level, Σ-Δ output modulation with and without input stimulus.

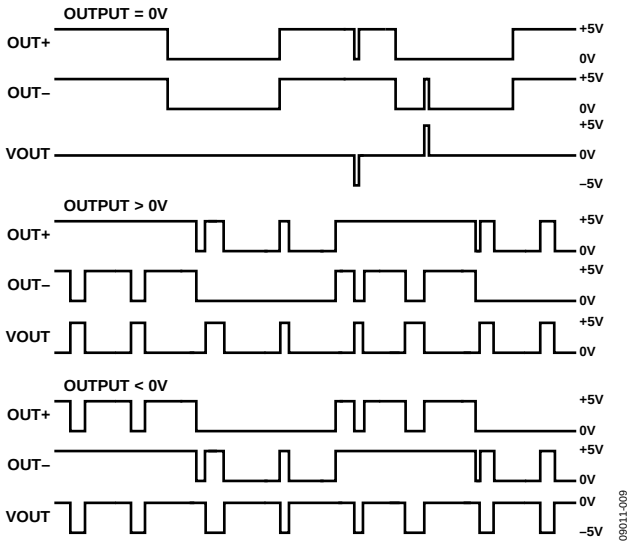

Figure 35. Three-Level, Σ-Δ Output Modulation With and Without Input Stimulus

LAYOUT

As output power increases, care must be taken to lay out PCB traces and wires properly among the amplifier, load, and power supply. A good practice is to use short, wide PCB tracks to decrease voltage drops and minimize inductance. The PCB layout engineer must avoid ground loops where possible to minimize common-mode current associated with separate paths to ground. Ensure that track widths are at least 200 mil for every inch of track length for lowest DCR, and use 1 oz or 2 oz copper PCB traces to further reduce IR drops and inductance. A poor layout increases voltage drops, consequently affecting efficiency. Use large traces for the power supply inputs and amplifier outputs to minimize losses due to parasitic trace resistance.

Proper grounding guidelines help to improve audio performance, minimize crosstalk between channels, and prevent switching noise from coupling into the audio signal. To maintain high output swing and high peak output power, the PCB traces that connect the output pins to the load, as well as the PCB traces to the supply pins, should be as wide as possible to maintain the minimum trace resistances. It is also recommended that a large ground plane be used for minimum impedances.

In addition, good PCB layout isolates critical analog paths from sources of high interference. High frequency circuits (analog and digital) should be separated from low frequency circuits.

Properly designed multilayer PCBs can reduce EMI emissions and increase immunity to the RF field by a factor of 10 or more, compared with double-sided boards. A multilayer board allows a complete layer to be used for the ground plane, whereas the ground plane side of a double-sided board is often disrupted by signal crossover.

INPUT CAPACITOR SELECTION

The SSM2375 does not require input coupling capacitors if the input signal is biased from 1.0 V to V_{DD} − 1.0 V. Input capacitors are required if the input signal is not biased within this recommended input dc common-mode voltage range, if high-pass filtering is needed, or if a single-ended source is used. If high-pass filtering is needed at the input, the input capacitor and the input resistor of the SSM2375 form a high-pass filter whose corner frequency is determined by the following equation:

$$f_C = 1/(2\pi \times R_{IN} \times C_{IN})$$

The input capacitor can significantly affect the performance of the circuit. Not using input capacitors degrades both the output offset of the amplifier and the dc PSRR performance.

POWER SUPPLY DECOUPLING

To ensure high efficiency, low total harmonic distortion (THD), and high PSRR, proper power supply decoupling is necessary. Noise transients on the power supply lines are short-duration voltage spikes. These spikes can contain frequency components that extend into the hundreds of megahertz. The power supply input must be decoupled with a good quality, low ESL, low ESR capacitor, with a minimum value of 4.7 μF. This capacitor bypasses low frequency noises to the ground plane. For high frequency transient noises, use a 0.1 μF capacitor as close as possible to the VDD pin of the device. Placing the decoupling capacitors as close as possible to the SSM2375 helps to maintain efficient performance.

OUTLINE DIMENSIONS

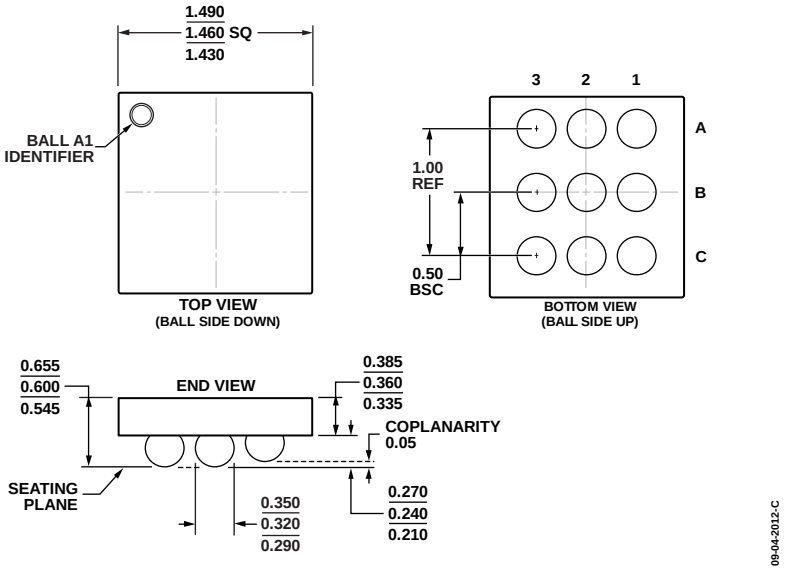

Figure 36. 9-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-9-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option[2]
SSM2375CBZ-REEL	−40°C to +85°C	9-Ball Wafer Level Chip Scale Package [WLCSP]	CB-9-2
SSM2375CBZ-REEL7	−40°C to +85°C	9-Ball Wafer Level Chip Scale Package [WLCSP]	CB-9-2
EVAL-SSM2375Z		Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] This package option is halide free.

NOTES

D09011-0-4/13(A)

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