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REVISION HISTORY

11/07—Revision 0: Initial Version

SPECIFICATIONS

Table 1.

Parameter	Conditions	Temp	Test Level[1]	Min	Typ	Max	Unit
DIGITAL INPUTS							
Input Voltage							
High (V_{IH})		Full	VI	1.4		3.5	V
Low (V_{IL})		Full	VI			0.7	V
Input Capacitance		25°C	V		3		pF
DIGITAL OUTPUTS							
Output Voltage							
High (V_{OH})		Full	VI	V_{DD} − 0.1			V
Low (V_{OL})		Full	VI			0.4	V
THERMAL CHARACTERISTICS							
Thermal Resistance							
Junction-to-Case (θ_{JC})			V		15.2		°C/W
Junction-to-Ambient (θ_{JA})			V		59		°C/W
Ambient Temperature		Full	V	−10	+25	+85	°C
DC SPECIFICATIONS							
Input Leakage Current (I_{IL})		25°C	VI	−10		+10	µA
Input Clamp Voltage	−16 mA	25°C	V		−0.8		V
	+16 mA	25°C	V		+0.8		V
Differential High Level Output Voltage			V		AV_{CC}		V
Differential Output Short-Circuit Current			IV			10	µA
POWER SUPPLY							
V_{DD} (All) Supply Voltage		Full	IV	1.71	1.8	1.89	V
V_{DD} Supply Voltage Noise		Full	V			50	mV p-p
Power-Down Current	With active video applied, 165 MHz, typical random pattern	25°C	IV		9		mA
Transmitter Supply Current	With active video applied, 165 MHz, typical random pattern	25°C	IV		240	280	mA
Transmitter Total Power		Full	VI		432	504	mW
AC SPECIFICATIONS							
CLK Frequency		25°C	IV	13.5		165	MHz
TMDS Output CLK Duty Cycle		25°C	IV	48		52	%
Worst Case CLK Input Jitter		Full	IV			2	ns
Input Data Setup Time		Full	IV	1			ns
Input Data Hold Time		Full	IV	1			ns
TMDS Differential Swing			VI	800	1000	1200	mV
V_{SYNC} and H_{SYNC}							
Delay from DE Falling Edge			VI		1		UI[2]
Delay to DE Rising Edge			VI		1		UI[2]
DE Time							
High Time		25°C	VI			8191	UI[2]
Low Time		25°C	VI		138		UI[2]
Differential Output Swing							
Low-to-High Transition Time		25°C	VII	75		490	ps
High-to-Low Transition Time		25°C	VII	75		490	ps

Parameter	Conditions	Temp	Test Level[1]	Min	Typ	Max	Unit
AUDIO AC TIMING							
Sample Rate	I^2S and S/PDIF	Full	IV	32		192	kHz
I^2S Bit Width		Full	IV	16		24	Bits
I^2S Cycle Time		25°C	IV			1	UI[2]
I^2S Setup Time		25°C	IV		15		ns
I^2S Hold Time		25°C	IV		0		ns
Audio Pipeline Delay		25°C	IV		75		µs

[1] See Explanation of Test Levels section.
[2] UI = unit interval.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Digital Inputs	5 V to 0.0 V
Digital Output Current	20 mA
Operating Temperature Range	−10°C to +85°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
Maximum Case Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

EXPLANATION OF TEST LEVELS

I. 100% production tested.

II. 100% production tested at 25°C and sample tested at specified temperatures.

III. Sample tested only.

IV. Parameter is guaranteed by design and characterization testing.

V. Parameter is a typical value only.

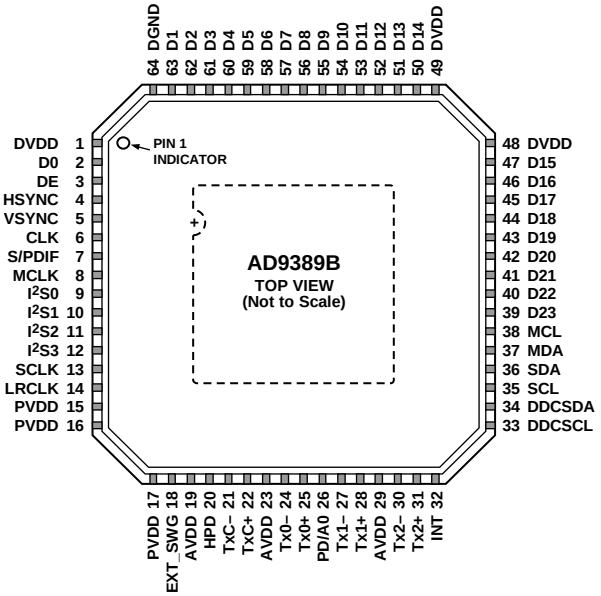
VI. 100% production tested at 25°C; guaranteed by design and characterization testing.

VII. Limits defined by HDMI specification; guaranteed by design and characterization testing.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. GND PADDLE ON BOTTOM OF PACKAGE.

Figure 2. 64-Lead LFCSP Pin Configuration (Top View)

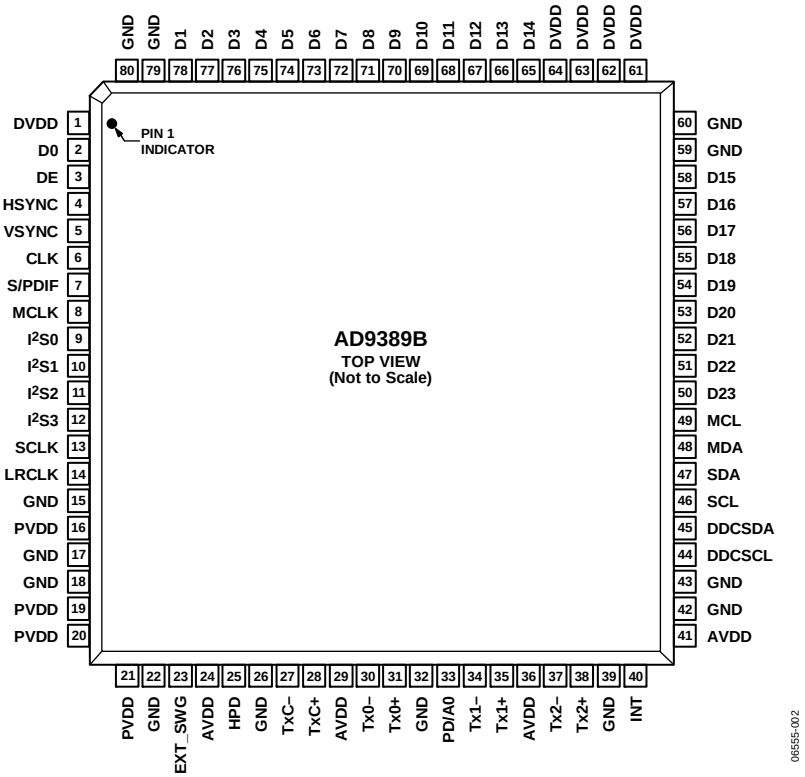


Figure 3. 80-Lead LQFP Pin Configuration (Top View)

Table 3. Pin Function Descriptions

Pin No.				
LFCSP	**LQFP**	**Mnemonic**	**Type[1]**	**Description**
2, 39 to 47, 50 to 63	2, 50 to 58, 65 to 78	D[23:0]	I	Video Data Input. Digital input in RGB or YCbCr format. Supports CMOS logic levels from 1.8 V to 3.3 V.
6	6	CLK	I	Video Clock Input. Supports CMOS logic levels from 1.8 V to 3.3 V.
3	3	DE	I	Data Enable Bit for Digital Video. Supports CMOS logic levels from 1.8 V to 3.3 V.
4	4	HSYNC	I	Horizontal Sync Input. Supports CMOS logic levels from 1.8 V to 3.3 V.
5	5	VSYNC	I	Vertical Sync Input. Supports CMOS logic levels from 1.8 V to 3.3 V.
18	23	EXT_SWG	I	Set Internal Reference Currents. Place 887 Ω resistor (1% tolerance) between this pin and ground.
20	25	HPD	I	Hot Plug Detect Signal. This indicates to the interface whether the receiver is connected. 1.8 V to 5.0 V CMOS logic levels.
7	7	S/PDIF	I	S/PDIF (Sony/Philips Digital Interface) Audio Input. This is the audio input from a Sony/Philips digital interface. Supports CMOS logic levels from 1.8 V to 3.3 V.
8	8	MCLK	I	Audio Reference Clock. $128 \times N \times f_S$ with N = 1, 2, 3, or 4. Set to 128 × sampling frequency (f_S), $256 \times f_S$, $384 \times f_S$, or $512 \times f_S$. 1.8 V to 3.3 V CMOS logic levels.
9 to 12	9 to 12	I^2S[3:0]	I	I^2S Audio Data Inputs. These represent the eight channels of audio (two per input) available through I^2S. Supports CMOS logic levels from 1.8 V to 3.3 V.
13	13	SCLK	I	I^2S Audio Clock. Supports CMOS logic levels from 1.8 V to 3.3 V.
14	14	LRCLK	I	Left/Right Channel Selection. Supports CMOS logic levels from 1.8 V to 3.3 V.
26[2]	33[2]	PD/A0	I	Power-Down Control and I^2C Address Selection. The I^2C address and the PD polarity are set by the PD/A0 pin state when the supplies are applied to the AD9389B. 1.8 V to 3.3 V CMOS logic levels.
21, 22	27, 28	TxC−/TxC+	O	Differential Clock Output. Differential clock output at pixel clock rate; TMDS logic level.
30, 31	37, 38	Tx2−/Tx2+	O	Differential Output Channel 2. Differential output of the red data at 10× the pixel clock rate; TMDS logic level.
27, 28	34, 35	Tx1−/Tx1+	O	Differential Output Channel 1. Differential output of the green data at 10× the pixel clock rate; TMDS logic level.
24, 25	30, 31	Tx0−/Tx0+	O	Differential Output Channel 0. Differential output of the blue data at 10× the pixel clock rate; TMDS logic level.
32	40	INT	O	Interrupt. Open drain. A 2 kΩ pull-up resistor to the microcontroller I/O supply is recommended. Active Low.
19, 23, 29	24, 29, 36, 41	AVDD	P	1.8 V Power Supply for TMDS Outputs.
1, 48, 49	1, 61 to 64	DVDD	P	1.8 V Power Supply for Digital and I/O Power Supply. These pins supply power to the digital logic and I/Os. They should be filtered and as quiet as possible.
15, 16, 17	16, 19 to 21	PVDD	P	1.8 V PLL Power Supply. The most sensitive portion of the AD9389B is the clock generation circuitry. These pins provide power to the clock PLL. Provide quiet, noise-free power to these pins.
N/A	15, 17, 18, 22, 26, 32, 39, 42, 43, 59, 60, 79, 80	GND	P	Ground. The ground return for all circuitry on-chip. It is recommended that the AD9389B be assembled on a single, solid ground plane with careful attention given to ground current paths.
64, paddle on bottom side	N/A	DGND		Ground. The ground return for all circuitry on-chip. It is recommended that the AD9389B be assembled on a single, solid ground plane with careful attention given to ground current paths.
36	47	SDA	C[3]	Serial Port Data I/O. This pin serves as the serial port data I/O slave for register access. Supports CMOS logic levels from 1.8 V to 3.3 V.
35	46	SCL	C[3]	Serial Port Data Clock. This pin serves as the serial port data clock slave for register access. Supports CMOS logic levels from 1.8 V to 3.3 V.
37	48	MDA	C[3]	Serial Port Data I/O Master to HDCP Key EEPROM. Supports CMOS logic levels from 1.8 V to 3.3 V.
38	49	MCL	C[3]	Serial Port Data Clock Master to HDCP Key EEPROM. Supports CMOS logic levels from 1.8 V to 3.3 V.

Pin No.		Mnemonic	Type[1]	Description
LFCSP	LQFP			
34	45	DDCSDA	C[3]	Serial Port Data I/O to Receiver. This pin serves as the master to the DDC bus. 5 V CMOS logic level.
33	44	DDCSCL	C[3]	Serial Port Data Clock to Receiver. This pin serves as the master clock for the DDC bus. 5 V CMOS logic level.

[1] I = input, O = output, P = power supply, C = control.
[2] Pin 26 (LFCSP) and Pin 33 (LQFP) are dual function pins: I^2C selection and power-down control. The I^2C selection function occurs at power-up; the power-down control function occurs whenever the state of the pin is changed from its original state at power-up.
[3] For a full description of the 2-wire serial interface and its functionality, obtain documentation by contacting NDA at flatpanel_apps@analog.com.

APPLICATIONS INFORMATION

DESIGN RESOURCES

Analog Devices, Inc. evaluation kits, reference design schematics, and other support documentation are available under the nondisclosure agreement (NDA) from flatpanel_apps@analog.com.

Other resources include:

EIA/CEA-861B which describes audio and video infoframes as well as the E-EDID structure for HDMI. It is available from the Consumer Electronics Association (CEA).

The *HDMI v. 1.3*, a defining document for HDMI 1.3, and the *HDMI Compliance Test Specification Version 1.3* are available from HDMI Licensing, LLC.

The *HDCP Specification v. 1.2* is the defining document for HDCP 1.2 available from Digital Content Protection, LLC.

DOCUMENT CONVENTIONS

In this data sheet, data is represented using the conventions described in Table 4.

Table 4. Document Conventions

Data Type	Format
0xNN	Hexadecimal (Base 16) numbers are represented using the C language notation, preceded by 0x.
0bNN	Binary (Base 2) numbers are represented using the C language notation, preceded by 0b.
NN	Decimal (Base 10) numbers are represented using no additional prefixes or suffixes.
Bit	Bits are numbered in little endian format, that is, the least significant bit of a byte or word is referred to as Bit 0.

PCB LAYOUT RECOMMENDATIONS

The AD9389B is a high precision, high speed analog device. As such, to obtain the maximum performance from the part, it is important to have a well laid out board.

POWER SUPPLY BYPASSING

It is recommended to bypass each power supply pin with a 0.1 μF capacitor. The exception is when two or more supply pins are adjacent to each other. For these groupings of powers/grounds, it is necessary to have only one bypass capacitor. The fundamental idea is to have a bypass capacitor within about 0.5 cm of each power pin. Also, avoid placing the capacitor on the opposite side of the PCB from the AD9389B because that interposes resistive vias in the path.

The bypass capacitors should be physically located between the power plane and the power pin. Current should flow from the power plane to the capacitor to the power pin. Do not make a power connection between the capacitor and the power pin. Placing a via underneath the capacitor pads, down to the power plane, is generally the best approach.

It is particularly important to maintain low noise and good stability of PVDD (the PLL supply). Abrupt changes in PVDD can result in similarly abrupt changes in sampling clock phase and frequency. This can be avoided by careful attention to regulation, filtering, and bypassing. It is best practice to provide separate regulated supplies for each of the analog circuitry groups (AVDD and PVDD).

It is also recommended to use a single ground plane for the entire board. Experience has repeatedly shown that the noise performance is the same or better with a single ground plane. Using multiple ground planes can be detrimental because each separate ground plane is smaller, and long ground loops can result.

DIGITAL INPUTS

Video and Audio Data Input Signals

The digital inputs on the AD9389B are designed to work with signals ranging from 1.8 V to 3.3 V logic level. Therefore, no extra components need to be added when using 3.3 V logic. Any noise that gets onto the clock input (labeled CLK) trace adds jitter to the system. Therefore, minimize the video clock input (CLK, Pin 6) trace length and do not run any digital or other high frequency traces near it. Make sure to match the length of the input data signals to optimize data capture, especially for high frequency modes such as 1080p and UXGA and double data rate input formats.

Other Input Signals

The HPD must be connected to the HDMI connector. A 10 kΩ pull-down resistor to ground is also recommended.

The PD/A0 input pin can be connected to GND or supply (through a resistor or a control signal). The device address and power-down polarity are set by the state of the PD/A0 pin when the AD9389B supplies are applied/enabled. For example, if the PD/A0 pin is low (when the supplies are turned on), then the device address is 0x72 and the power-down is active high. If the PD/A0 pin is high (when the supplies are turned on), the device address is 0x7A and the power-down is active low.

Connect the SCL and SDA pins to the I^2C master. A pull-up resistor of 2 kΩ to 1.8 V or 3.3 V is recommended.

EXTERNAL SWING RESISTOR

The external swing resistor must be connected directly to the EXT_SWG pin and ground. The external swing resistor must have a value of 887 Ω (±1% tolerance). Avoid running any high speed ac or noisy signals next to, or close to, the EXT_SWG pin.

OUTPUT SIGNALS

TMDS Output Signals

The AD9389B has three TMDS data channels (0, 1, and 2) that output signals up to 800 MHz as well as the TMDS output data clock. To minimize the channel-to-channel skew, make the trace length of these signals the same. Additionally, these traces need to have a 50 Ω characteristic impedance and need to be routed as 100 Ω differential pairs. Best practice recommends routing these lines on the top PCB layer, avoiding the use of vias.

Other Output Signals (non TMDS)

DDCSCL and DDCSDA

The DDCSCL and DDCSDA outputs need to have a minimum amount of capacitance loading to ensure the best signal integrity. The DDCSCL and DDCSDA capacitance loading must be less than 50 pF to meet the HDMI compliance specification. The DDCSCL and DDCSDA must be connected to the HDMI connector and a pull-up resistor to 5 V is required. The pull-up resistor must have a value between 1.5 kΩ and 2 kΩ.

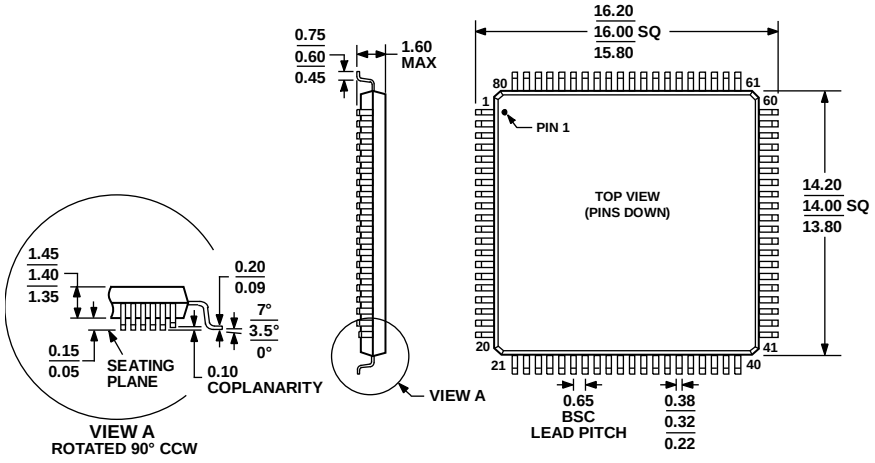
INT Pin

The INT pin is an output that should be connected to the microcontroller of the system. A pull-up resistor to 1.8 V or 3.3 V is required for proper operation—the recommended value is 2 kΩ.

MCL and MDA

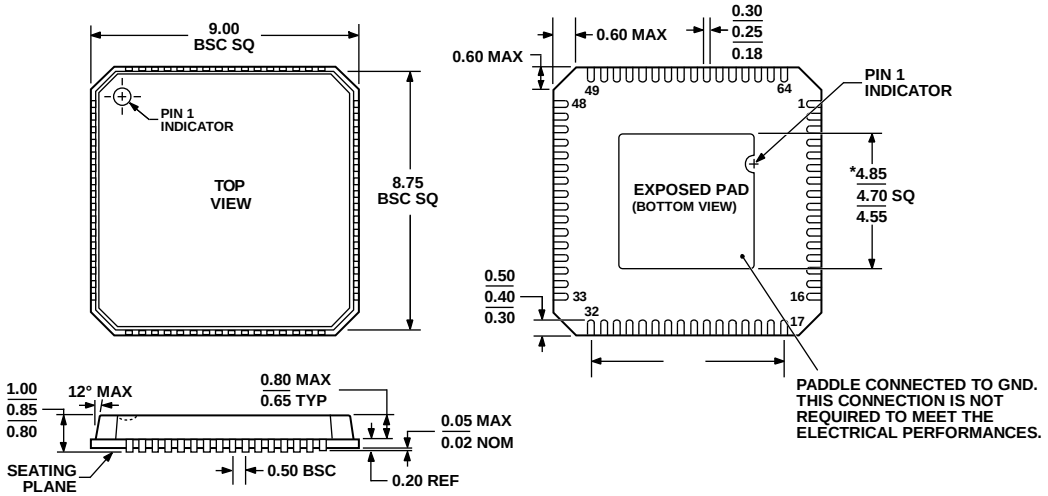
The MCL and MDA outputs should be connected to the EEPROM containing the HDCP key (if HDCP is implemented). Pull-up resistors of 2 kΩ are recommended.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-BEC

Figure 4. 80-Lead Low Profile Quad Flat Package [LQFP]
(ST-80-2)
Dimensions shown in millimeters



*COMPLIANT TO JEDEC STANDARDS MO-220-VMMD-4
EXCEPT FOR EXPOSED PAD DIMENSION

Figure 5. 64-Lead Lead Frame Chip Scale Package [LFCSP]
(CP-64-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9389BBCPZ-80[1]	−10°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP]	CP-64-1
AD9389BBCPZ-165[1]	−10°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP]	CP-64-1
AD9389BBSTZ-80[1]	−10°C to +85°C	80-Lead Low Profile Quad Flat Package [LQFP]	ST-80-2
AD9389BBSTZ-165[1]	−10°C to +85°C	80-Lead Low Profile Quad Flat Package [LQFP]	ST-80-2
AD9389B/PCBZ[1]		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

Purchase of licensed I²C components of Analog Devices or one of its sublicensed Associated Companies conveys a license for the purchaser under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

D06555-0-11/07(0)

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