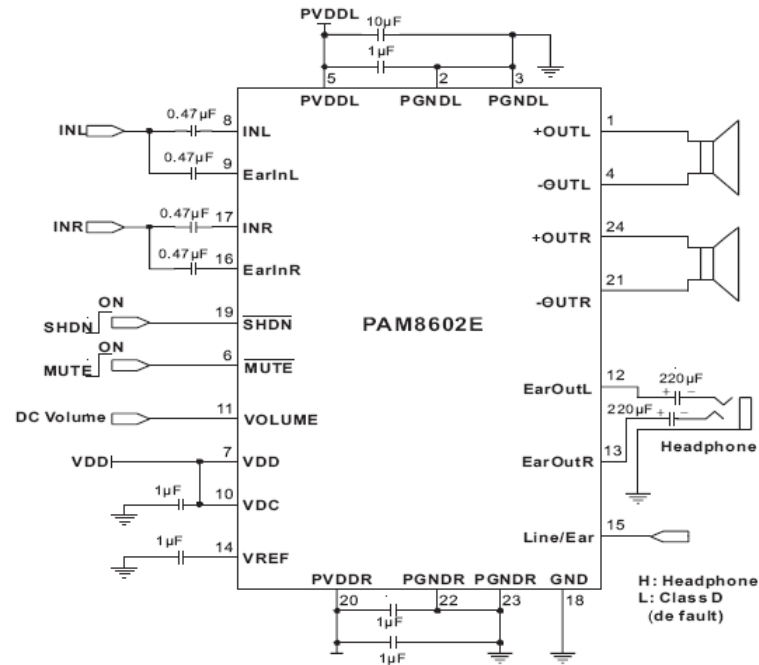


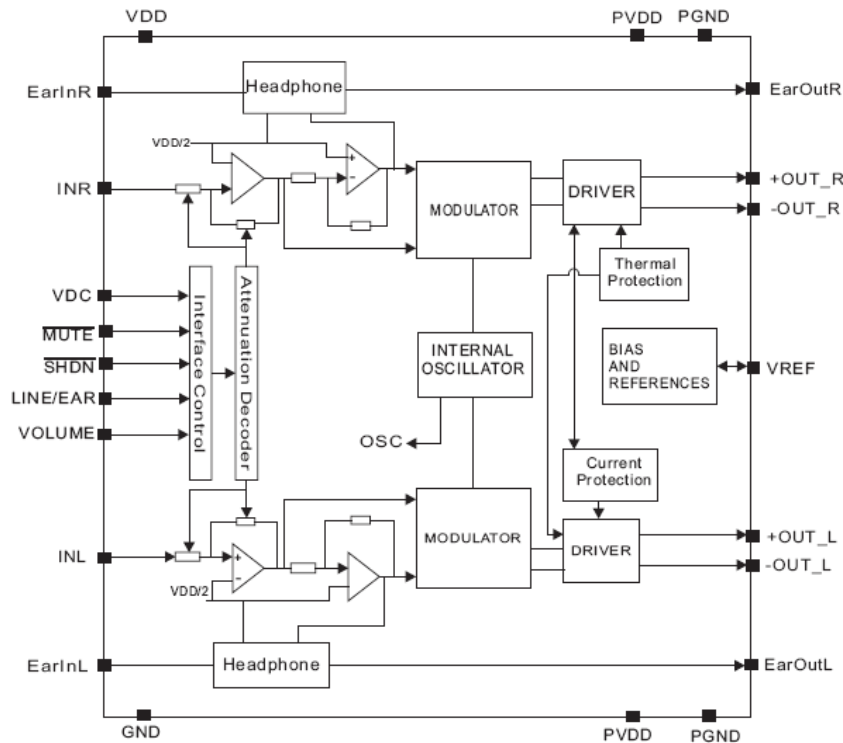
Typical Applications Circuit



Pin Descriptions

Pin Number	Pin Name	Function
1	+OUT_L	Left Channel Positive Output
2	PGNDL	Left Channel Power GND
3	PGNDL	Left Channel Positive GND
4	-OUT_L	Left Channel Negative Output
5	PVDDL	Left Channel Power Supply
6	$\overline{\text{MUTE}}$	Mute Control Input (active low)
7	VDD	Analog VDD
8	IN L	Left Channel Input
9	EAR IN L	Left Earphone Input
10	VDC	Analog Reference for Gain Control Section
11	VOLUME	DC Voltage Control to Set the Gain of Class-D
12	EAR OUT L	Left Earphone Output
13	EAR OUT R	Right Earphone Output
14	VREF	Internal Analog Reference, Connect a Bypass Capacitor from VREF to GND
15	LINE/EAR	Line/ Ear Detect
16	EAR IN R	Right Earphone Input
17	IN R	Right Channel Input
18	GND	Analog GND
19	$\overline{\text{SHDN}}$	Shutdown Control Input (active low)
20	PVDDR	Right Channel Power Supply
21	-OUT_R	Right Channel Negative Output
22	PGNDR	Right Channel Power GND
23	PGNDR	Right Channel Power GND
24	+OUT_R	Right Channel Positive Output

Functional Block Diagram



Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for prolonged time periods may affect device reliability. All voltages are with respect to ground.

Parameter	Rating	Unit
Supply Voltage	6.0	V
Input Voltage	-0.3 to V _{DD} +0.3	
Operation Junction Temperature	-40 to +125	°C
Storage Temperature	-65 to +150	
Soldering Temperature	300, 5 sec	

Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.)

Parameter	Rating	Unit
Supply Voltage Range	2.5 to 5.5	V
Ambient Operation Temperature Range	-20 to +85	°C
Junction Temperature Range	-20 to +125	°C

Thermal Information

Parameter	Package	Symbol	Max	Unit
Thermal Resistance (Junction to Ambient)	SSOP-24	θ _{JA}	96	°C/W
Thermal Resistance (Junction to Ambient)	SOP-24	θ _{JA}	79.2	°C/W

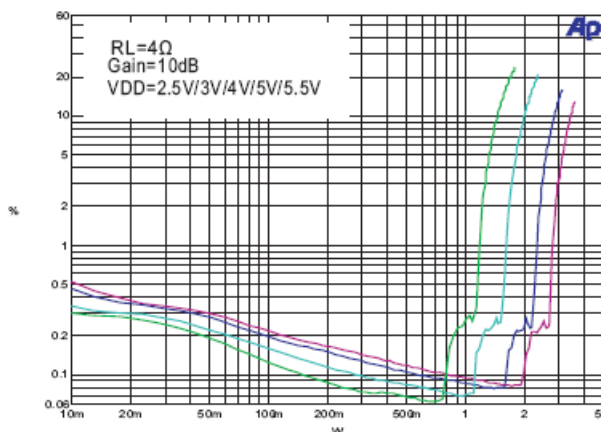
Electrical Characteristics (@T_A = +25°C, V_{DD} = 5V, Gain = Maximum, R_L = 8Ω, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Class D Stage						
Supply Voltage Range	V _{DD}		2.5		5.5	V
Quiescent Current	I _Q	No Load		10	15	mA
Output Offset Voltage	V _{OS}	No Load		10	50	mV
Drain-Source On-State Resistance	R _{DS(ON)}	I _{DS} = 0.5A	P MOSFET	0.35		Ω
			N MOSFET	0.25		
Output Power	P _O	THD+N = 10%, f = 1kHz	1.55	1.70		W
Total Harmonic Distortion Plus Noise	THD+N	P _O = 0.85W, f = 1KHz		0.08		%
Power Supply Ripple Rejection	PSRR	Input AC-GND, f = 1KHz, V _{PP} = 200mV		70		dB
Channel Separation	CS	P _O = 1W, f = 1KHz		-95		dB
Oscillator Frequency	f _{OSC}		200	250	300	kHz
Efficiency	η	P _O = 1.7W, f = 1 kHz	85	89		%
Noise	V _N	Input AC-GND	A-Weighting	220		μV
			No A-Weighting	350		
Signal Noise Ratio	SNR	f = 20 – 20kHz, THD = 1%		85		dB
Earphone Stage						
Quiescent Current	I _Q	No Load		4.5	7.5	mA
Output Offset Voltage	V _{OS}	No Load		2.5		V
Output Power	P _O	THD+N = 1%, R _L = 32Ω, f = 1KHz		60		mW
Total Harmonic Distortion Plus Noise	THD+N	R _L = 32Ω, P _O = 10mW, f = 1kHz		0.02		%
Power Supply Ripple Rejection	PSRR	Input AC-GND, f = 1kHz, V _{PP} = 200mV		75		dB
Channel Separation	CS	P _O = 1W, f = 1kHz		-85		dB
Noise	V _N	Input AC-GND	A-Weighting	70		μV
			No A-Weighting	40		
Signal Noise Ratio	SNR	f = 20 - 20kHz, THD = 1%		75		dB
Control Section						
Under Voltage Lock-Out	UVLO			2		
Mute Current	I _{MUTE}	V _{MUTE} = 0V		1	3	mA
Shutdown Current	I _{SHDN}	V _{SHDN} = 0V			1	μA
SHDN Input High	V _{SH}		1.2			
SHDN Input High	V _{SL}				0.5	
MUTE Input High	V _{MH}		1.2			
MUTE Input High	V _{ML}				0.5	
Over Temperature Protection	OTP			140		°C
Over Temperature Hysteresis	OTH			30		°C

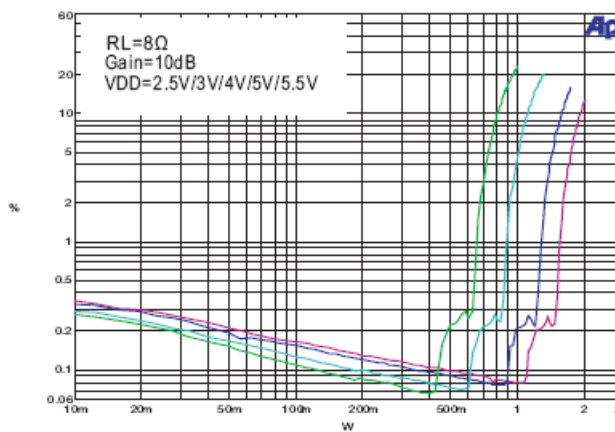
Typical Performance Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Class-D Output

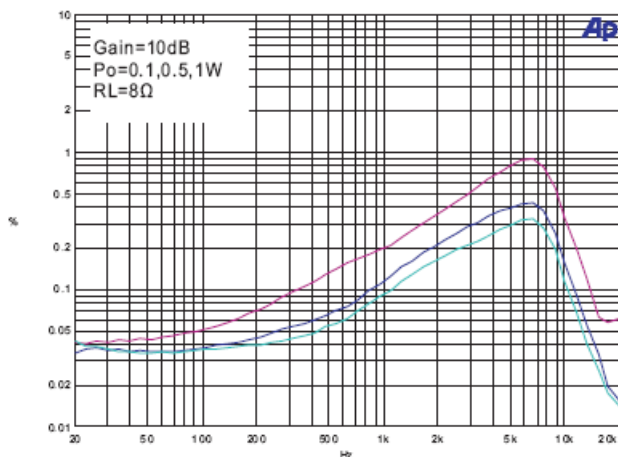
1. THD+N vs Output Power



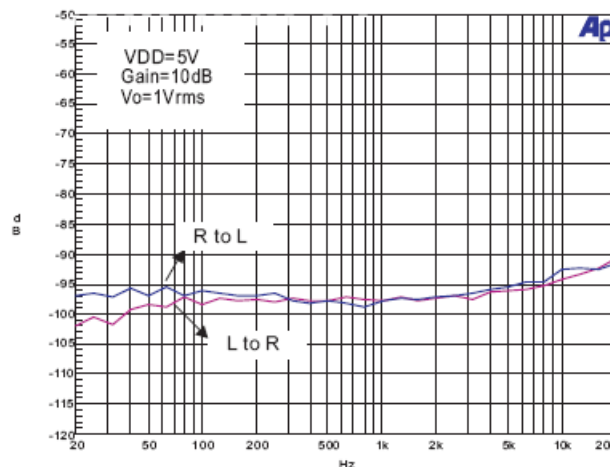
2. THD+N vs Output Power



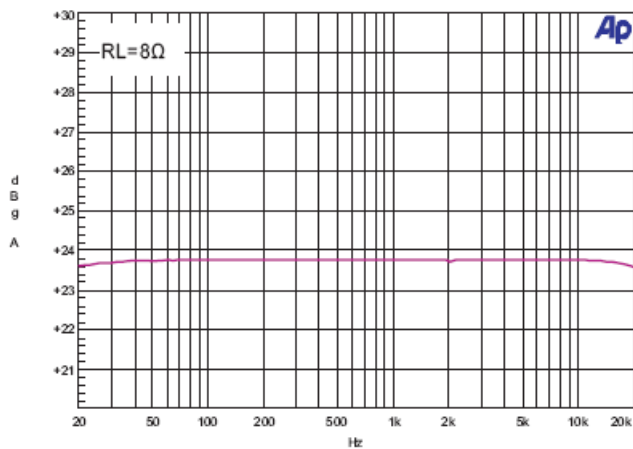
3. THD+N vs Frequency



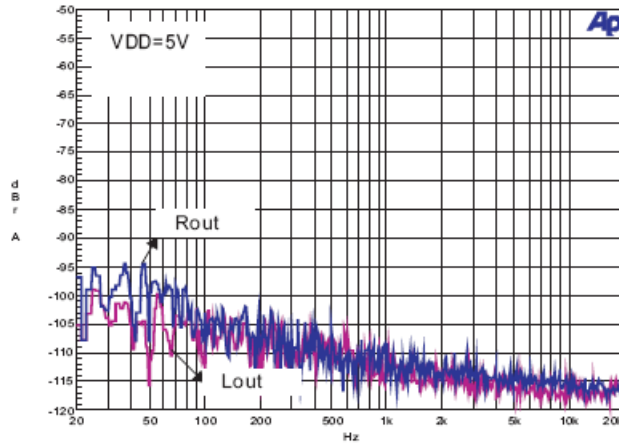
4. Crosstalk vs Frequency



5. Frequency Response

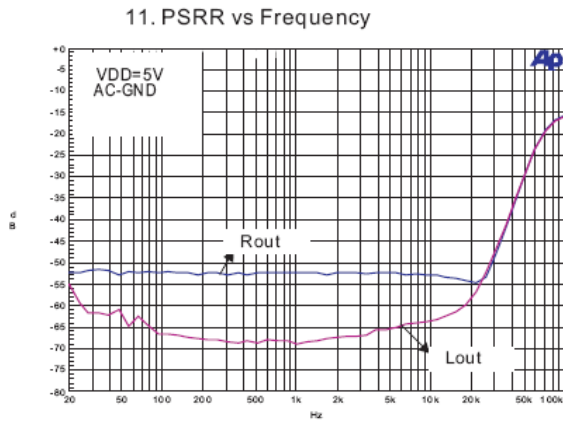
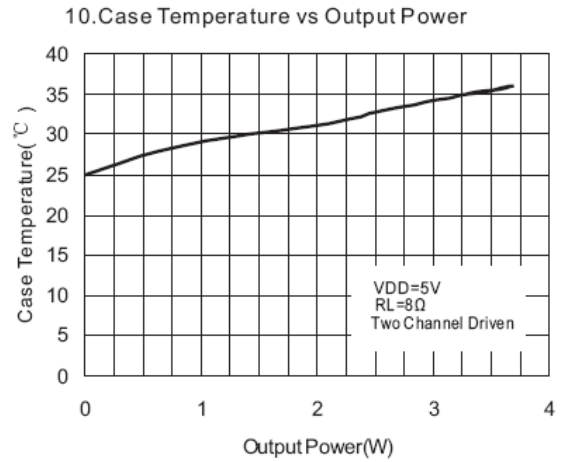
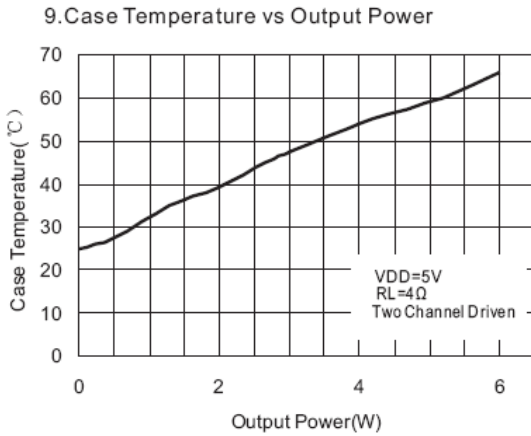
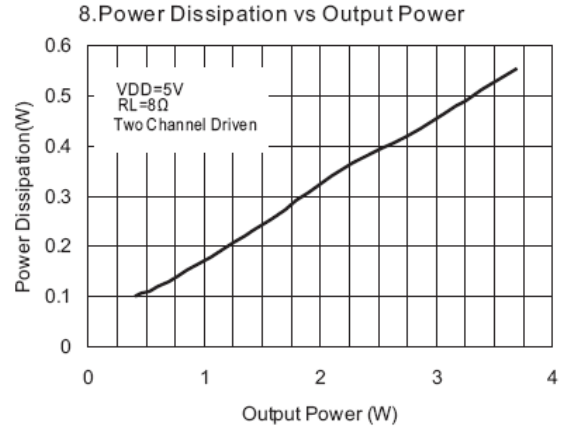
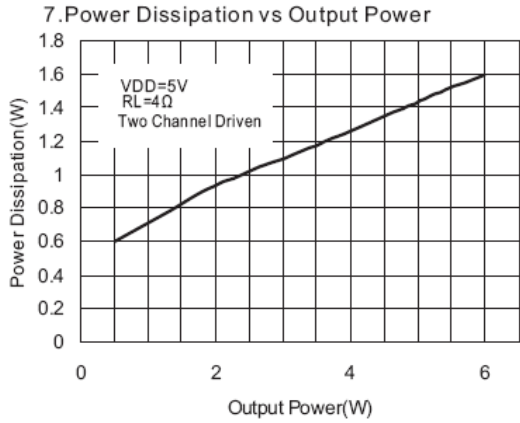


6. Noise Floor



Typical Performance Characteristics (cont.) (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

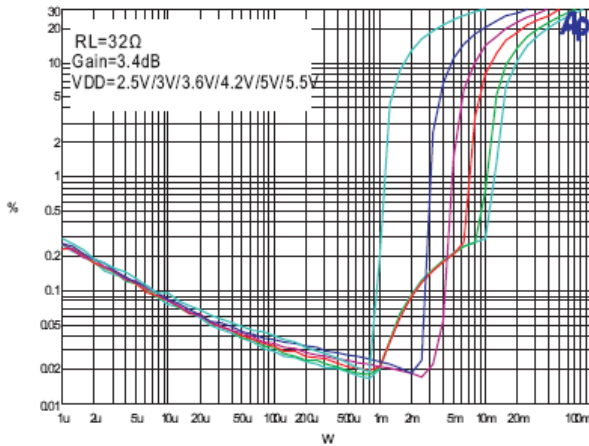
Class-D Output



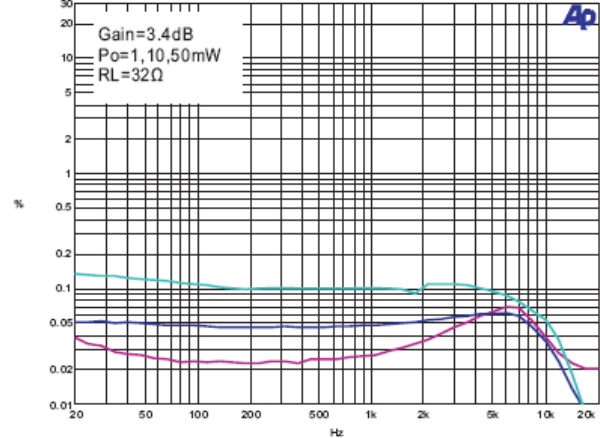
Typical Performance Characteristics (cont.) (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Earphone Output

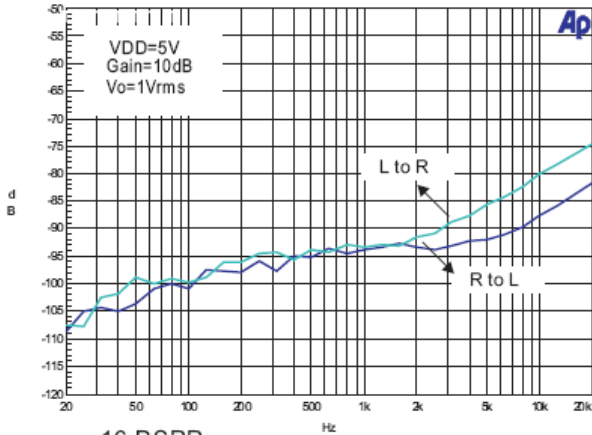
12. THD+N vs Output Power



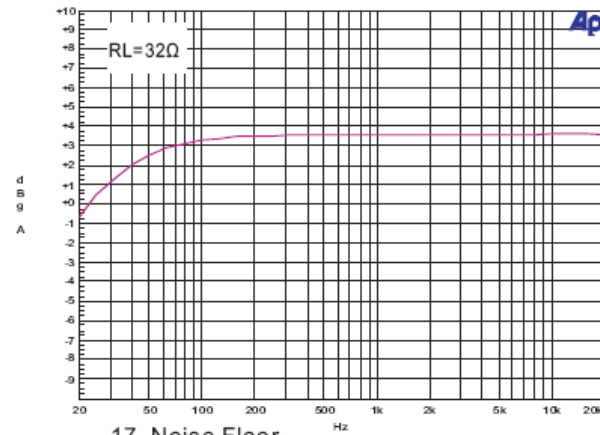
13. THD+N vs Frequency



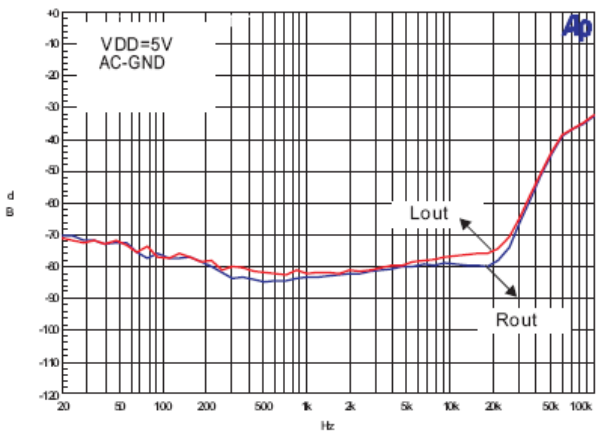
14. Crosstalk vs Frequency



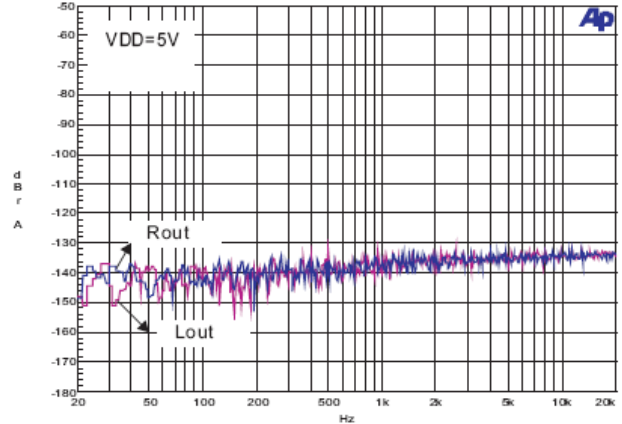
15. Frequency Response



16. PSRR

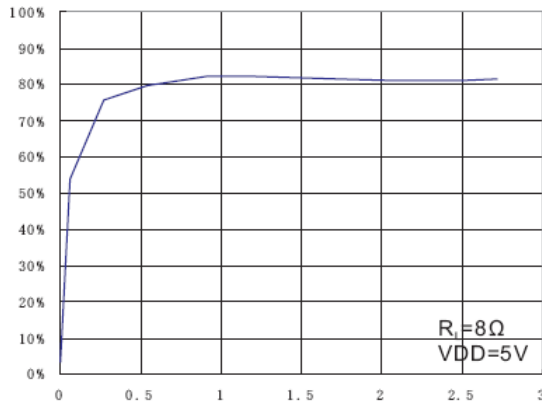


17. Noise Floor

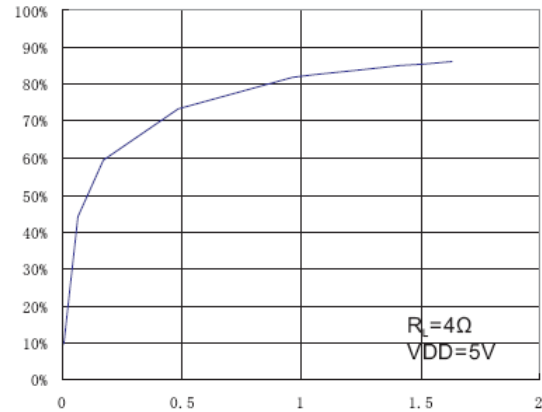


Typical Performance Characteristics (cont.) (@T_A = +25°C, unless otherwise specified.)

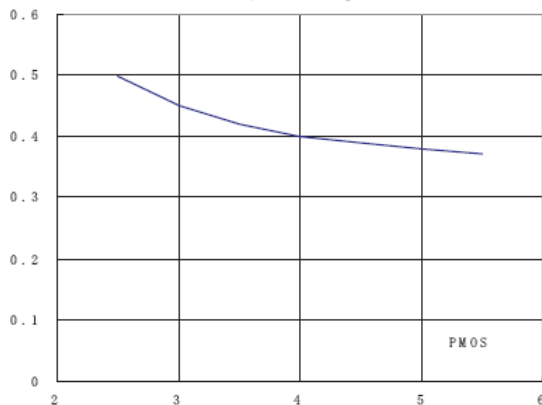
19. Efficiency VS Output Power



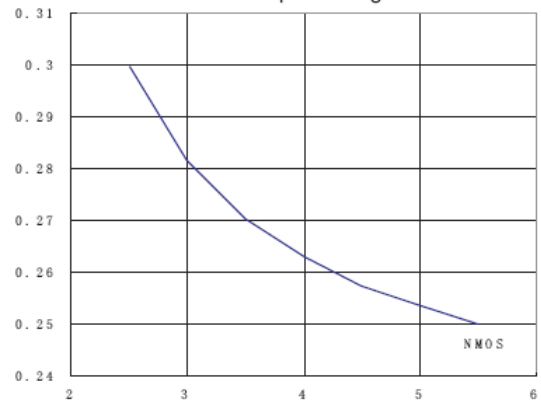
20. Efficiency VS Output Power



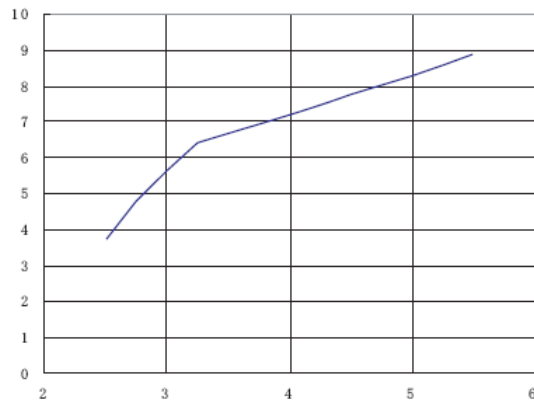
21. Rdson VS Input Voltage



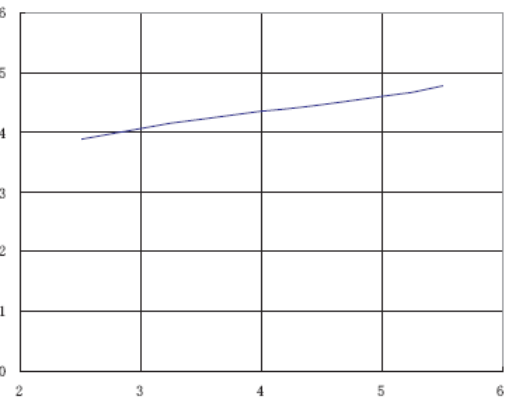
22. Rdson VS Input Voltage



23. Quiescent Current VS VDD(Class D)

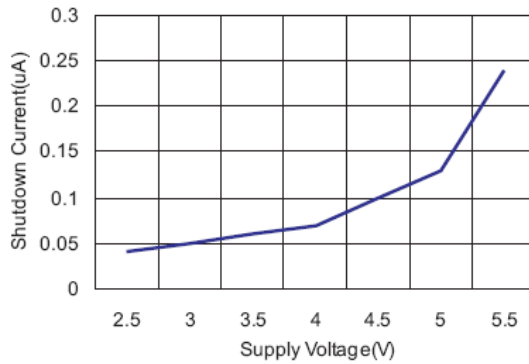


24. Quiescent Current VS VDD(Earphone)

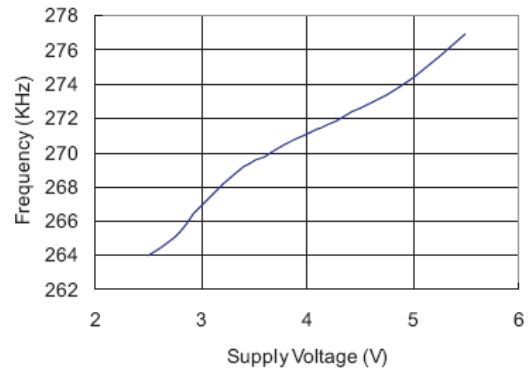


Typical Performance Characteristics (cont.) (@T_A = +25°C, unless otherwise specified.)

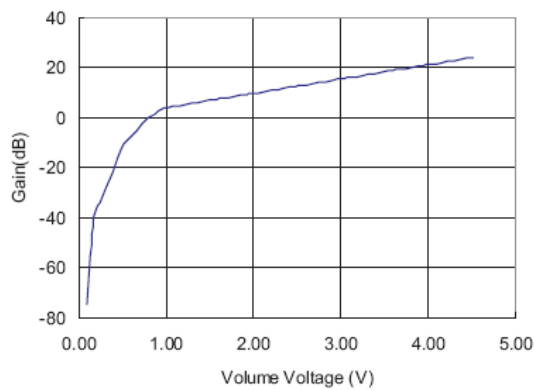
27. Shutdown Current



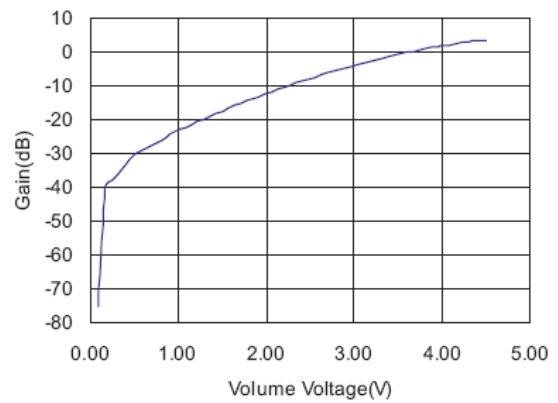
28. Switching Frequency (Class D)



29. Gain Control (Class D)



30. Gain Control (Earphone)



Typical Performance Characteristics (cont.) (@T_A = +25°C, unless otherwise specified.)

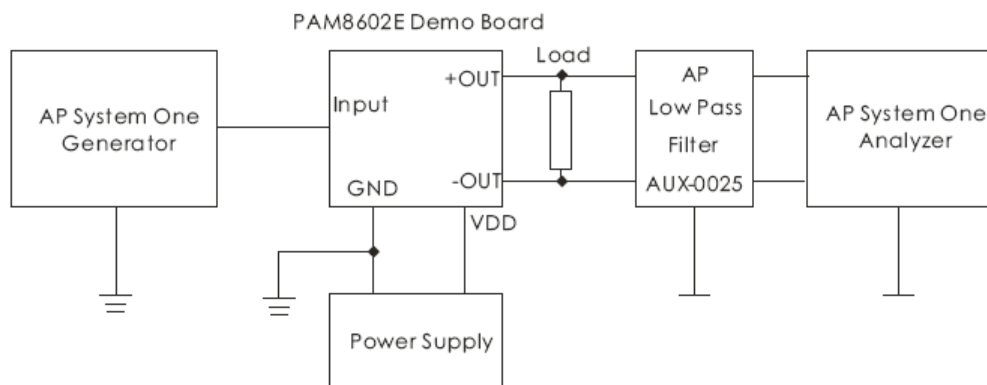
Table 1. DC Volume Control

STEP	Gain (dB) Class D	Gain (dB) Earphone		STEP	Gain (dB) Class D	Gain (dB) Earphone
0	-75	-75		32	11.6	-9.2
1	-40	-40		33	12.0	-8.6
2	-34	-38		34	12.4	-8.0
3	-28	-36		35	12.8	-7.4
4	-22	-34		36	13.2	-6.8
5	-16	-32		37	13.6	-6.2
6	-10	-30		38	14.0	-5.7
7	-7.5	-29		39	14.4	-5.2
8	-5.0	-28		40	14.8	-4.7
9	-2.5	-27		41	15.2	-4.2
10	0	-26		42	15.6	-3.7
11	1.5	-25		43	16.0	-3.2
12	3.0	-24		44	16.4	-2.7
13	4.0	-23		45	16.8	-2.2
14	4.4	-22.2		46	17.2	-1.8
15	4.8	-21.4		47	17.6	-1.4
16	5.2	-20.6		48	18.0	-1.0
17	5.6	-19.8		49	18.4	-0.6
18	6.0	-19.0		50	18.8	-0.2
19	6.4	-18.2		51	19.2	0.2
20	6.8	-17.4		52	19.6	0.6
21	7.2	-16.6		53	20.0	0.9
22	7.6	-15.9		54	20.4	1.2
23	8.0	-15.2		55	20.8	1.5
24	8.4	-14.5		56	21.2	1.8
25	8.8	-13.8		57	21.6	2.1
26	9.2	-13.1		58	22.0	2.4
27	9.6	-12.4		59	22.4	2.7
28	10.0	-11.7		60	22.8	2.9
29	10.4	-11.0		61	23.2	3.1
30	10.8	-10.4		62	23.6	3.3
31	11.2	-9.8		63	24.0	3.5

Application Information

Test Setup for Performance Testing (Class D)

1. When the PAM8602E works with LC filters, it should be connected with the speaker before it's powered on, otherwise it will be damaged easily.
2. When the PAM8602E works without LC filters, it's better to add a ferrite chip bead at the outgoing line of speaker for suppressing the possible electromagnetic interference.
3. The absolute maximum rating of the PAM8602E operation voltage is 6V. When the PAM8602E is powered with four battery cells, it should be noted that the voltage of four new dry or alkaline batteries is over 6V, higher than its maximum operation voltage, which probably make the device damaged. Therefore, it's recommended to use either four Ni-MH (Nickel Metal Hydride) rechargeable batteries or three dry or alkaline batteries.
4. The input signal should not be too high, if too high, it will cause the clipping of output signal when increasing the volume. Because the DC volume control of the PAM8602E has big gain, it will make the device damaged.
5. When testing the PAM8602E without LC filters by using resistor instead of speaker as the output load, the test results, e.g. THD or efficiency, will be worse than those using speaker as load.



- Notes:
1. The Audio Precision (AP) AUX-0025 low pass filter is necessary for class-D amplifier measurement with AP analyzer.
 2. Two 22 μ H inductors are used in series with load resistor to emulate the small speaker for efficiency measurement.

Mute Operation

The $\overline{\text{MUTE}}$ pin is an input for controlling the output state of the PAM8602E. A logic low on this pin disables the outputs, and a logic high enables the outputs. This pin may be used as a quick disable or enable of the outputs without a volume fade. Quiescent current is listed in the electrical characteristic table. The $\overline{\text{MUTE}}$ pin can be left floating due to the internal pull-up.

Shutdown Operation

In order to reduce power consumption while not in use, the PAM8602E contains shutdown circuitry to turn off the amplifier's bias circuitry. The amplifier is turned off when logic low is placed on the $\overline{\text{SHDN}}$ pin. By switching the $\overline{\text{SHDN}}$ pin connected to GND, the PAM8602E supply current draw will be minimized in idle mode. The $\overline{\text{SHDN}}$ pin can be left floating due to the pull-up.

For the best power on/off pop performance, the amplifier should be placed in the Mute mode prior to turning on/off the power supply.

Power Supply Decoupling

The PAM8602E is a high performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output THD and PSRR are as low as possible. Power supply decoupling affects low frequency on the power supply leads for higher frequency response. Optimum decoupling is achieved by using two capacitors of different types that target different types of noise frequency transients, spike, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1.0 μ F, placed as close as possible to the device V_{DD} terminal works best. For filtering lower-frequency noise signals, a large capacitor of 10 μ F (ceramic) or greater placed near the audio power amplifier is recommended.

Application Information

Input Capacitor (C_I)

Large input capacitors are both expensive and space hungry for portable designs. Clearly, a certain sized capacitor is needed to couple in low frequencies without severe attenuation. But in many cases the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 100Hz to 150Hz. Thus, using a large input capacitor may not increase actual system performance. In this case, input capacitor (C_I) and input resistance (R_I) of the amplifier form a high-pass filter with the corner frequency determined equation below,

$$f_c = \frac{1}{2\pi R_I C_I}$$

In addition to system cost and size, click and pop performance is affected by the size of the input coupling capacitor, C_I. A larger input coupling capacitor requires more charge to reach its quiescent DC voltage (nominally ½ V_{DD}). This charge comes from the internal circuit via the feedback and is apt to create pops upon device enable. Thus, by minimizing the capacitor size based on necessary low frequency response, turn-on pops can be minimized.

Analog Reference Bypass Capacitor (C_{BYP})

Analog Reference Bypass Capacitor (C_{BYP}) is the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode, C_{BYP} determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the internal analog reference to the amplifier, which appears as degraded PSRR and THD+N.

A ceramic bypass capacitor (C_{BYP}) of 0.47µF to 1.0µF is recommended for the best THD and noise performance. Increasing the bypass capacitor reduces clicking and popping noise from power on/off and entering and leaving shutdown.

Under Voltage Lock-Out (UVLO)

The PAM8602E incorporates circuitry designed to detect when the supply voltage is low. When the supply voltage drops to 1.8V or below, the PAM8602E outputs are disabled, and the device comes out of this state and states to normal functional once V_{DD} ≥ 2.0V.

Short Circuit Protection (SCP)

The PAM8602E has short circuit protection circuitry on the outputs that prevents the device from damage when output-to-output and output-to-GND short. When a short circuit is detected on the outputs, the outputs are disabled immediately. If the short was removed, the device activates again.

Over Temperature Protection

Thermal protection on the PAM8602E prevents the device from damage when the internal die temperature exceeds +135°C. There is a 15 degree tolerance on this point from device to device. Once the die temperature exceeds the thermal set point, the device outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 30°C. This large hysteresis will prevent motor boating sound well. The device begins normal operation at this point without external system interaction.

How to Reduce EMI (Electro Magnetic Interference)

A simple solution is to put an additional capacitor 1000µF at power supply terminal for power line coupling if the traces from amplifier to speakers are short (< 20CM).

Most applications require a ferrite bead filter as shown at Figure 1. The ferrite filter reduces EMI around 1MHz and higher. When selecting a ferrite bead, choose one with high impedance at high frequencies, and low impedance at low frequencies (MH2012HM221-T).

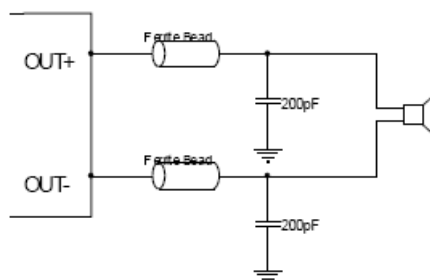


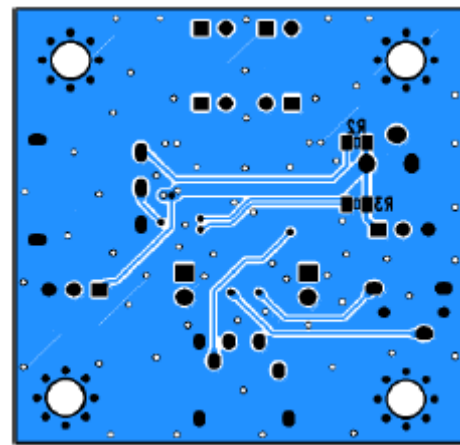
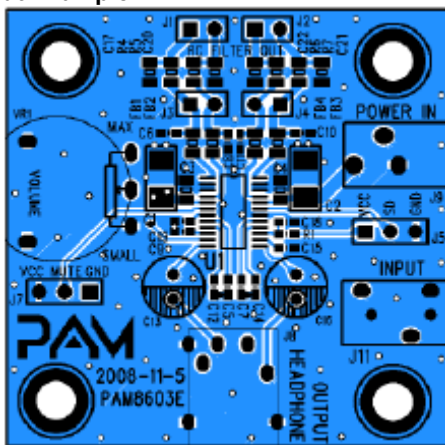
Figure 1. Ferrite Bead Filter to Reduce EMI

Application Information (cont.)

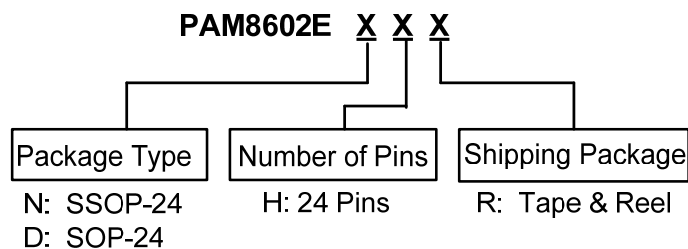
PCB Layout Guidelines Grounding

At this stage it is paramount to notice the necessity of separate grounds. Noise currents in the output power stage need to be returned to output noise ground and nowhere else. Were these currents to circulate elsewhere, they may get into the power supply, the signal ground, etc, worse yet, they may form a loop and radiate noise. Any of these cases results in degraded amplifier performance. The logical returns for the output noise currents associated with Class-D switching are the respective PGND pins for each channel. The switch state diagram illustrates that PGND is instrumental in nearly every switch state. This is the perfect point to which the output noise ground trace should return. Also note that output noise ground is channel specific. A two channel amplifier has two separate channels and consequently must have two separate output noise ground traces. The layout of the PAM8602E offers separate PGND connections for each channel and in some cases each side of the bridge. Output noise grounds must be tied to system ground at the power in exclusively. Signal currents for the inputs, reference, etc need to be returned to quiet ground. This ground is only tied to the signal components and the GND pin, and GND then tied to system ground.

PCB Layout Example

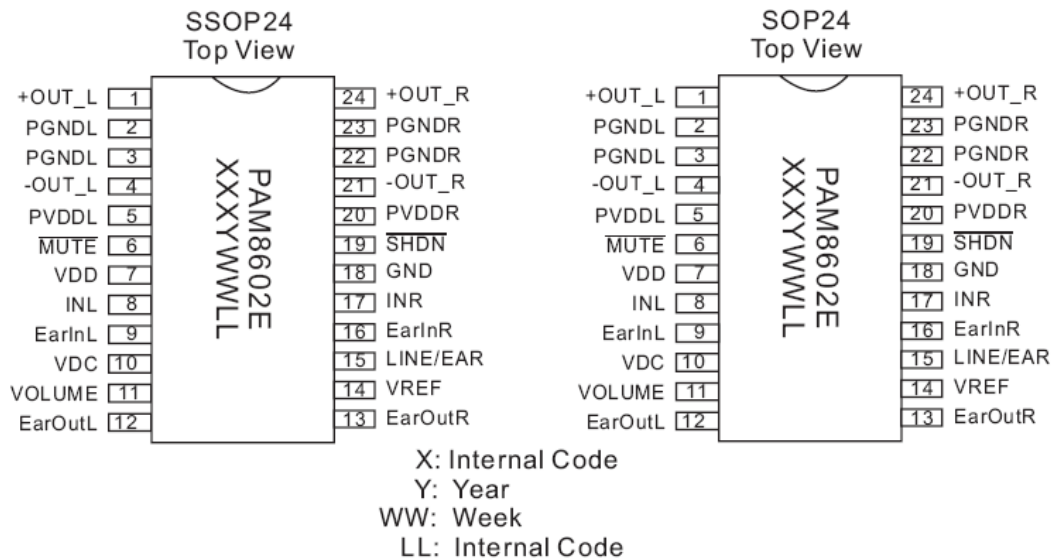


Ordering Information



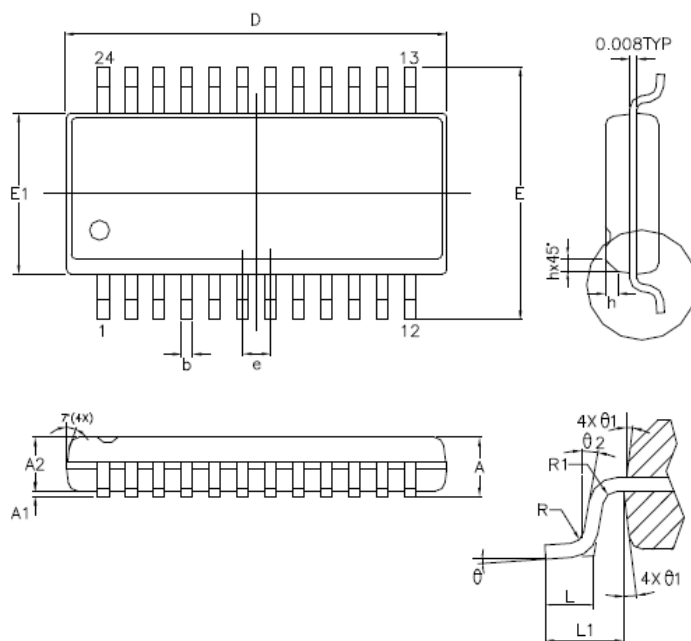
Part Number	Package Type	Standard Package
PAM8602ENHR	SSOP-24	2500 Units/Tape&Reel
PAM8602EDHR	SOP-24	100 Units/Tape&Reel

Marking Information



Package Outline Dimensions (All dimensions in mm.)

SSOP-24

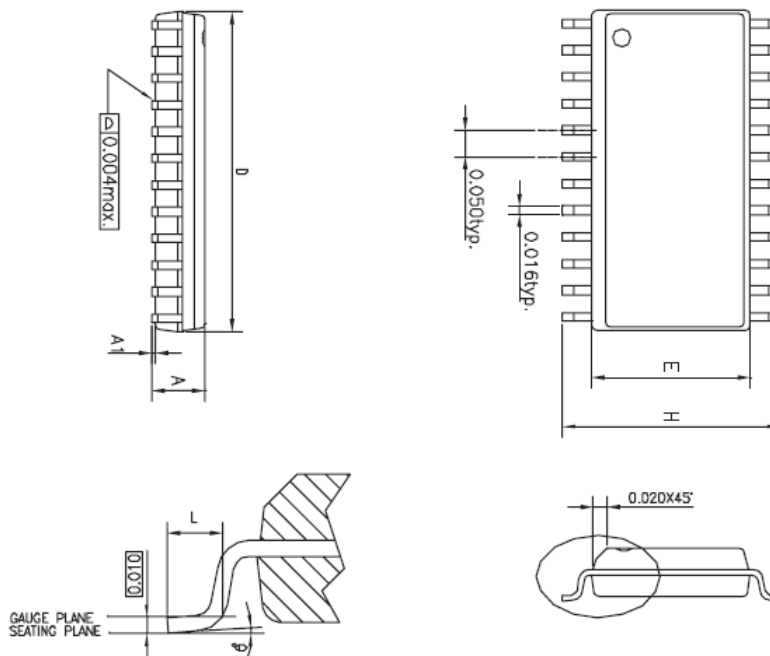


SYMBOLS	MIN.	NOM.	MAX.
A	0.053	0.061	0.069
A1	0.004	-	0.010
A2	0.049	0.057	0.065
b	0.008	0.010	0.012
D	0.335	0.341	0.347
E	0.228	0.236	0.244
E1	0.150	0.154	0.158
e	-	0.025	-
L	0.016	0.033	0.050
L1	0.041 REF		
R	0.003	-	-
R1	0.003	-	-
h	0.010	0.015	0.020
θ	0°	4°	8°
θ1	5°	10°	15°
θ2	0°	-	-

UNIT : INCH

Package Outline Dimensions (cont.) (All dimensions in mm.)

SOP-24



SYMBOLS	MIN.	NOM	MAX.
A	0.093	0.099	0.104
A1	0.004	-	0.012
D	0.599	0.600	0.614
E	0.291	0.295	0.299
H	0.394	0.406	0.419
L	0.016	0.035	0.050
θ°	0	-	8

UNIT : INCH

NOTES:

1. JEDEC OUTLINE : MS-013 AD
2. DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.006in) PER SIDE.
3. DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.

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