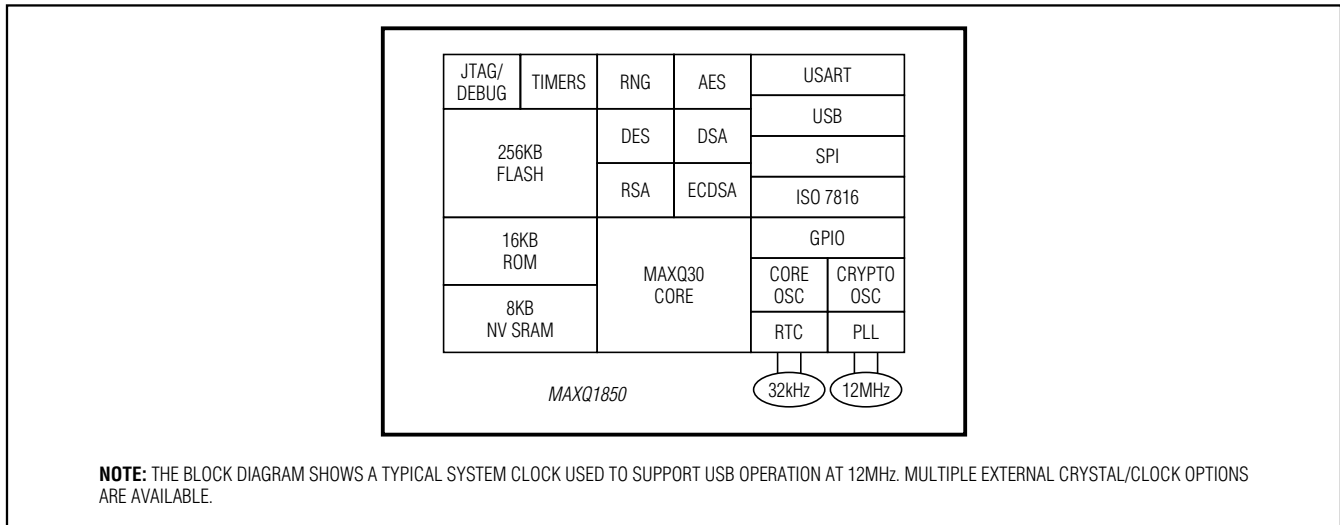


ABRIDGED DATA SHEET

MAXQ1850

DeepCover Secure Microcontroller with Rapid Zeroization Technology and Cryptography

Block Diagram



Detailed Features

- ◆ High-Performance, Low-Power, 32-Bit MAXQ30 RISC Core
- ◆ Single 3.3V Supply Enables Low Power/Flexible Interfacing
- ◆ DC to 16MHz Code Execution Across Entire Operating Range
- ◆ 65MHz Cryptography Engine Execution to Reduce Processing Time
- ◆ On-Chip 2x/4x Clock Multiplier
- ◆ 33 Instructions
- ◆ Three Independent Data Pointers Accelerate Data Movement with Automatic Increment/Decrement
- ◆ 16-Bit Instruction Word, 32-Bit Internal Data Bus
- ◆ 16 x 32-Bit Accumulators
- ◆ Up to 16 General-Purpose I/O Pins
- ◆ 5V Tolerant I/O
- ◆ Virtually Unlimited Software Stack
- ◆ Optimized for C-Compiler (High-Speed/Density Code)
- ◆ Memory Features
 - 256KB Flash, Composed of 2048 Byte Sectors (1K Erase/Write Cycles per Sector)
 - 8KB Battery-Backed Data SRAM
 - Dedicated Cryptographic Memory Space

Security Features

- Unique ID
- Tamper Detection with Rapid Key/Data Destruction
- Four Self-Destruct Inputs
- Hardware AES and DES Engines
- Public Key Cryptographic Accelerator for DSA, ECDSA, and RSA
- Supports SHA-1, SHA-224, and SHA-256
- Real Hardware RNG and PRNG
- Hardware CRC-32/16
- Unalterable, Battery-Backed Real-Time Clock

Additional Peripherals

- Power-Fail Warning
- Power-On Reset/Brownout Reset
- JTAG I/F for System Programming and Accessing On-Chip Debugger
- USB I/F with Four End-Point Buffers
- ISO 7816 Smart Card UART with FIFO
- Four 16-Bit Timer/Counters, Two with PWM Function
- SPI and USART Communication Ports
- Programmable Watchdog Timer

Low-Power Consumption

- 150nA Typical Current Draw in Battery-Backed Mode, Preserving 8KB NV SRAM and with Security Sensors Active (460nA with RTC Active)

Note to readers: This document is an abridged version of the full data sheet. To request the full data sheet, go to www.maximintegrated.com/MAXQ1850 and click on **Request Full Data Sheet**.